NCP1600

High Voltage PFC Controller with Standby Power Saving

The NCP1600 is an active power factor correction controller that operates as a boost pre−converter in off−line power supply applications. NCP1600 is optimized for low to medium power, high−density power supplies requiring a minimum board area, reduced component count and low power dissipation. Two comparators are built into this device to improve standby (power) efficiency. With these two comparators, the PFC controller automatically switches itself in between normal mode and standby mode (skip or off mode) to save power consumption during light load conditions.

The NCP1600 can achieve deliver follow−boost operation that is an innovative mode allowing a drastic size reduction of both the inductor and the power switch. Ultimately, the solution system cost is significantly lowered. NCP1600 can also work in a traditional constant output voltage mode and intermediate solutions can be easily implemented. This flexibility makes it ideal to optimally cope with a wide range of applications.

Features

- Lose Less High−Voltage Startup Source
- Standard Constant Output Voltage or “Follow−Boost” Mode
- PFC Skip Mode and Off Mode under Light Load Conditions
- Selectable Switching Frequency Clamp
- Disable Pin to Stop PFC Operation
- Restart Delay Timer
- Brown−out Protection for Startup
- Feedback Loop Open Detection
- Output Overvoltage Comparator
- Switch Mode Operation: Voltage Mode
- Constant On−Time Operation That Saves the Use of an Extra Multiplier
- Improved Regulation Block Dynamic Behavior
- Internally Trimmed Reference Current Source
- Internal Leading Edge Blanking (LEB) for Noise Immunity

Typical Applications

- Monitor/TV Power Supplies
- PC Power Supplies
- Notebook PC Adapters
- Medium Power Adapters

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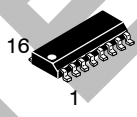
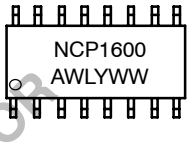
MARKING DIAGRAM

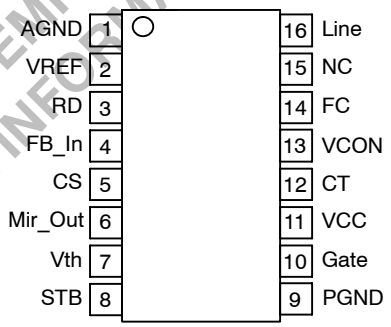


SO−16
D SUFFIX
CASE 751B



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP1600D	SO−16	48 Units / Rail

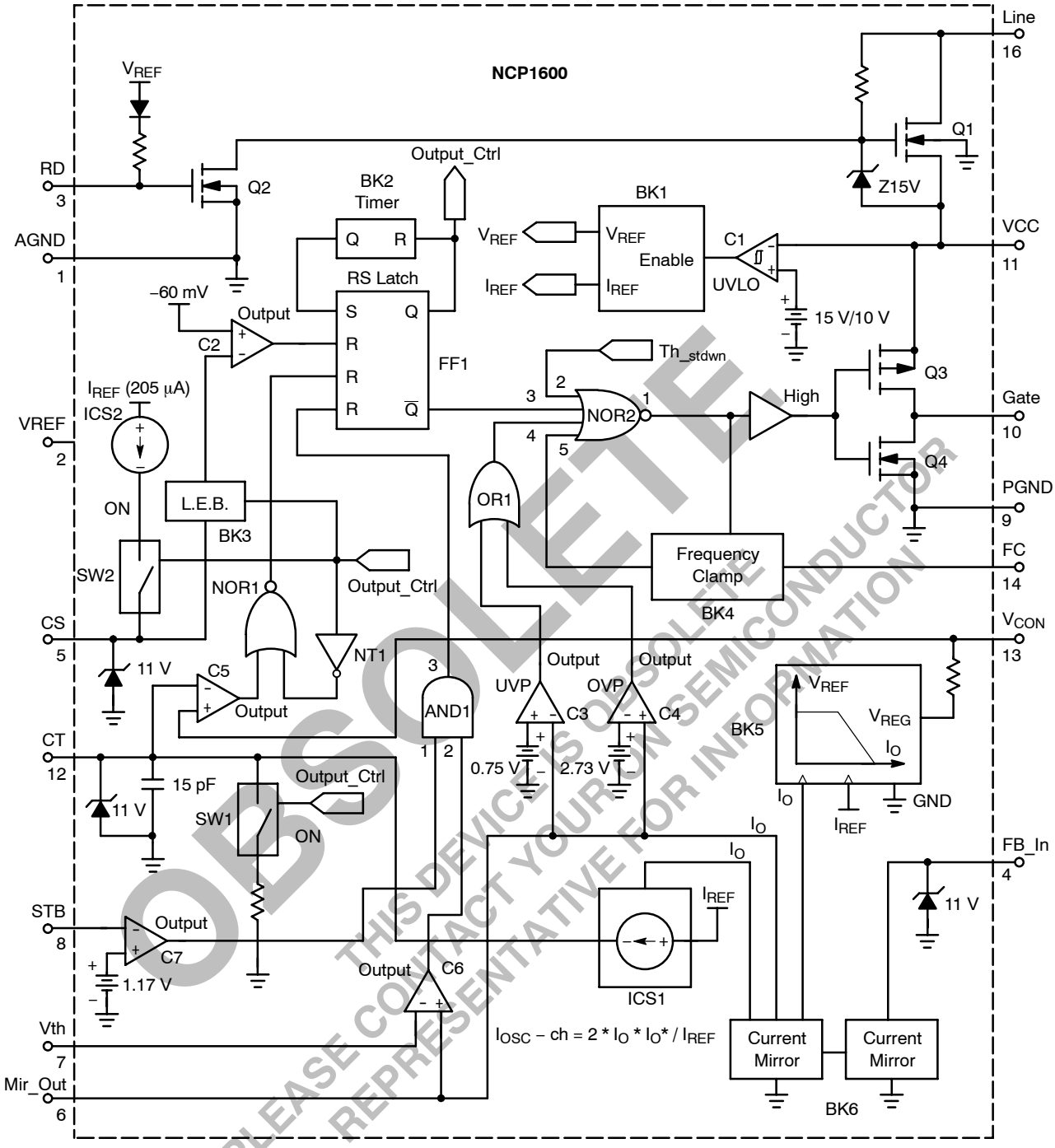


Figure 1. Detailed Functional Diagram

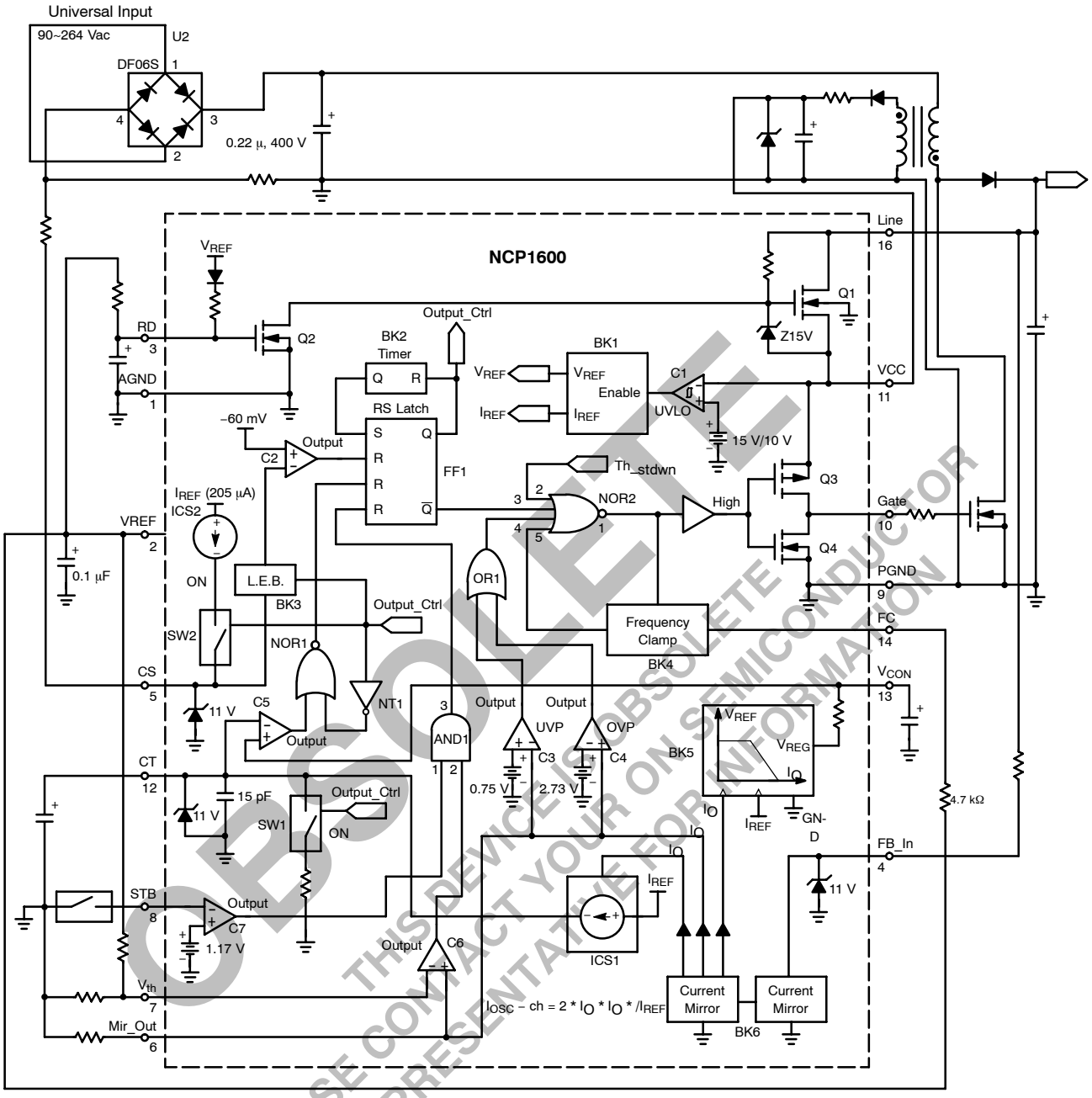


Figure 2. Representative Application Circuit

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Description
1	AGND	Analog Ground.
2	V_{REF}	Output reference voltage 6.5 V.
3	Restart Delay, RD	This pin is a high impedance input and is typically connected to a resistor and capacitor to setup the Delay Time. After this delay time, the IC will turn off the internal startup FET Q1.
4	FB_In	This pin is designed to receive a current that is proportional to the pre−converter output voltage.
5	CS	This pin is designed to receive a negative voltage signal proportional to the current flowing through the inductor. This information is generally built using a sense resistor. The Zero Current Detection prevents any restart as long as the Pin 5 voltage is below (−60 mV). This pin is also used to perform the peak current limitation. The resistor connected between the pin and the current−sense−resistor programs the overcurrent threshold.
6	Mir_Out	The Current Mirror delivers one current which is the same as the Pin 4 (FB_In) input current. This current information is used for disabling the PFC boost pre−converter during Standby, Overvoltage and Undervoltage conditions.
7	V_{th}	This pin divides the reference voltage to design the minimum threshold voltage of PFC Output Voltage during standby.
8	STB	PFC boost pre−converter standby pin. The PFC enters standby mode (PFC boost pre−converter enter both skip mode and off mode) when voltage at this pin falls below 1.17 V. This pin also can be connected to the PWM feedback pin.
9	PGND	Power Ground.
10	Gate	The gate drive current capability is suited to drive an IGBT or a power MOSFET.
11	V_{CC}	This pin is the positive supply of the IC. The circuit turns on when V_{CC} becomes higher than 15 V, the operating range after startup being 8.0 V up to 30 V.
12	C_T	The circuit uses an on−time control mode. This on−time is controlled by comparing the C_T voltage to the $V_{control}$ voltage. C_T is charged by the squared feedback current.
13	V_{CON}	This pin makes available the regulation block output. The capacitor connected between this pin and ground adjusts the control bandwidth. It is typically set below 20 Hz to obtain a nondistorted input current.
14	Freq. Clamp, FC	Connecting a resistor and capacitor on this pin to program the maximum switch frequency.
15	NC	No connection.
16	Line	This pin connects directly to the rectified AC line voltage source.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Transient), Pin 11 to both the AGND Pin and PGND Pin	V_{CC}	30	V
Power Supply Voltage (Operating), Pin 11 to both the AGND Pin and PGND Pin	V_{CC}	25	V
Line Voltage, Pin 16 to both the AGND Pin and PGND Pin	V_{Line}	500	V
Power Supply Voltage on all Pins Except Pin 4, Pin 11, Pin 16, and Pin 10	–	−0.3 to +10	V
Feedback Pin Voltage, Pin 4 to both the AGND Pin and PGND Pin	V_{FB_In}	−0.3 to +6.5	V
Gate Pin Voltage, Pin10 to both the AGND Pin and PGND Pin	V_{Gate}	−0.3 to 15	V
Restart Diode Current	I_{IN}	5.0	mA
Gate Driver Output Current, Source or Sink, Pin 10	I_{Gate}	1.0	A
Power Dissipation and Thermal Characteristic D Suffix, Plastic Package Case 751B Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$	 550 145	 mW °C/W
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
2. Latchup Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

ELECTRICAL CHARACTERISTICS (V_{CC} = 17 V, for typical values T_J = 25°C, for min/max values T_J = −25 to +125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATION SECTION					
Regulation High Current Reference	I_{REF}	190	200	205	μA
Ratio (Regulation Low Current Reference)/I_{REF}	I_{reg-L}/I_{reg-H}	0.965	0.977	0.99	–
$V_{control}$ Impedance	$Z_{vcontrol}$	–	300	–	kΩ
Feedback Pin Clamp Voltage @ I_{FB} = 100 μA Feedback Pin Clamp Voltage @ I_{FB} = 200 μA	V_{FB-100} V_{FB-200}	2.0 3.0	2.6 3.5	3.0 4.0	V
VOLTAGE REFERENCE					
Voltage Reference (I_O = 0 mA)	V_{REF}	6.25	6.5	6.75	V
Line Regulation (V_{CC} = 11 V to 25 V)	Reg_{line}	–	5.0	125	mV
Load Regulation (I_O = 0 to 5.0 mA)	Reg_{load}	–	45	125	mV
Total Output Variation Over Line, Load and Temperature	V_{REF}	6.25	6.5	6.75	V
Maximum Output Current	I_O	5.0	35	–	mA
FREQUENCY CLAMP					
Frequency Clamp Input Threshold	$V_{th\ (FC)}$	1.9	2.0	2.1	V
Frequency Clamp Capacitor Reset Current (V_{FC} = 0.5 V)	I_{Reset}	0.5	1.5	4.0	mA
Frequency Clamp Disable Voltage	V_{DFC}	7.0	7.8	8.0	V
V_{CC} HYSTERESIS					
Startup Threshold (V_{CC} Increasing)	$V_{th(ON)}$	12.5	15	17	V
Minimum Operating Voltage After Turn−On (V_{CC} Decreasing)	$V_{Shutdown}$	8.0	9.5	10.5	V
Hysteresis	V_H	–	5.5	–	V
TIMER					
Minimum Off Time	t_{OFF}	1.2	1.8	2.7	μs
CURRENT MIRROR					
Current Mirror Radio at 200 μA Input Current when 13 kΩ Resistor on Mir_Out Pin	I_{OUT}/I_{IN}	0.99	1.02	1.07	–
OSCILLATOR SECTION					
Maximum Oscillator Swing	ΔVT	1.35	1.44	1.6	V
Charge Current @ I_{FB} = 100 μA	$I_{charge-100}$	87.5	98	112.5	μA
Charge Current @ I_{FB} = 200 μA	$I_{charge-200}$	350	380	450	μA
Ratio Multiplier Gain Over Maximum Swing	K_{OSC}	5600	7050	7600	1/(V,A)
Average Internal Oscillator Pin Capacitance Over Oscillator Maximum Swing (C_T Voltage Varying From 0 up to 1.5 V)	C_{int}	–	15	–	pF
Discharge Time	T_{disch}	–	0.5	1.0	μS
CURRENT SENSE SECTION					
Zero Current Detection Comparator Threshold	V_{ZCD-th}	−95	−60	−15	mV
Negative Clamp Level (I_{CS} − pin = −1.0 mA)	C_{I-neg}	−0.9	−0.7	−0.3	V
Bias Current @ VCS = V_{ZCD-th}	I_{b-cs}	−0.2	–	–	μA
Propagation Delay (VCS > V_{ZCD-th}) to Gate Drive High	T_{ZCD}	–	500	–	nS
Current Sense Pin Internal Current Source	I_{OCP}	225	245	260	μA
Leading Edge Blanking Duration	t_{LED}	–	400	–	nS
Overvoltage Protection Propagation Delay (VCS < V_{ZCD-th} to Gate Drive Low)	T_{OCP}	–	160	–	nS

ELECTRICAL CHARACTERISTICS (V_{CC} = 17 V, for typical values T_J = 25°C, for min/max values T_J = −25 to +125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
GATE DRIVER OUTPUT					
Source Resistance (C_T = 0 V, V_{Gate} = 14 V) Sink Resistance (C_T = 2.0 V, V_{Gate} = 1.0 V)	R_{OH} R_{OL}	4.0 4.0	11 8.1	20 20	Ω
Output Voltage Rise Time (10%−90%) (C_L = 1.0 nF)	t_r	–	14	200	ns
Output Voltage Fall Time (90%−10%) (C_L = 1.0 nF)	t_f	–	14	200	ns
Output Voltage in Undervoltage (V_{CC} = 10 V, I_{sink} = 1.0 mA)	$V_{O(UV)}$	–	–	0.25	V
OVERVOLTAGE PROTECTION SECTION					
Overvoltage Protection Threshold (C4 Comparator)	V_{C4}	2.65	2.73	2.8	V
Propagation Delay (V_{Pin6} > 2.73 V to Gate Drive Low)	T_{OVP}	–	500	–	ns
UNDERVOLTAGE PROTECTION SECTION					
Undervoltage Protection Threshold (C3 Comparator)	V_{C3}	0.65	0.75	0.8	V
Propagation Delay (V_{Pin6} < 0.75 V to Gate Drive Low)	T_{UVLO}	–	500	–	ns
STANDBY SECTION					
Standby Threshold (C7 Comparator)	V_{C7}	1.1	1.17	1.25	V
Propagation Delay (V_{Pin8} < 1.17 V to Gate Drive Low)	T_{OVP}	–	500	–	ns
THERMAL SHUTDOWN SECTION					
Thermal Shutdown Threshold	T_{stdwn}	–	160	–	°C
Hysteresis	ΔT_{stdwn}	–	36	–	°C
TOTAL DEVICE					
Line Startup Current (V_{CC} = 0 V, V_{Line} = 50 V) (T_A = −25°V to +100°C)	I_{SU}	2.0	12.2	20	mA
Line Operating Current (V_{CC} = $V_{th(ON)}$, V_{Line} = 50 V)	I_{OP}	–	10	20	mA
V_{CC} Dynamic Operating Current (50 kHz, C_L = 1.0 nF) V_{CC} Static Operating Current (I_O = 0)	I_{CC}	– –	4.9 3.9	8.5 –	mA
Line Pin Leakage (V_{Line} = 500 V)	I_{Line}	–	20	80	μA

TYPICAL CHARACTERISTICS (Junction Temperature from −25°C to 125°C)

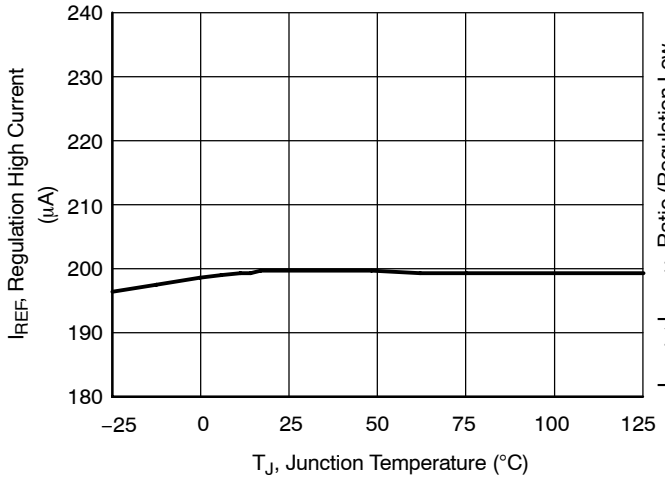


Figure 3. Regulation High Current Reference vs. Junction Temperature

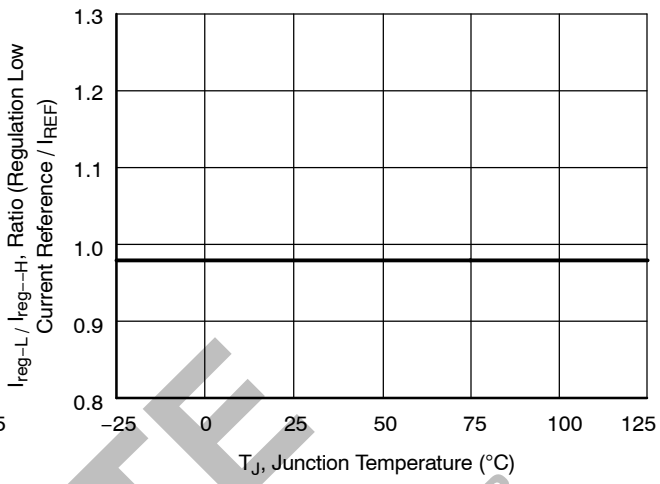


Figure 4. Ratio (Regulation Low Current Reference / I_{REF}) vs. Junction Temperature

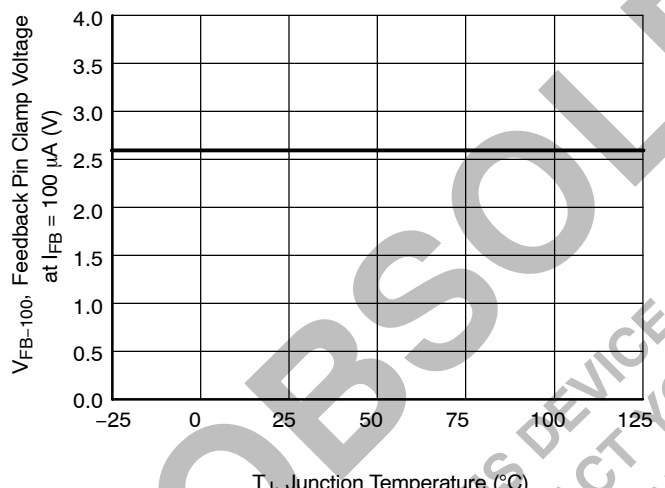


Figure 5. Feedback Pin Clamp Voltage at I_{FB} = 100 μA vs. Junction Temperature

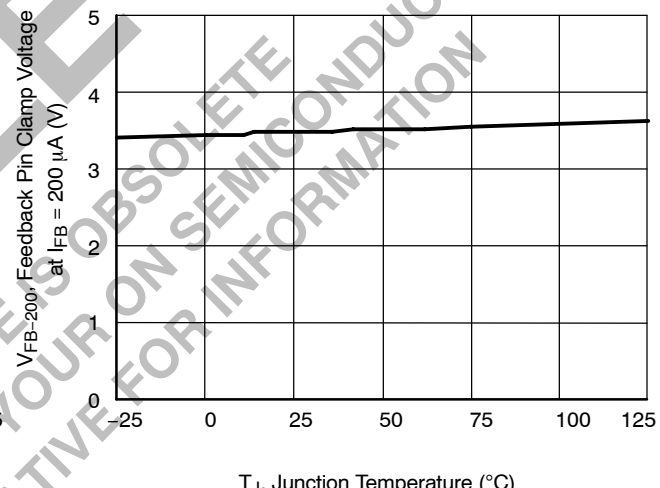


Figure 6. Feedback Pin Clamp Voltage at I_{FB} = 200 μA vs. Junction Temperature

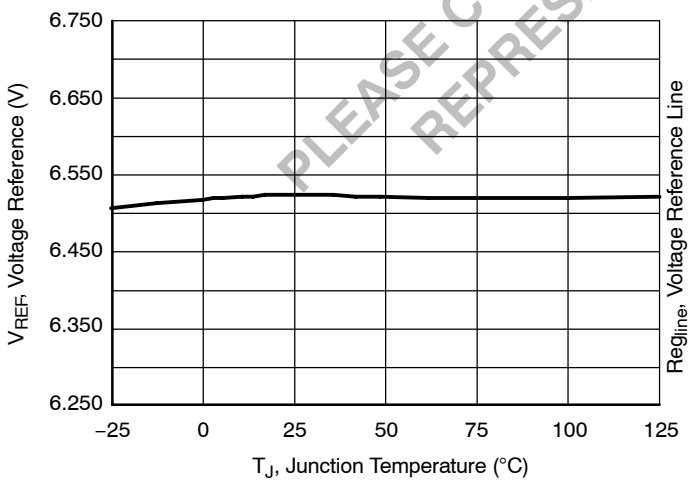


Figure 7. Voltage Reference (I_O = 0 mA) vs. Junction Temperature

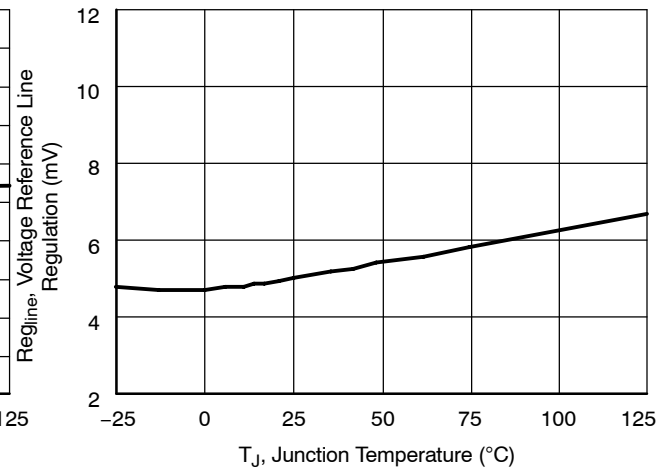


Figure 8. Voltage Reference Line Regulation (V_{CC} = 11 V to 25 V) vs. Junction Temperature

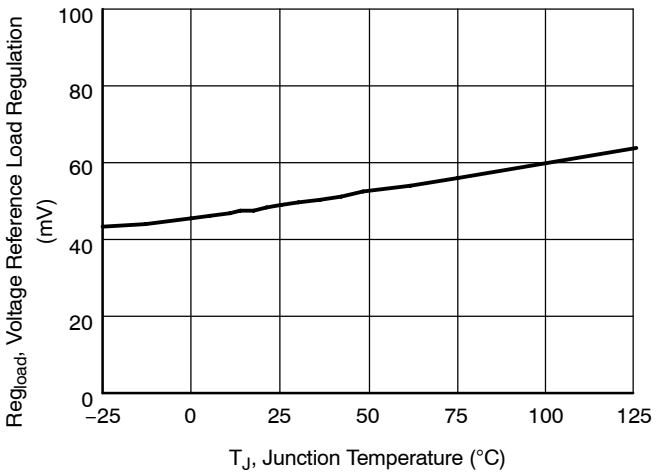


Figure 9. Voltage Reference Load Regulation (I_O = 0 to 5 mA) vs. Junction Temperature

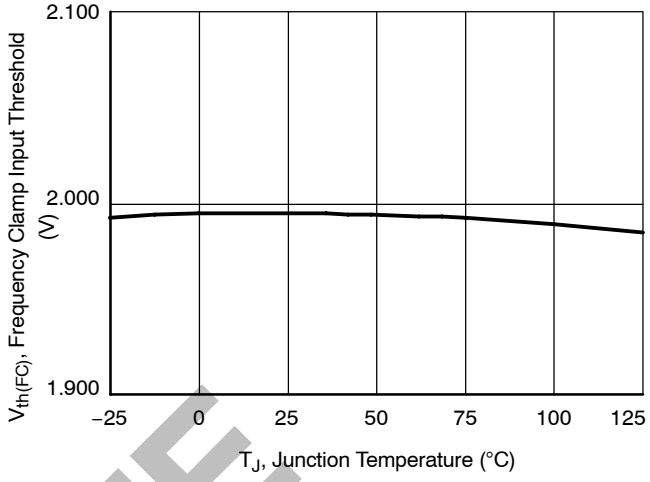


Figure 10. Frequency Clamp Input Threshold vs. Junction Temperature

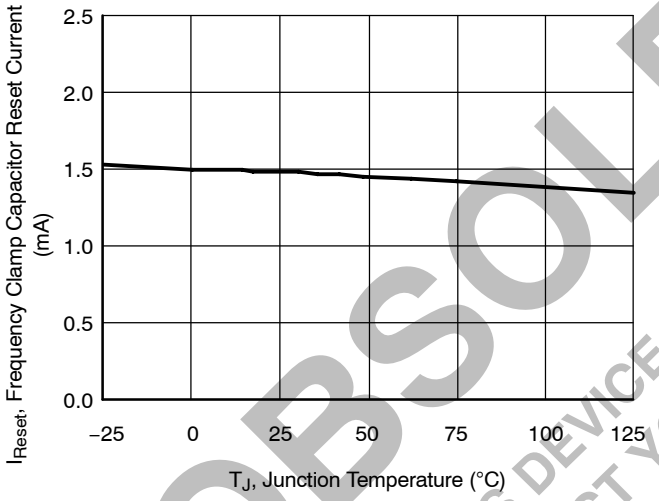


Figure 11. Frequency Clamp Capacitor Reset Current (V_{FC} = 0.5 V) vs. Junction Temperature

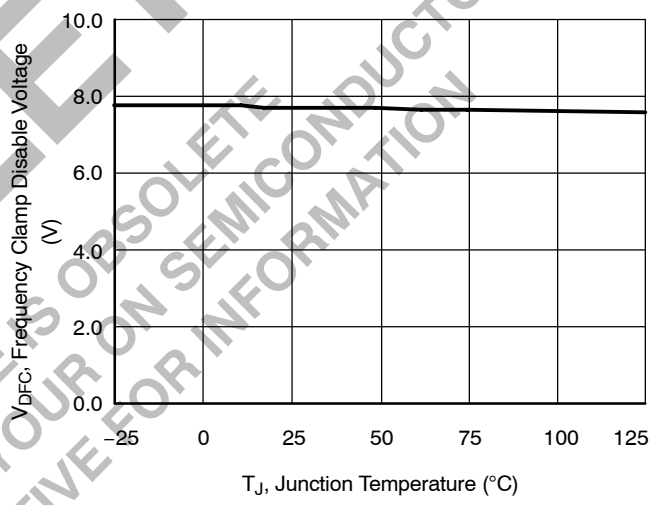


Figure 12. Frequency Clamp Disable Voltage vs. Junction Temperature

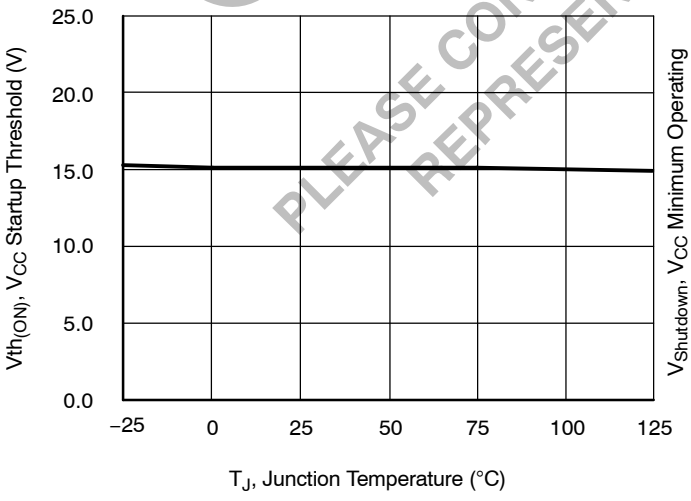


Figure 13. V_{CC} Startup Threshold vs. Junction Temperature

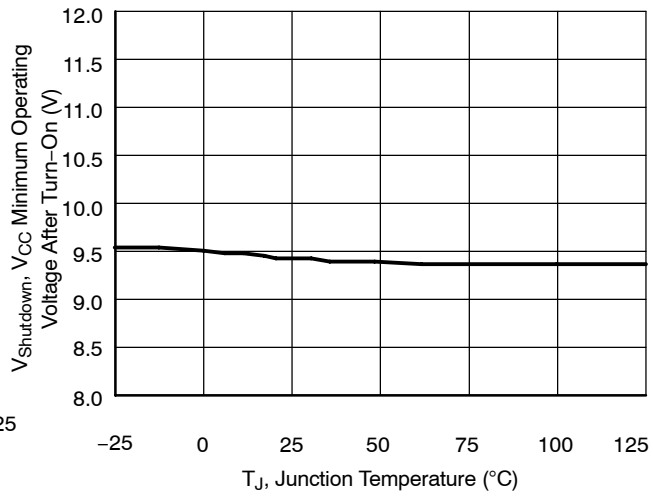


Figure 14. V_{CC} Minimum Operating Voltage After Turn−On vs. Junction Temperature

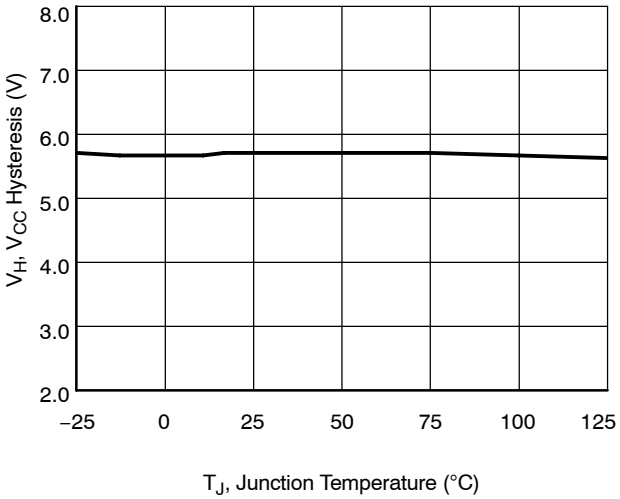


Figure 15. V_{CC} Hysteresis vs. Junction Temperature

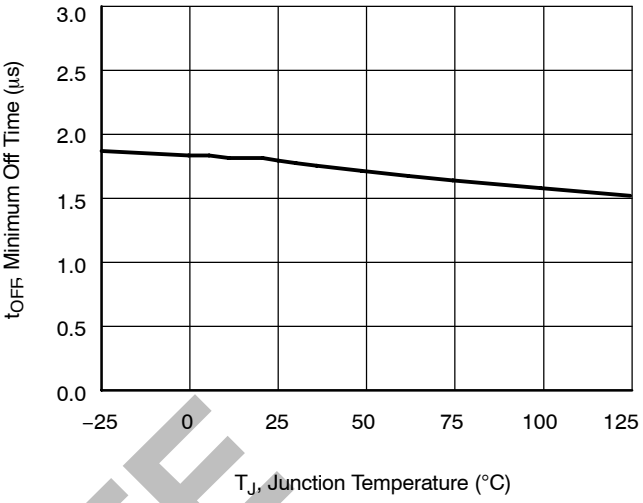


Figure 16. Minimum Off Time vs. Junction Temperature

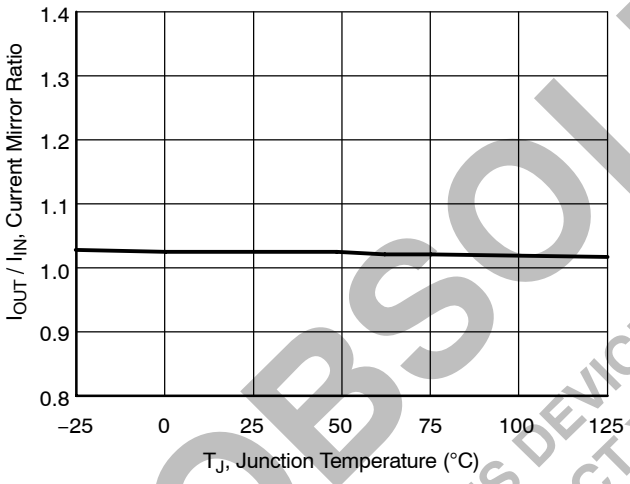


Figure 17. Current Mirror Ratio vs. Junction Temperature

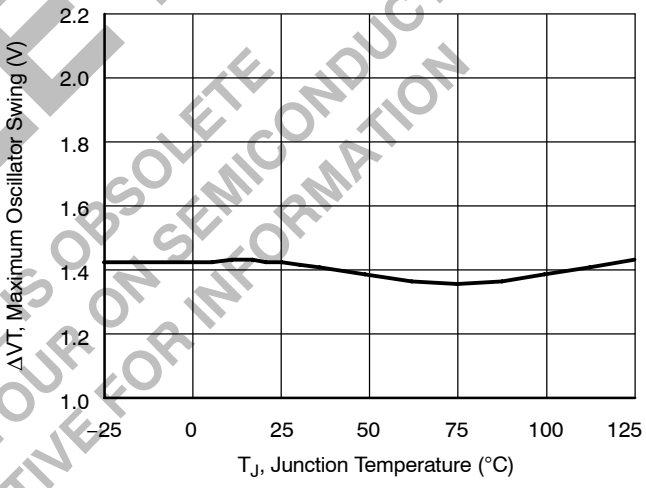


Figure 18. Maximum Oscillator Swing vs. Junction Temperature

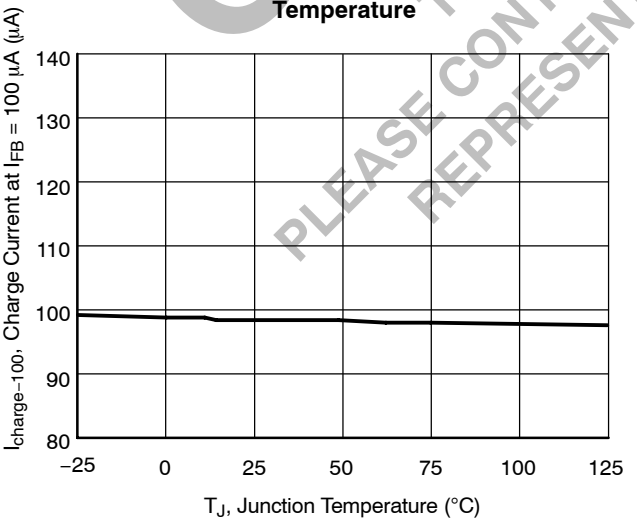


Figure 19. Charge Current at I_{FB} = 100 μA vs. Junction Temperature

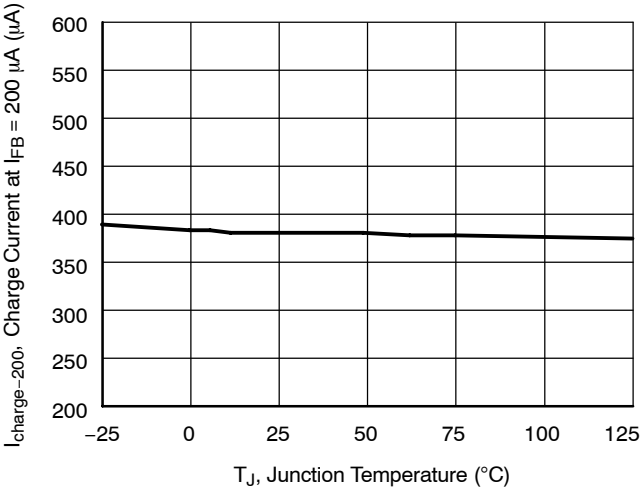


Figure 20. Charge Current at I_{FB} = 200 μA vs. Junction Temperature

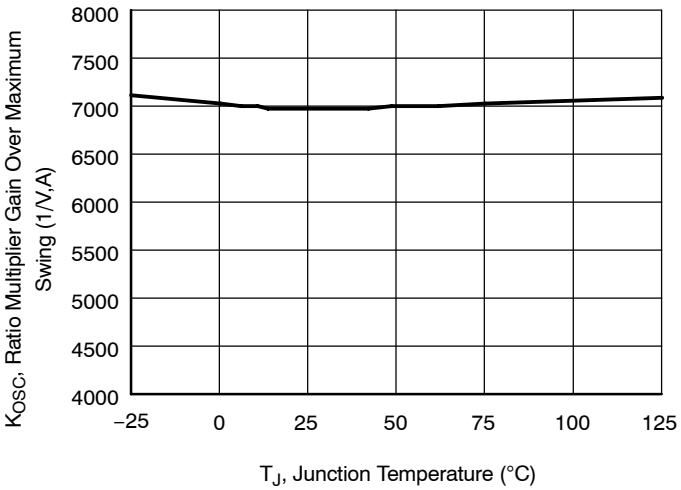


Figure 21. Ratio Multiplier Gain Over Maximum Swing vs. Junction Temperature

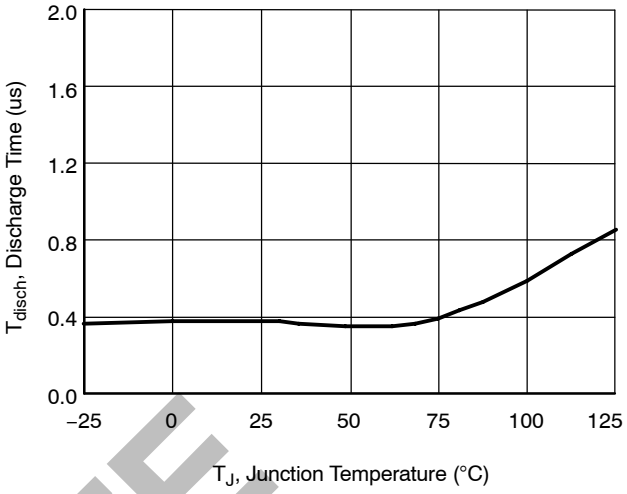


Figure 22. Discharge Time vs. Junction Temperature

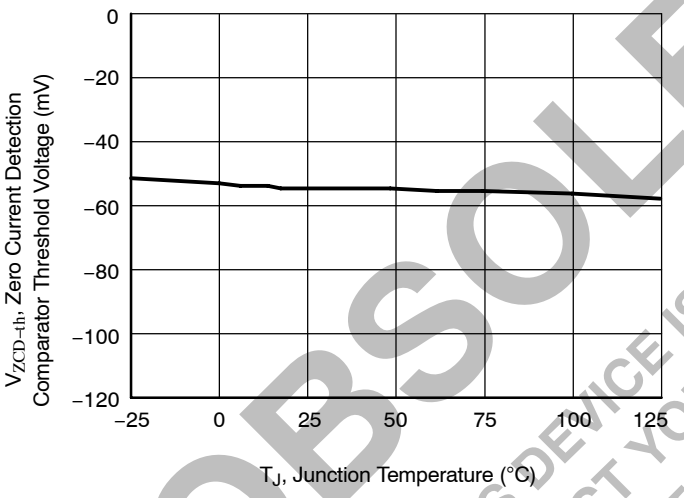


Figure 23. Zero Current Detection Comparator Threshold Voltage vs. Junction Temperature

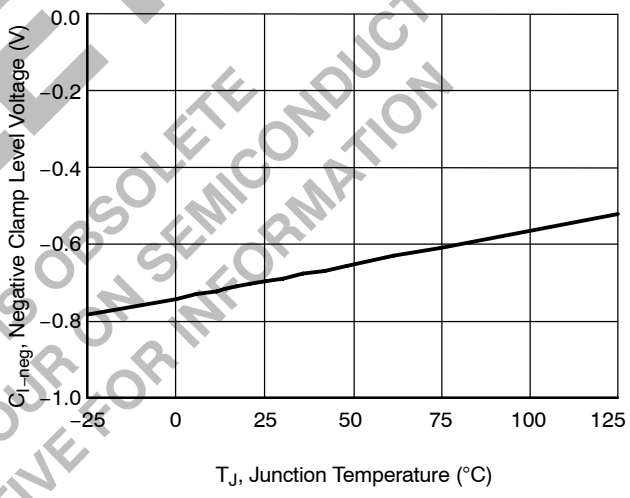


Figure 24. Negative Clamp Level Voltage vs. Junction Temperature

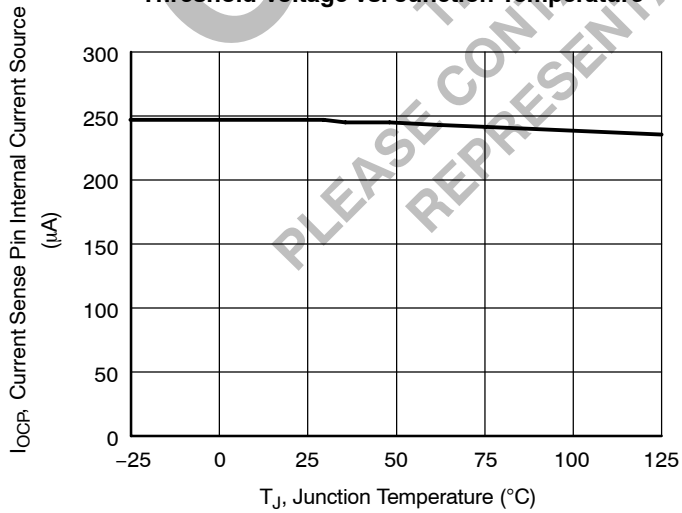


Figure 25. Current Sense Pin Internal Current Source vs. Junction Temperature

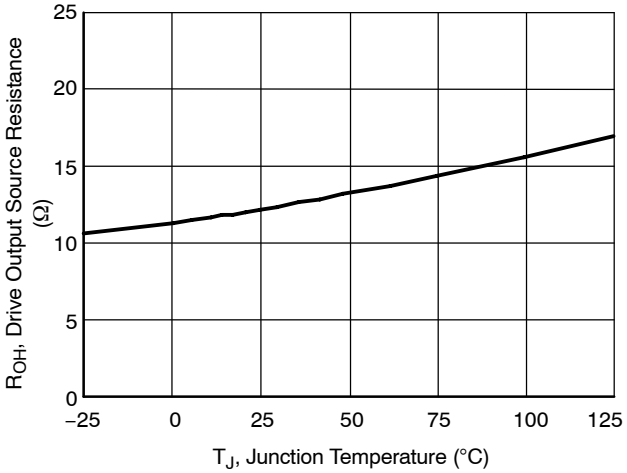


Figure 26. Drive Output Source Resistance vs. Junction Temperature

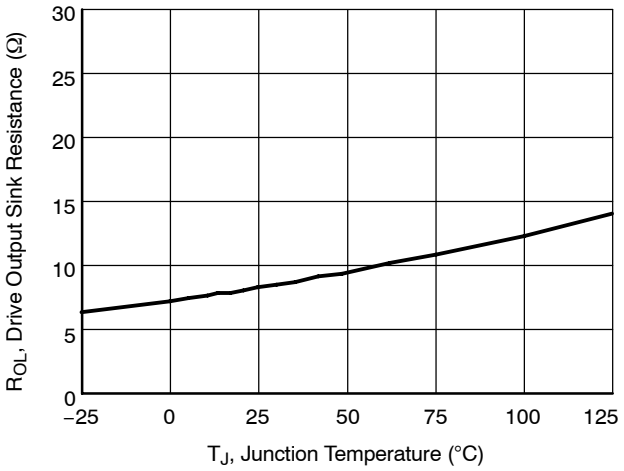


Figure 27. Drive Output Sink Resistance vs. Junction Temperature

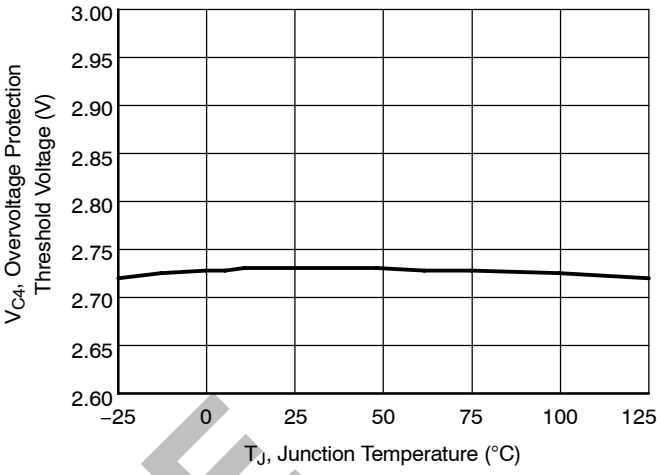


Figure 28. Overvoltage Protection Threshold Voltage vs. Junction Temperature

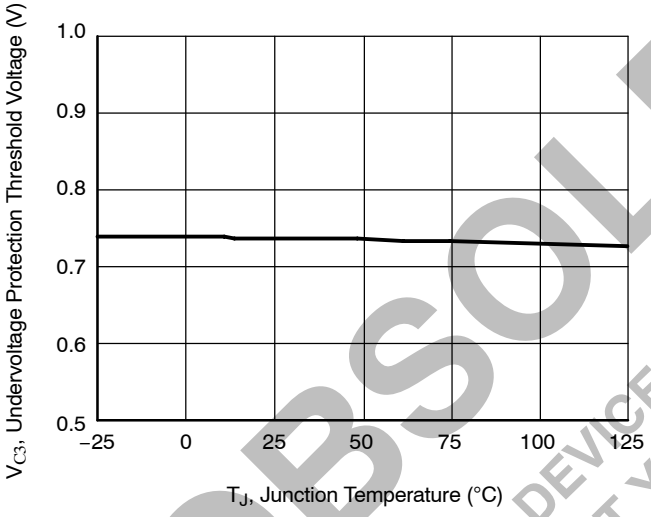


Figure 29. Undervoltage Protection Threshold Voltage vs. Junction Temperature

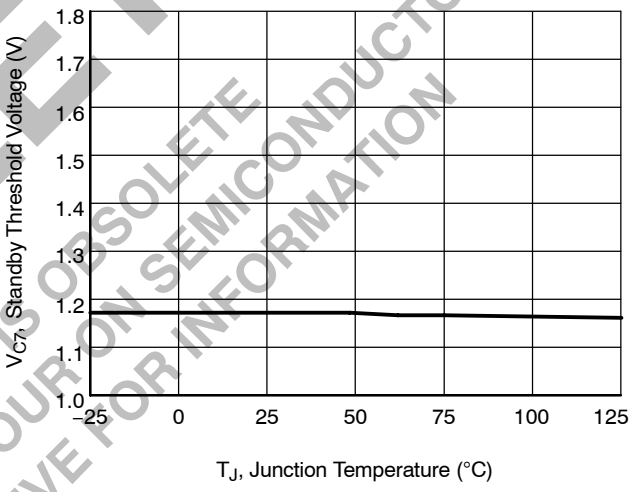


Figure 30. Standby Threshold Voltage vs. Junction Temperature

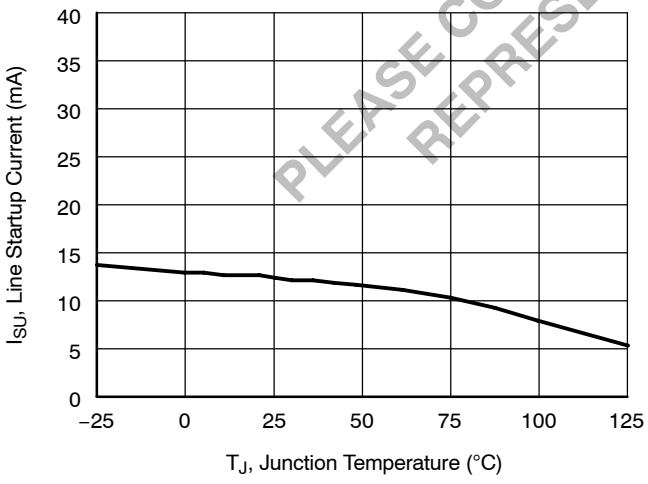


Figure 31. Line Startup Current vs. Junction Temperature

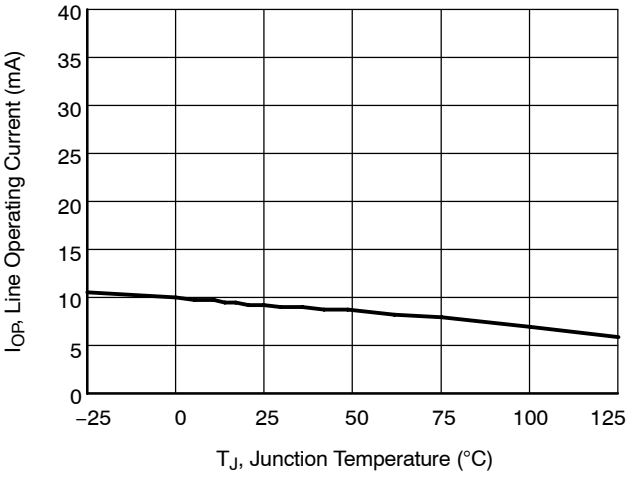


Figure 32. Line Operating Current vs. Junction Temperature

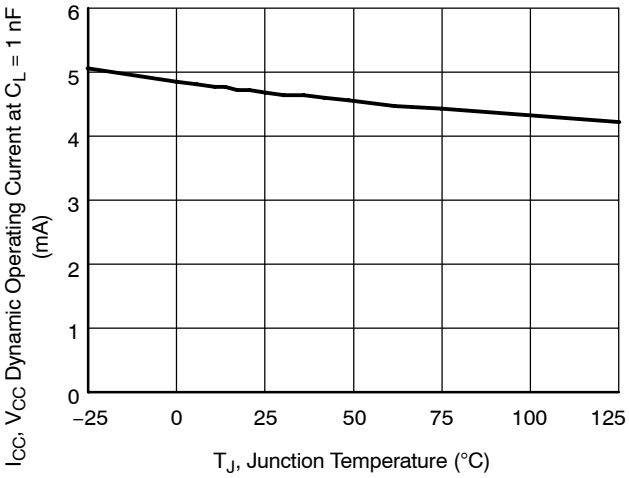


Figure 34. V_{CC} Dynamic Operating Current at C_L = 1.0 nF vs. Junction Temperature

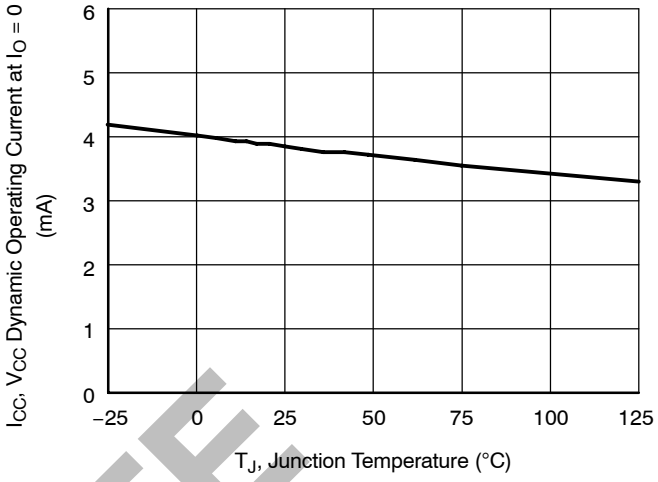


Figure 35. V_{CC} Dynamic Operating Current at I_O = 0 vs. Junction Temperature

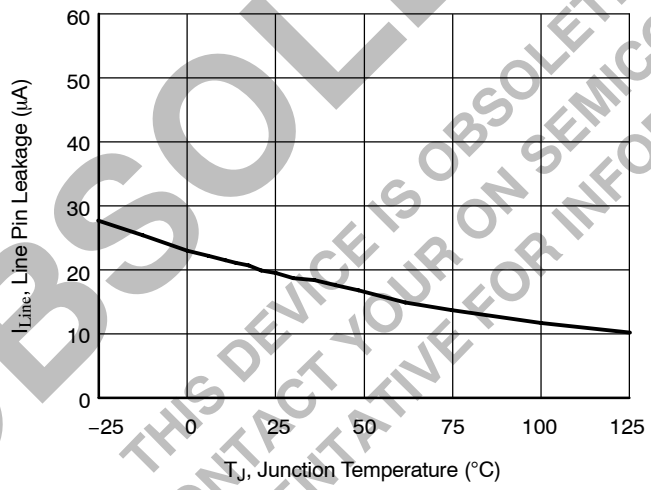


Figure 33. Line Pin Leakage (V_{Line} = 500 V) vs. Junction Temperature

DETAILED OPERATING DESCRIPTION

Introduction

The need of meeting the requirements of legislation on line current harmonic content, results in an increasing demand for cost effective solutions to comply with the Power Factor regulations. This data sheet describes a monolithic controller specially designed for this purpose.

Most off–line appliances use a bridge rectifier associated to a huge bulk capacitor to derive raw DC voltage from the utility AC line.

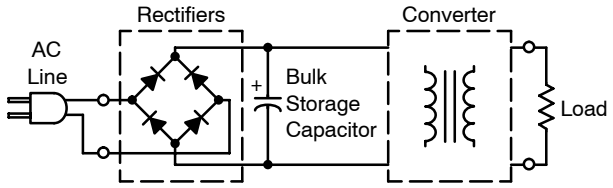


Figure 36. Typical Circuit Without PFC

This technique results in a high harmonic content and in poor power factor ratios. In effect, the simple rectification technique draws power from the mains when the instantaneous AC voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike. Consequently, a poor power factor (in the range of 0.5–0.7) is generated, resulting in an apparent input power that is much higher than the real power.

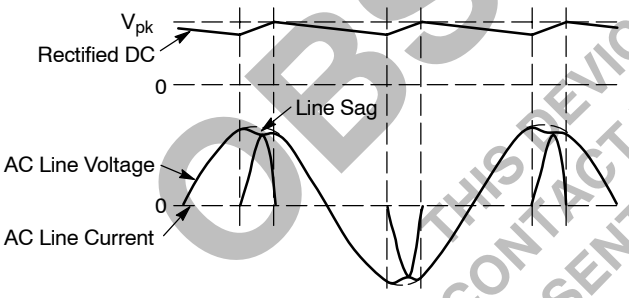


Figure 37. Line Waveforms Without PFC

Active solutions are the most popular way to meet the legislation requirements. They consist of inserting a PFC pre–regulator between the rectifier–bridge and the bulk capacitor. This interface is, in fact, a step–up SMPS that outputs a constant voltage while drawing a sinusoidal current from the line.

The NCP1600 was developed to control an active solution with the goal of increasing its robustness while lowering its global cost.

Operating Description

The NCP1600 is optimized to just as well drive a free running as a synchronized discontinuous voltage mode converter.

It also features valuable protections (overvoltage and undervoltage protection, overcurrent limitation, ...) that make the PFC pre–regulator very safe and reliable while requiring very few external components. In particular, it is able to safely face any uncontrolled direct charges of the output capacitor from the mains which occur when the output voltage is lower than the input voltage (start–up, overload, ...).

In addition to the low count of elements, the circuit can run in an innovative mode named “Follower Boost” that permits significant reduction of the size of the pre–converter inductor and power MOSFET. With this technique, the output regulation level is not forced to a constant value, but can vary according to the AC line amplitude and to the output power. The gap between the output voltage and the AC line is then lowered, allowing for pre–converter inductor and power MOSFET size reduction. Finally, this method brings significant cost reduction. A description of the functional blocks is given below.

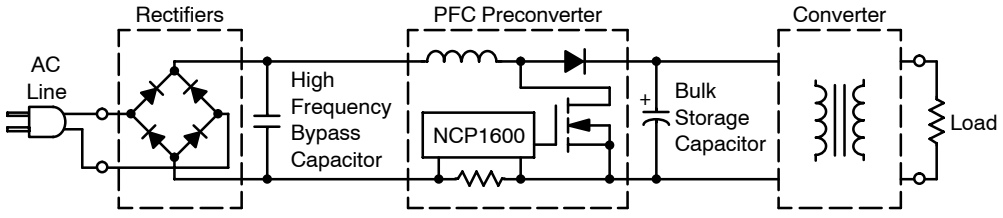


Figure 38. PFC Preconverter

Regulator Section

By connecting a resistor between the output voltage to be regulated and the Pin 4, a feedback current is obtained.

Typically, this current is built by connecting a resistor between the output voltage and the Pin 4. Its value is then given by the following equation:

$$I_{Pin4} = \frac{V_O - V_{Pin4}}{R_O}$$

where:

R_O is the feedback resistor,

V_O is the output voltage,

V_{Pin4} is the Pin 4 clamp value.

The feedback current is compared to the reference current so that the regulation block outputs a signal following the characteristic depicted in Figure 39.

According to the power and the input voltage, the output voltage regulation level varies between two values $(V_O)_{reg-L}$ and $(V_O)_{reg-H}$ corresponding to the I_{reg-L} and I_{reg-H} levels.

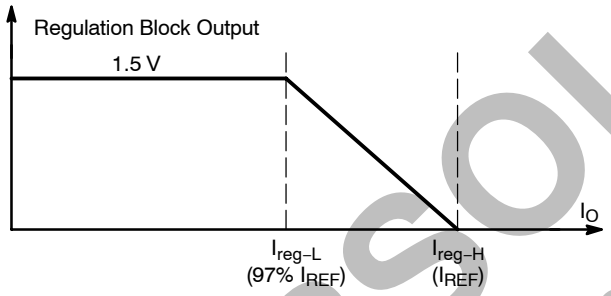


Figure 39. Regulation Characteristic

The feedback resistor must be chosen so that the feedback current should equal the internal current source I_{reg-H} when the output voltage exceeds the chosen upper regulation voltage $[(V_O)_{reg-H}]$. Consequently:

$$R_O = \frac{(V_O)_{reg-H} - V_{Pin4}}{I_{reg-H}}$$

In practice, V_{Pin3} is small compared to $(V_O)_{regH}$ and this equation can be simplified as follows (I_{reg-H} being also replaced by its typical value 200 μA):

$$R_O \approx 5 \times (V_O)_{reg-H} \quad \text{in k}\Omega$$

The regulation block output is connected to the Pin 13 through a 300 kΩ resistor. The Pin 13 voltage ($V_{control}$) is compared to the oscillator saw−tooth for PWM control. An external capacitor must be connected between Pin 13 and ground, for external loop compensation. The bandwidth typically set below 20 Hz so that the regulation block output should be relatively constant over a given AC line cycle. This integration that results in a constant on−time over the AC line period, prevents the mains frequency output ripple from distorting the AC line current.

Oscillator Section

The oscillator consists of three phases:

- Charge Phase: The oscillator capacitor voltage grows up linearly from its bottom value (ground) until it exceeds $V_{control}$ (regulation block output voltage). At that moment, the PWM latch output gets low and the oscillator discharge sequence is set.
- Discharge Phase: The oscillator capacitor is abruptly discharged down to its valley value (0 V).
- Waiting Phase: At the end of the discharge sequence, the oscillator voltage is that maintained in a low state until the PWM latch is set again.

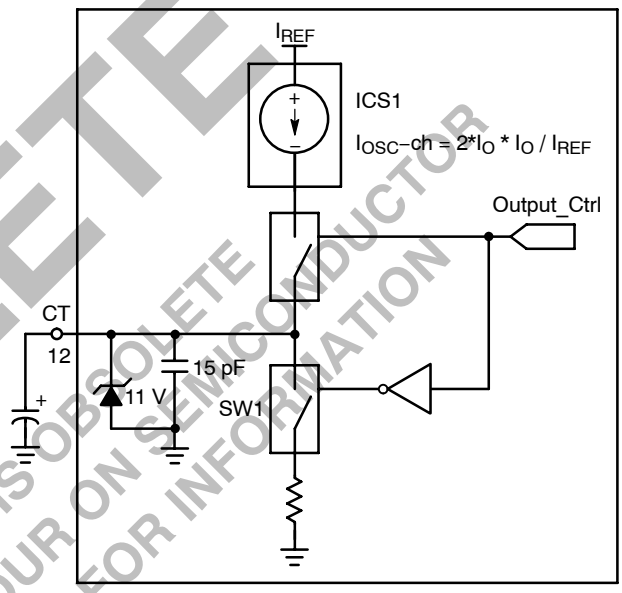


Figure 40. Oscillator

The oscillator charge current is dependent on the feedback current (I_O). In effect:

$$I_{charge} = 2 \times \frac{I_O^2}{I_{REF}}$$

where:

I_{charge} is the oscillator charge current,

I_O is the feedback current (drawn by pin 4),

I_{REF} is the internal reference current (200 μA).

So, the oscillator charge current is linked to the output voltage level as follows:

$$I_{charge} = \frac{2\,(V_O - V_{Pin4})^2}{R_O^2 \times I_{REF}}$$

where:

V_O is the output voltage,

R_O is the feedback resistor,

V_{Pin4} is the Pin 4 Clamp voltage.

In practice, V_{Pin4} that is in the range of 2.5 V, is very small compared to V_O. The equation can then be simplified by neglecting V_{Pin4}:

$$I_{charge} \approx \frac{2 \times V_O^2}{R_O^2 \times I_{REF}}$$

It must be noticed that the oscillator terminal (Pin 12) has an internal capacitance (C_{int}) that varies versus the Pin 12 voltage. Over the oscillator swing, its average value typically equals 15 pF. The total oscillator capacitor is then the sum of the internal and external capacitors.

$$C_{Pin12} = C_T + C_{int}$$

PWM Latch Section

The NCP1600 operates in voltage mode: the regulation block output $V_{control}$ (Pin 13 voltage) is compared to the oscillator saw−tooth so that the gate drive signal (Pin 10) is high until the oscillator ramp exceeds $V_{control}$. The on–time is then given by the following equation:

$$t_{ON} = \frac{C_{Pin12} \times V_{control}}{I_{charge}}$$

where:

t_{ON} is the on–time,

C_{Pin12} is the total oscillator capacitor (sum of the internal and external capacitor),

I_{charge} is the oscillator charge current (Pin 12 current),

$V_{control}$ is the Pin 13 voltage (regulation block output).

Consequently, replacing I_{charge} by the expression given in the **Oscillator Section**:

$$t_{ON} = \frac{R_O^2 \times I_{REF} \times C_{Pin12} \times V_{control}}{2 \times V_O^2}$$

One can notice that the on–time depends on V_O (pre−converter output voltage) and that the on–time is maximum when $V_{control}$ is maximum (1.5 V typically).

At a given Vo, the maximum on–time is then expressed by the following equation:

$$(t_{ON})_{max} = \frac{R_O^2 \times I_{REF} \times C_{Pin12} \times (V_{control})_{max}}{2 \times V_O^2}$$

This equation can be simplified replacing:

$$\frac{2}{I_{ref} \times (V_{control})_{max}} \quad \text{by } K_{osc}$$

Refer to **Electrical Characteristics, Oscillator Section**.

Then:

$$(t_{ON})_{max} = \frac{C_{Pin12} \times R_O^2}{K_{OSC} \times V_O^2}$$

This equation shows that the maximum on–time is inversely proportional to the squared output voltage. This property is used for follower boost operation (refer to **Follower Boost** section).

Current Sense Block

The inductor current is converted into a voltage by inserting a ground referenced resistor (R_{CS}) in series with the input diodes bridge (and the input filtering capacitor). Therefore a negative voltage proportional to the inductor current is built:

$$V_{CS} = -(R_{CS} \times I_L)$$

where:

I_L is the inductor current,

R_{CS} is the current sense resistor,

VCS is the measured R_{CS} voltage.

The negative signal VCS is applied to the current sense through a resistor R_{OCP}. This pin is internally protected by a negative clamp (–0.7 V) that prevents substrate injection.

As long as the Pin 5 voltage is lower than (–60 mV), the Current Sense comparator resets the PWM latch to force the gate drive signal low state. In that condition, the power MOSFET cannot be on.

During the on–time, the Pin 5 information is used for the overcurrent limitation while it serves the zero current detection during the off time.

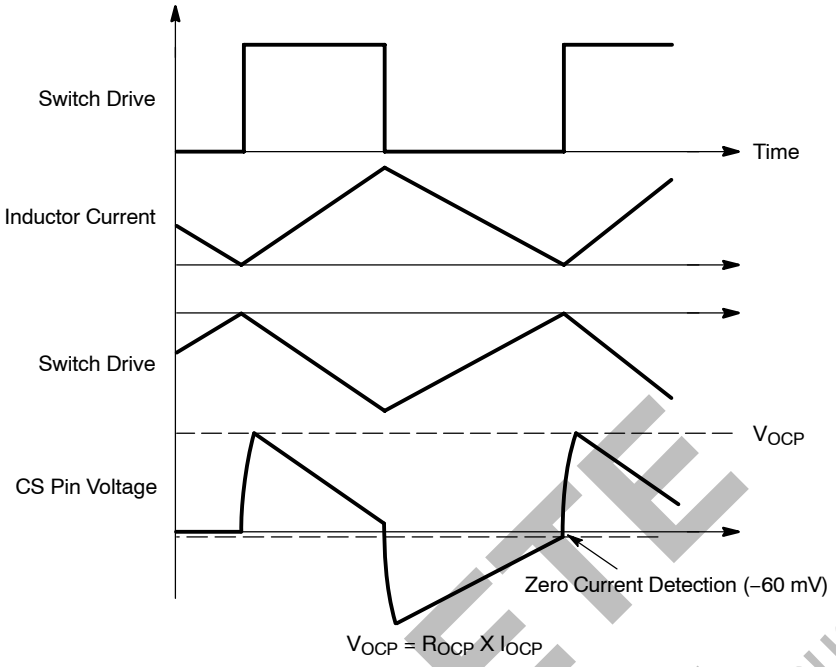


Figure 41. Current Sensing

Zero Current Detection

The Zero Current Detection function guarantees that the MOSFET cannot turn on as long as the inductor current hasn't reached zero (discontinuous mode).

The Pin 5 voltage is simply compared to the (–60 mV) threshold so that as long as VCS is lower than this threshold, the circuit gate drive signal is kept in low state. Consequently, no power MOSFET turn on is possible until the inductor current is measured as smaller than (60 mV/R_{CS}) or, the inductor current nearly equals zero.

OCP (Overcurrent Protection)

During the power switch conduction (i.e. when the Gate Drive pin voltage is high), a current source is applied to Pin 5. A voltage drop V_{OCP} is then generated across the resistor R_{OCP} that is connected between the sense resistor and the Current Sense pin (refer to Figure 42). So, instead of VCS, the sum (VCS + V_{OCP}) is compared to (−60 mV) and the maximum permissible current is the solution of the following equation:

$$-(R_{CS} \times I_{pk(max)}) + V_{OCP} = -60\ mV$$

where:

$I_{pk(max)}$ is the maximum allowed current,

R_{CS} is the sensing resistor.

The overcurrent threshold is then:

$$I_{pk(max)} = \frac{(R_{OCP} \times I_{OCP}) + (60 \times 10^{-3})}{R_{CS}}$$

where:

R_{OCP} is the resistor connected between the pin and the sensing resistor (R_{CS}), I_{OCP} is the current supplied by the Current Sense pin when the gate drive signal is high (power switch conduction phase). I_{OCP} equals 245 μA typically.

Practically, the V_{OCP} offset is high compared to 60 mV and the precedent equation can be simplified. The maximum current is then given by the following equation:

$$I_{pk(max)} \approx \frac{R_{OCP(k\Omega)}}{R_{CS(\Omega)}} \times 0.245\ (mA)$$

Consequently, the R_{OCP} resistor can program the OCP level no matter what the R_{CS} value is. This gives great freedom in the choice of R_{CS}. In particular, R_{CS} can be utilized as the inrush resistor.

A Leading Edge Blanking (LEB) circuit has been implemented. This circuitry disconnects the Current Sense comparator from Pin 5 and disables it during the first 400 ns of the power switch conduction. This prevents the block from reacting on the current spikes that generally occur at power switch turn on. Consequently, proper operation does not require any filtering capacitor on Pin 5.

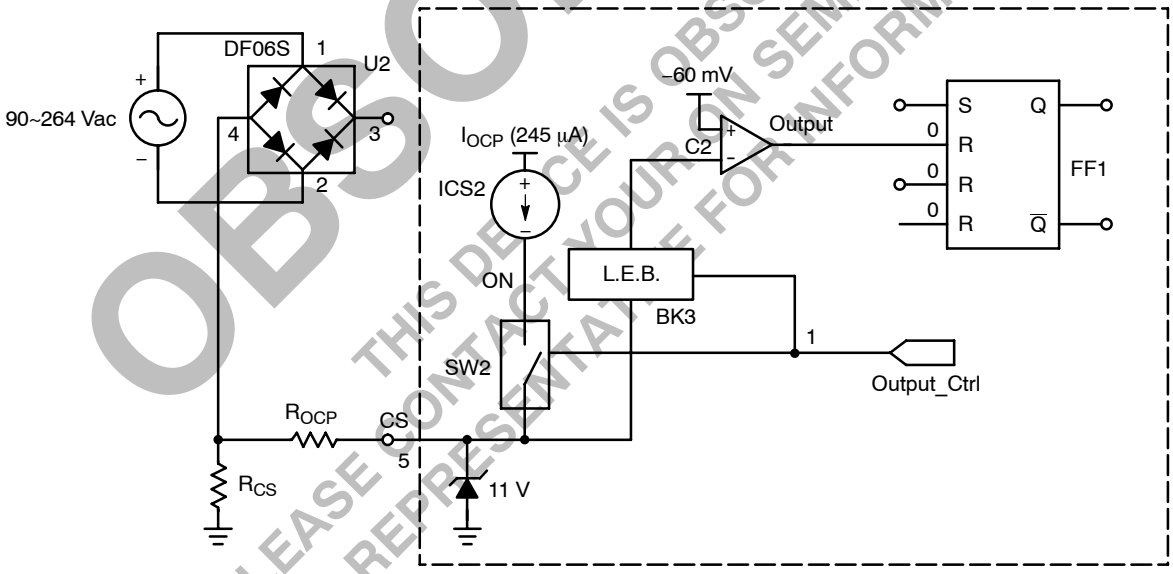


Figure 42. Current Sense Block

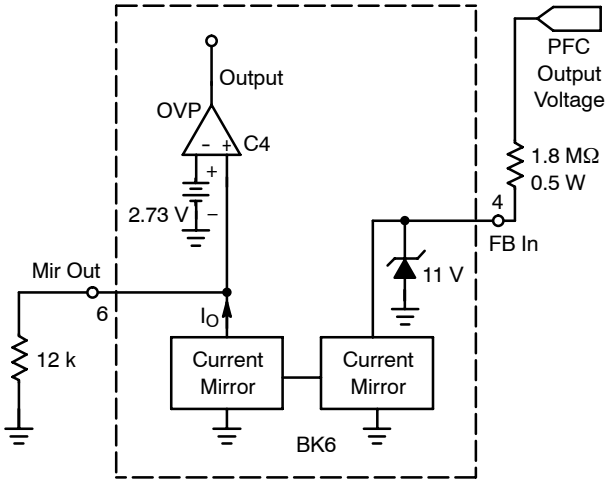


Figure 43. Overvoltage Protection

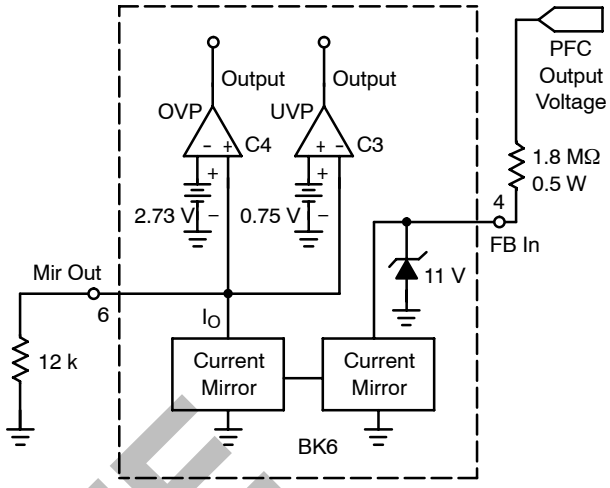


Figure 44. Undervoltage Detection

OVP (Overvoltage Protection)

Referring to Figure 43, Current Mirror output I_O is relating to PFC output voltage. The current I_O flows into the external resistor and a voltage drop developed across Pin 6. This voltage then is compared with the Overvoltage Protection Threshold, V_{C4}, 2.73 V. When the voltage is higher than the V_{C4}, the OVP comparator, C4 will be enabled and the PFC gate drive disabled as a result to keep the bulk capacitor voltage below the set level. By selecting the value of the external resistor, the OVP voltage can then be determined. With this feature, the maximum bulk capacitor voltage can be set to value below 400 V so that lower cost bulk capacitor can be used.

Undervoltage Protection and Feedback Loop Open Detection

Referring to Figure 44, similarly, the PFC function will be bypassed until the Pin 6 voltage exceed 0.75 V. This feature is used to avoid the PFC drawing high current while the line voltage fall below a reasonable level in order to protect the power elements. This protection feature is also applicable for Feedback Loop Open Detection. While the feedback resistor is open, no current flows into the FB_In pin (Pin 4), hence the voltage across Pin 6 will be diminished and the protection will be activated.

Switching Frequency Clamp

Refer to Figure 45, the Switching Frequency Clamp. The frequency clamp function can be disabled by pulling the FC pin voltage higher than frequency clamp threshold. While the frequency clamp function is disabled, the PFC gate drive turn−on depends on zero−current−detection of CS pin.

By connecting the RC to the frequency clamp pin, the PFC gate drive turn−on depends on both the FC pin voltage and the CS pin's zero−current−detection. When the FC pin voltage reaches its threshold, the PFC gate drive turn−on by the zero−current−detection of the CS pin.

For best results, the minimum off−time, determined by the values of R and C on the FC pin, should be chosen so that $t_{s(min)} = t_{ON} + t_{OFF(FC)}$. The output drive is inhibited when the voltage at the frequency clamp input is less than 2.0 V. When the output drive is high, C is discharged through an internal 100 μA current source. When the output drive switches low, C7 is charged through R_{FC}. The drive output is inhibited until the voltage across C_{FC} reaches 2.0 V, establishing a minimum off−time where:

$$t_{OFF} = -(R_{FC})(C_{FC}) \log_{ln}\left[1 - \frac{2}{V_{REF}}\right]$$

Output Section

The output stage contains a totem pole optimized to minimize the cross conduction current during high speed operation. The gate drive is kept in a sinking mode whenever the Undervoltage Lockout is active. The rise and fall times have been controlled to typically equal 14 ns while loaded by 1.0 nF.

Reference Section

An internal reference current source (I_{REF}) is trimmed to be ±5% accurate over the temperature range (the typical value is 200 μA). I_{REF} is the reference used for the regulation. An internal reference voltage (V_{REF}) is trimmed to be ±3.85% accurate over the temperature range (the typical value is 6.5 V).

Thermal Shutdown

Internal thermal, circuitry sensing is provided to disable the circuit gate drive and then to prevent it from oscillating, if the junction temperature exceeds 160°C typically. The output stage is again enabled when the temperature drops below 124°C typically (36°C hysteresis).

Follower Boost Operation

Traditional PFC pre−converters provide the load with a regulated voltage that generally equals 400 V or can change according to the mains type (U.S., European, or universal). In the "Follower Boost" operation, the pre−converter output regulation level is not fixed but varies linearly versus the AC line amplitude at a given input power.

This technique aims at reducing the gap between the output and the input voltages to minimize the boost efficiency degradation.

Follower Boost Benefits

The boost presents two phases:

- The on–time during which the power switch is on. The inductor current grows up linearly according to a slope (V_{IN}/L_p), where V_{IN} is the instantaneous input voltage and L_p the inductor value.
- The off–time during which the power switch is off. The inductor current decreases linearly according to the slope ($V_O - V_{IN})/L_p$, where O_o is the output voltage. This sequence that terminates when the current equals zero has a duration that is inversely proportional to the gap between the output and input voltages. Consequently, the off–time duration becomes longer in follower boost.

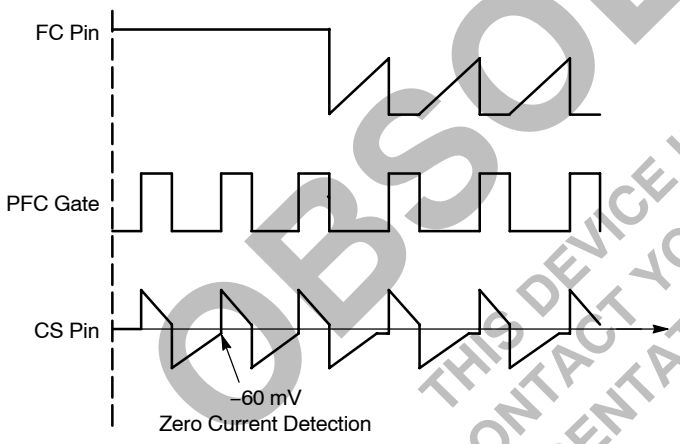


Figure 45. Switch Frequency Clamp

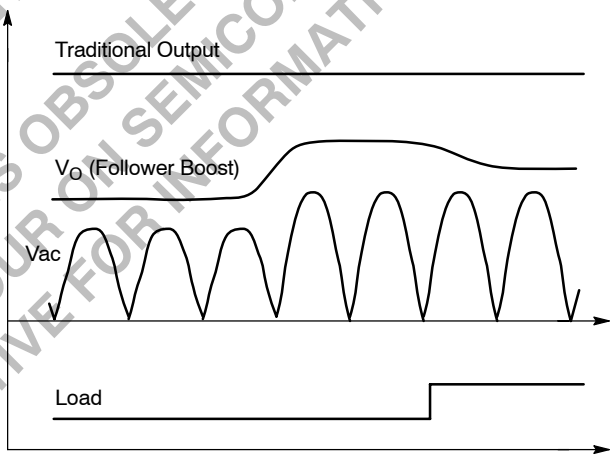


Figure 46. Follower Boost Characteristics

Consequently, for a given peak inductor current, the longer the off−time, the smaller power switch duty cycle and then its conduction dissipation. This is the first benefit of this technique: the MOSFET on–time losses are reduced.

The increase of the off−time duration also results in a switching frequency reduction (for a given inductor value). Given that, in practice, the boost inductor is selected to be big enough to limit the switching frequency down to an acceptable level, one can immediately see the second benefit of the follower boost: it allows the use of smaller, lighter and cheaper inductors compared to traditional systems. Finally, this technique utilization brings a drastic system cost reduction by lowering the cost of both the inductor and the power switch.

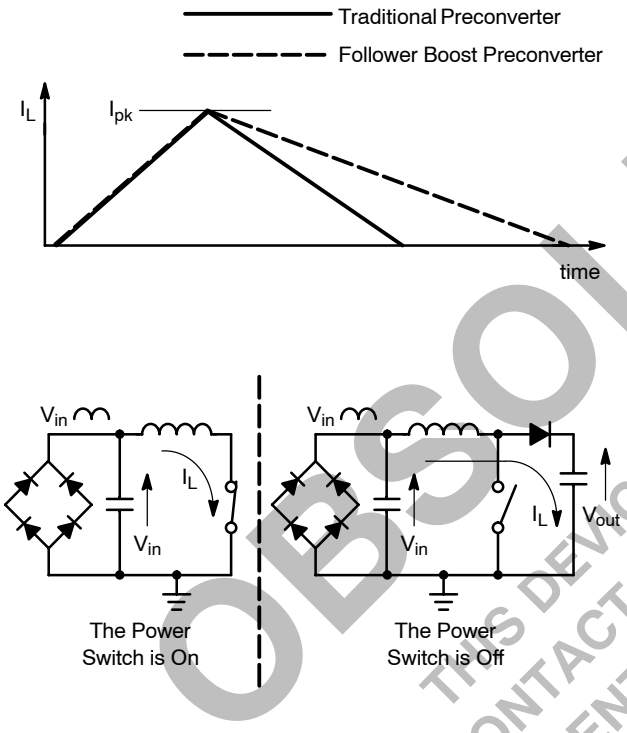


Figure 47. Off−Time Duration Increase

Follower Boost Implementation

In the NCP1600, the on–time is controlled differently according to the feedback current level. Two areas can be defined:

- When the feedback current is higher than I_{reg-L} (refer to regulation section), the regulation block output ($V_{control}$) is modulated to force the output voltage to a desired value.
- On the other hand, when the feedback current is lower than I_{reg-L}, the regulation block output and therefore, the on–time, are maximum. As explained in the **PWM Latch Section,** the on–time is then inversely proportional to the output voltage square. The Follower Boost is active in these conditions in which the on–time is simply limited by the output voltage level. Note: In this equation, the feedback pin voltage (V_{Pin1}) is neglected compared to the output voltage (refer to the **PWM Latch Section**).

$$t_{ON} = (t_{ON})_{max} = \frac{C_{Pin12} \times R_O^2}{K_{OSC} \times V_O^2}$$

where:
C_{Pin12} is the total oscillator capacitor (sum of the internal and external capacitors – $C_{int} + C_T$),
K_{OSC} is the ratio (oscillator swing over oscillator gain),
V_O is the output voltage,
R_O is the feedback resistor.

On the other hand, the boost topology has its own rule that dictates the on–time necessary to deliver the required power:

$$t_{ON} = \frac{4 \times L_p \times P_{IN}}{V_{pk}^2}$$

where:
V_{pk} is the peak AC line voltage,
L_p is the inductor value,
P_{IN} is the input power.

Combining the two equations, one can obtain the Follower Boost equation:

$$V_O = \left(\frac{R_O}{2}\right)\sqrt{\frac{C_{Pin12}}{K_{OSC} \times L_p \times P_{IN}}} \times V_{pk}$$

Consequently, a linear dependency links the output voltage to the AC line amplitude at a given input power.

The behavior of the output voltage is depicted in Figures 48 and 49. In particular, Figure 48 illustrates how the output voltage converges to a stable equilibrium level. First, at a given AC line voltage, the on–time is dictated by the power demand. Then, the follower boost characteristic makes correspond one output voltage level to this on–time.

Combining these two laws, it appears that the power level forces the output voltage.

One can notice that the system is fully stable:

- If an output voltage increase makes it move away from its equilibrium value, the on–time will immediately diminish according to the follower boost law. This will result in a delivered power decrease. Consequently, the supplied power being too low, the output voltage will decrease back.
- In the same way, if the output voltage decreases, more power will be transferred and then the output voltage will increase back.

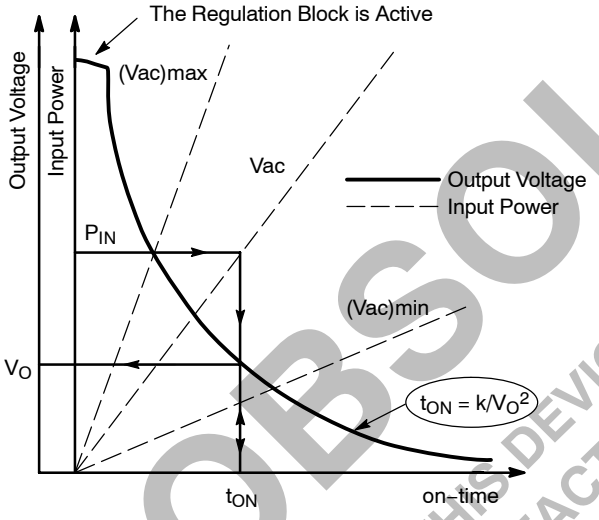


Figure 48. Follower Boost Characteristics

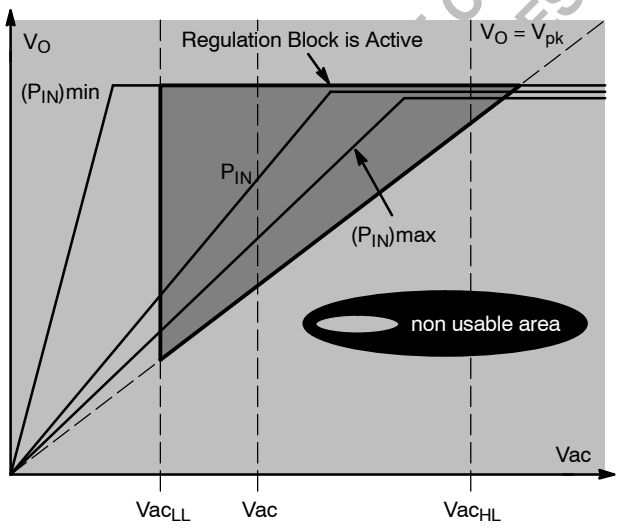


Figure 49. Follower Boost Output Voltage

Mode Selection

The operation mode is simply selected by adjusting the oscillator capacitor value. As shown in Figure 49, the output voltage first has an increasing linear characteristic versus the AC line magnitude and then is clamped down to the regulation value. In the traditional mode, the linear area must be rejected. This is achieved by dimensioning the oscillator capacitor so that the boost can deliver the maximum power while the output voltage equals its regulation level and this, whatever the given input voltage.

Practically, that means that whatever the power and input voltage conditions are, the follower boost would generate output voltages values higher than the regulation level, if there was no regulation block.

In other words, if $(V_O)_{reg-L}$ is the low output regulation level:

$$(V_O)_{reg-L} \leq \frac{R_O}{2} \times \sqrt{\frac{C_T + C_{IN}}{K_{OSC} \times L_p \times (P_{IN})_{max}}} V_{pk}$$

Consequently,

$$C_T \geq -C_{int} + \frac{4 \times K_{OSC} \times L_p \times (P_{IN})_{max} \times (V_O)_{-reg-L}^2}{R_O^2 \times V_{pk}^2}$$

Using I_{reg-L} (regulation block current reference), this equation can be simplified as follows:

$$C_T \geq -C_{int} + \frac{4 \times K_{OSC} \times L_p \times (P_{IN})^2}{V_{pk}^2}$$

In the Follower Boost case, the oscillator capacitor must be chosen so that the desired characteristics are obtained.

Consequently, the simple choice of the oscillator capacitor enables the mode selection.

Standby Operation

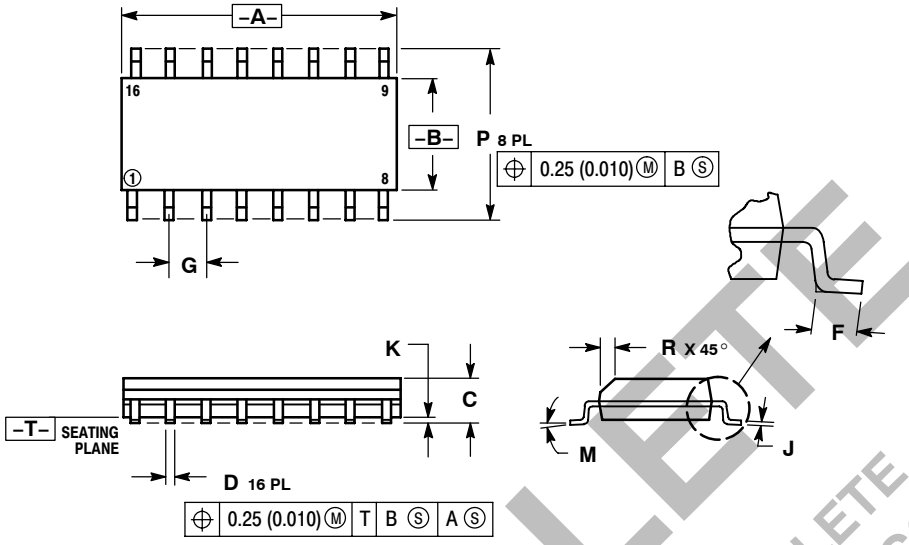
The PFC boost pre–converter entering standby mode depends on the STB (Standby) pin voltage (Pin 8 voltage) which is a high impedance input, and can be directly connected to PWM section's Opto–coupler output to derive PWM output load information. PFC boost pre–converter will enter Standby mode when the voltage at this pin falls below 1.17 V.

While the output of C7 is low, the PFC will stay in normal operation and the AND1 gate output will stay low for all the time. When the STB pin voltage falls below the threshold, 1.17 V, the output of C7 will go high and the output of the AND1 gate will depend on the output of C6. The current flowing from the current on Pin 4 is equal to the FB–In pin (Pin 4) current which is derived from the Bulk Capacitor voltage at the output. The PFC pre–converter will be disabled when the voltage at Pin 6 is higher than the voltage at Pin 7. The minimum PFC output voltage can be set by the Pin 7 voltage during standby mode. This voltage can be derived from the V_{REF} (Pin 2) by a voltage divider network.

During standby operation, the PFC boost pre–converter will enter skip mode when AC input voltage falls below this pre–set value. The minimum PFC output voltage and PFC boost pre–converter will enter off mode when AC input voltage higher than the pre–set minimum PFC output voltage.

PACKAGE DIMENSIONS

SO−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

The products described herein (NCP1600), may be covered by one or more of the following U.S. patents: 5,073,850; 5,862,045; 6,177,782. There may be more patents pending.
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