NCP1377, NCP1377B

PWM Current-Mode Controller for Free-Running Quasi-Resonant Operation

The NCP1377 combines a true current mode modulator and a demagnetization detector which ensures full borderline/critical Conduction Mode in any load/line conditions together with minimum drain voltage switching (Quasi−Resonant operation). Due to its inherent skip cycle capability, the controller enters burst mode as soon as the power demand falls below a predetermined level. As this happens at low peak current, no audible noise can be heard. For NCP1377, an internal 8.0 μs timer prevents the free−run frequency to exceed 100 kHz (therefore below the 150 kHz CISPR−22 EMI starting limit), while the skip adjustment capability lets the user select the frequency at which the burst foldback takes place. For NC1377B, the internal timer duration is reduced to 3.0 μs to allow operation at higher frequencies (up to 300 kHz).

The transformer core reset detection is done through an auxiliary winding which, brought via a dedicated pin, also enables fast Over Voltage Protection (OVP). Once an OVP has been detected, the IC permanently latches off. The 1377 features a sampling time of 4.5 μs whereas it is 1.5 μs for the B version.

The NCP1377 also features an efficient protective circuitries which, in presence of an overcurrent condition, disables the output pulses and enters a safe burst mode, trying to restart. Once the default has gone, the device auto−recovers. Finally an internal 1.0 ms Soft−Start eliminates the traditional startup stress.

Features

- Pb−Free Package is Available
- Free−Running Borderline/Critical Mode Quasi−Resonant Operation
- Latched Overvoltage Protection
- Auto−Recovery Short−Circuit Protection Via UVLO Crossover
- External Latch Triggering, e.g. Via Overtemperature Signal
- Current−Mode with Adjustable Skip Cycle Capability
- Internal 1.0 ms Soft−Start
- Internal Temperature Shutdown
- Internal Leading Edge Blanking
- 500 mA Peak Current Source/Sink Capability
- Under Voltage Lockout Level of 12.5 V (On) and 7.5 V (Min)
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient Analysis
- Internal Minimum T_{OFF}

Typical Applications

- AC−DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Consumer Electronics (DVD Players, Set−Top Boxes, TVs, etc.)
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

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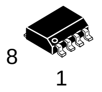
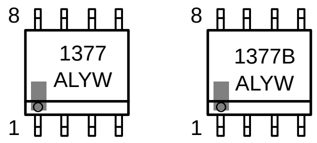
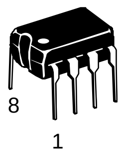
MARKING DIAGRAMS

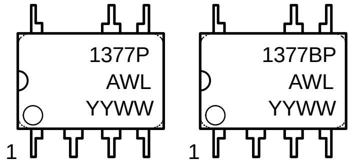
SOIC−8
D SUFFIX
CASE 751





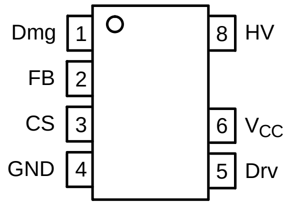
PDIP−7
P SUFFIX
CASE 626B





A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



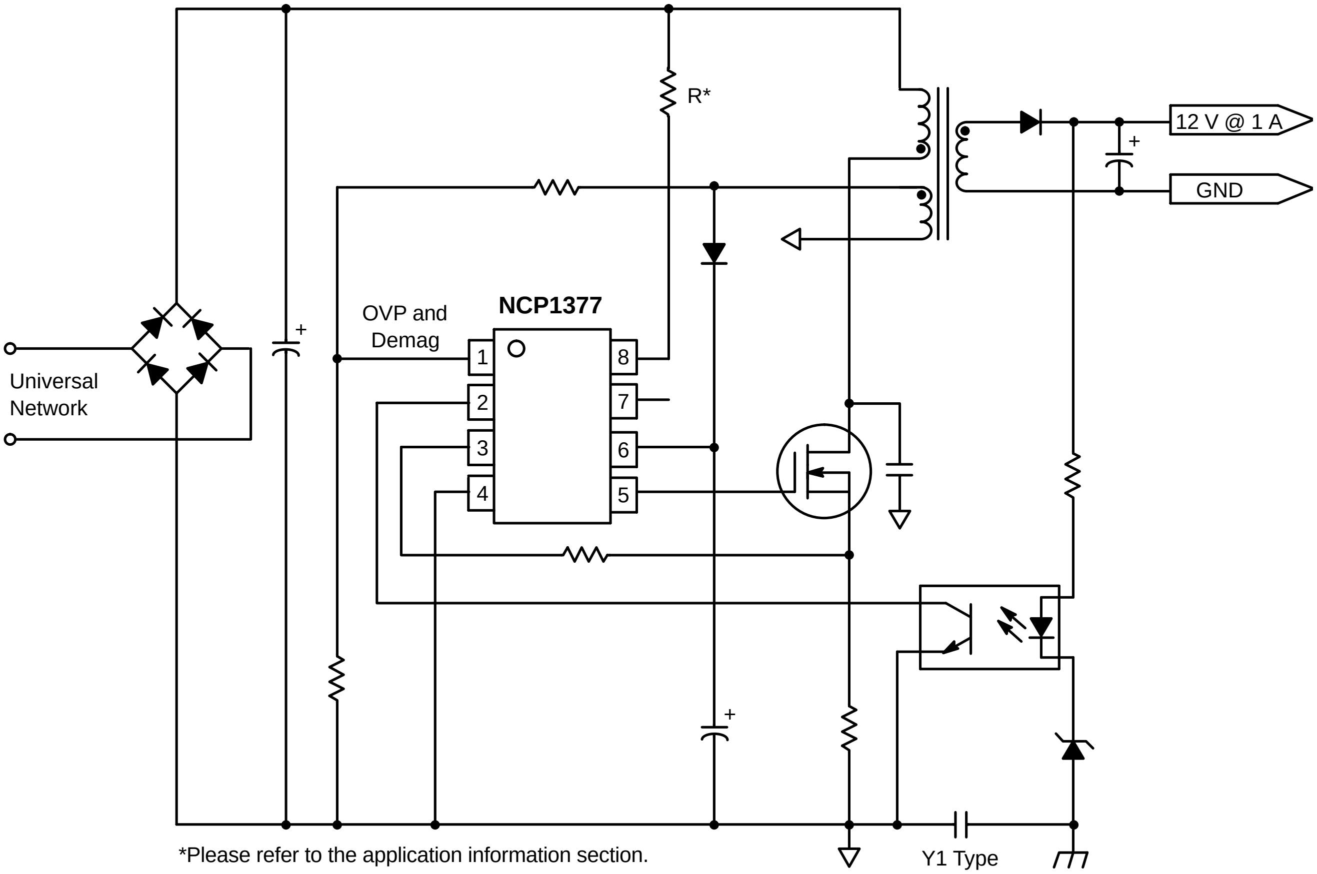
(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1377DR2	SOIC−8	2500 Tape & Reel
NCP1377DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
NCP1377BDR2	SOIC−8	2500 Tape & Reel
NCP1377P	PDIP−7	50 Units/Tube
NCP1377BP	PDIP−7	50 Units/Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

October, 2004 − Rev. 1



*Please refer to the application information section.

Figure 1. Typical Application Schematic

PIN FUNCTION DESCRIPTION

Pin	Symbol	Function	Description
1	Demag	Core reset detection and OVP	The auxiliary FLYBACK signal ensures discontinuous operation and offers a fixed overvoltage detection level of 7.2 V.
2	FB	Sets the peak current setpoint	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand. By bringing this pin below the internal skip level, you shut off the device.
3	CS	Current sense input and skip cycle level selection	This pin senses the primary current and routes it to the internal comparator via an L.E.B. By inserting a resistor in series with the pin, you control the level at which the skip operation takes place.
4	GND	The IC ground	−
5	Drv	Driving pulses	The driver’s output to an external MOSFET.
6	V_{CC}	Supplies the IC	This pin is connected to an external bulk capacitor of typically 10 μF.
7	NC	−	This unconnected pin ensures adequate creepage distance.
8	HV	High−voltage pin	Connected to the high−voltage rail, this pin injects a constant current into the V_{CC} bulk capacitor and ensures a clean lossless startup sequence.

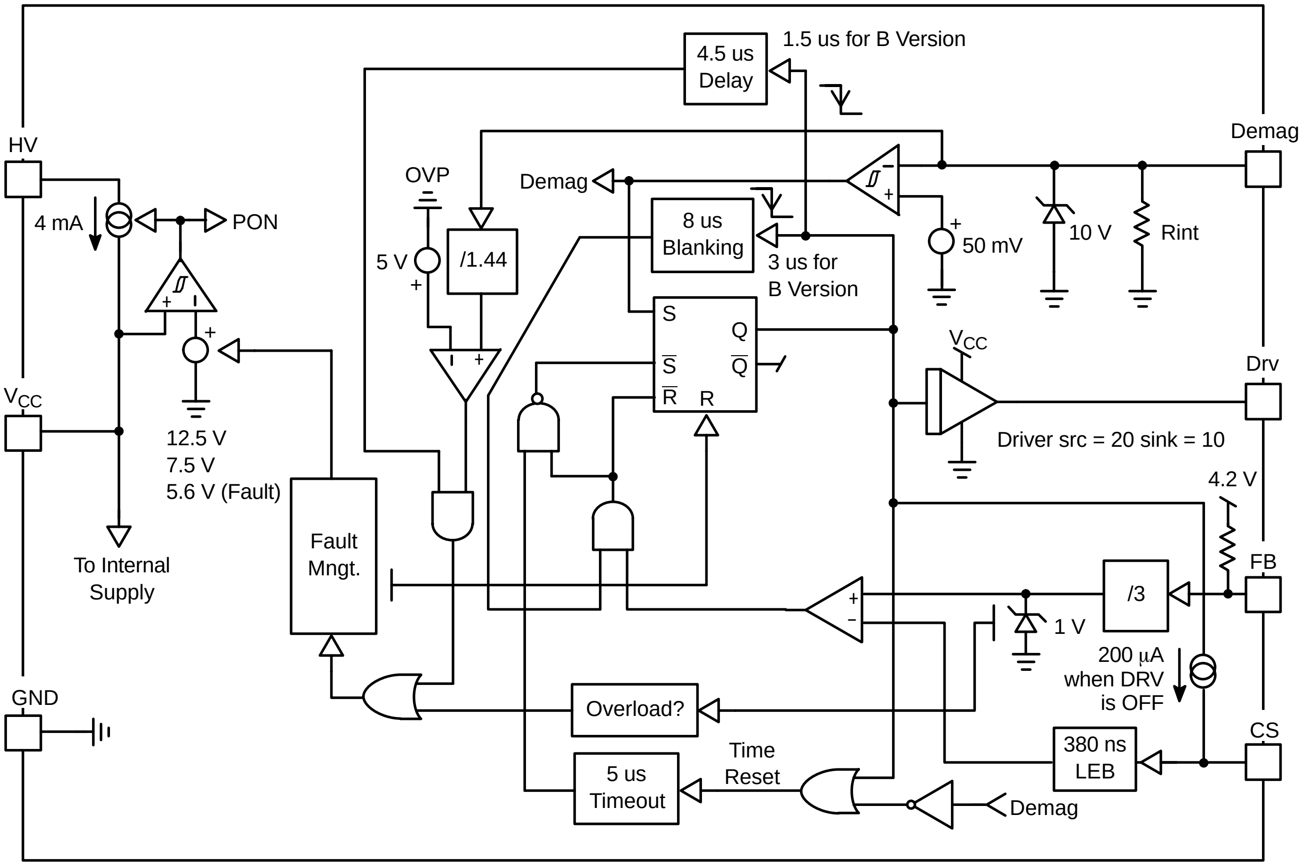


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, Drv	16	V
Maximum Voltage on all other pins except Pin 8 (HV), Pin 6 (V_{CC}) and Pin 5 (Drv)	−	−0.3 to 10	V
Maximum Current into all pins except V_{CC} (6), HV (8) and Demag (1) when 10 V ESD diodes are activated	−	5.0	mA
Maximum Current in Pin 1	Idem	+3.0/−2.0	mA
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	57	°C/W
Thermal Resistance, Junction−to−Air, SOIC Version	$R_{\theta JA}$	178	°C/W
Thermal Resistance, Junction−to−Air, PDIP Version	$R_{\theta JA}$	100	°C/W
Maximum Junction Temperature	TJ_{MAX}	150	°C
Temperature Shutdown	−	155	°C
Hysteresis in Shutdown	−	30	°C
Storage Temperature Range	−	−60 to +150	°C
ESD Capability, HBM Model (All pins except V_{CC} and HV)	−	2.0	kV
ESD Capability, Machine Model	−	200	V
Maximum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) Decoupled to Ground with 10 µF	V_{HV}	500	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (For typical values T_j = 25°C, for min/max values T_j = 0°C to +125°C, Max T_j = 150°C, V_{CC} = 11 V unless otherwise noted.)

Characteristic		Pin	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION							
V_{CC} Increasing Level at which the Current Source Turns−Off		6	VCC_{ON}	11.6	12.5	13.7	V
V_{CC} Decreasing Level at which the Current Source Turns−On		6	VCC_{min}	7.0	7.5	8.2	V
V_{CC} Decreasing Level at which the Latchoff Phase Ends		6	VCC_{latch}	−	5.6	−	V
Internal IC Consumption, No Output Load on Pin 5, F_{SW} = 60 kHz		6	ICC1	−	1.0	1.3 (Note 1)	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 60 kHz		6	ICC2	−	1.6	2.0 (Note 1)	mA
Internal IC Consumption, Latchoff Phase, V_{CC} = 6.0 V		6	ICC3	−	220	−	μA
INTERNAL STARTUP CURRENT SOURCE (Vpin 8 = 40 V)							
High−Voltage Current Source, V_{CC} = 10 V		8	IC1	2.4	4.0	6.0	mA
High−Voltage Current Source, V_{CC} = 0		8	IC2	−	4.5	−	mA
DRIVE OUTPUT							
Output Voltage Rise−Time @ CL = 1.0 nF, 10−90% of Output Signal		5	T_r	−	40	−	ns
Output Voltage Fall−Time @ CL = 1.0 nF, 10−90% of Output Signal		5	T_f	−	20	−	ns
Source Resistance		5	R_{OH}	12	20	36	Ω
Sink Resistance		5	R_{OL}	5.0	10	19	Ω
CURRENT COMPARATOR							
Input Bias Current @ 1.0 V Input Level on Pin 3		3	I_{IB}	−	0.02	−	μA
Maximum Internal Current Setpoint		3	I_{Limit}	0.9	1.0	1.1	V
Propagation Delay from Current Detection to Gate OFF State		3	T_{DEL}	−	100	160	ns
Leading Edge Blanking Duration		3	T_{LEB}	−	380	−	ns
Internal Current Offset Injected on the CS Pin During OFF Time		3	Iskip	−	200	−	μA
OVERVOLTAGE SECTION							
Sampling Delay After ON Time	NCP1377 NCP1377B	1 1	T_{sample}	− −	4.5 1.5	− −	μs
OVP Internal Reference Level		1	V_{ref}	6.4	7.2	8.0	V
FEEDBACK SECTION							
Internal Pullup Resistor		2	Rup	−	20	−	kΩ
Pin 3 to Current Setpoint Division Ratio		−	Iratio	−	3.3	−	−
Internal Soft−Start		−	Tss	−	1.0	−	ms
DEMAGNETIZATION DETECTION BLOCK							
Input Threshold Voltage (Vpin 1 Decreasing)		1	V_{th}	35	50	90	mV
Hysteresis (Vpin 1 Decreasing)		1	V_H	−	20	−	mV
Input Clamp Voltage							V
High State (Ipin 1 = 3.0 mA)		1	VC_H	8.0	10	12	
Low State (Ipin 1 = −2.0 mA)		1	VC_L	−0.9	−0.7	−0.5	
Pin1 Internal Resistance		1	R_{int}	−	28	−	kΩ
Demag Propagation Delay		1	T_{dem}	−	210	−	ns
Timeout After Last Demag Transition		1	Tout	−	5.0	−	μs
Internal Input Capacitance at Vpin 1 = 1.0 V		1	C_{par}	−	10	−	pF
Minimum T_{OFF} (Internal Blanking Delay After T_{ON})	NCP1377 NCP1377B	1 1	T_{blank}	− −	8.0 3.0	− −	μs

1. Max value at T_j = 0°C, please see characterization curves.

TYPICAL CHARACTERISTICS

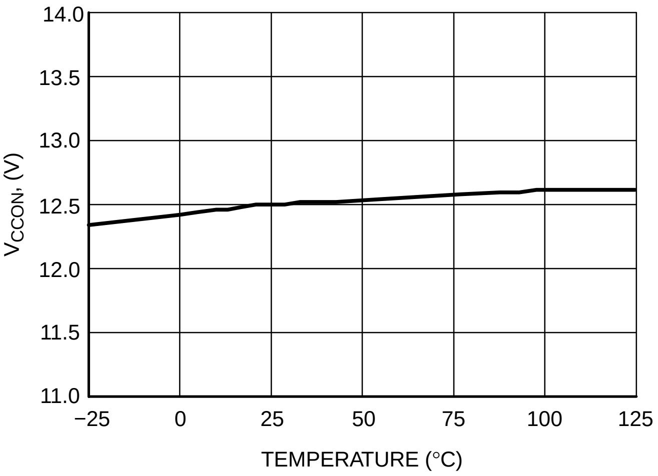


Figure 3. V_{CCON} Threshold versus Temperature

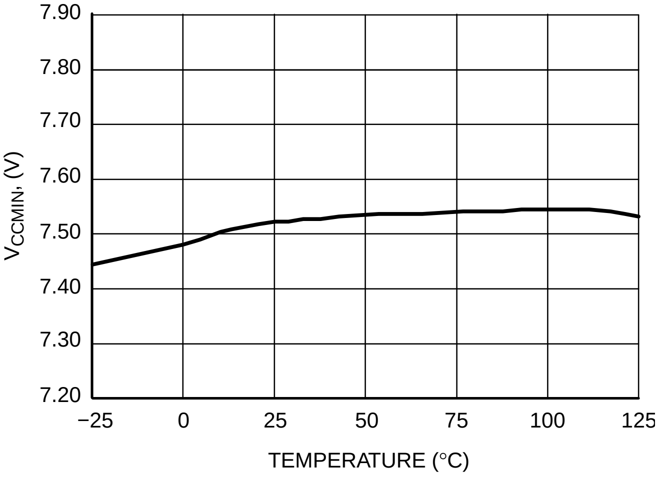


Figure 4. V_{CCMIN} Threshold versus Temperature

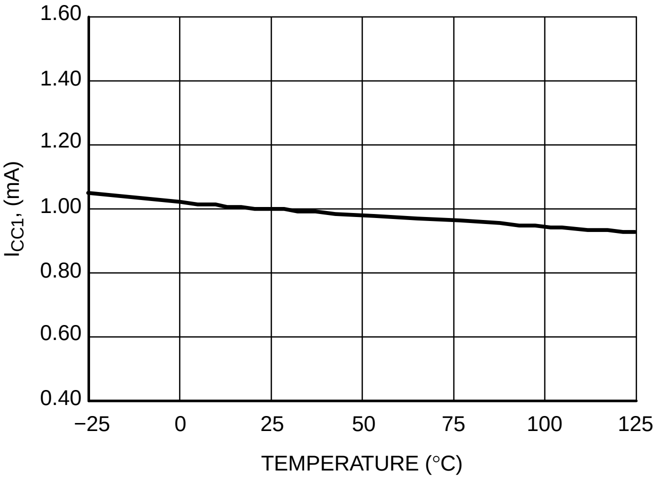


Figure 5. Current Consumption (No Load) versus Temperature

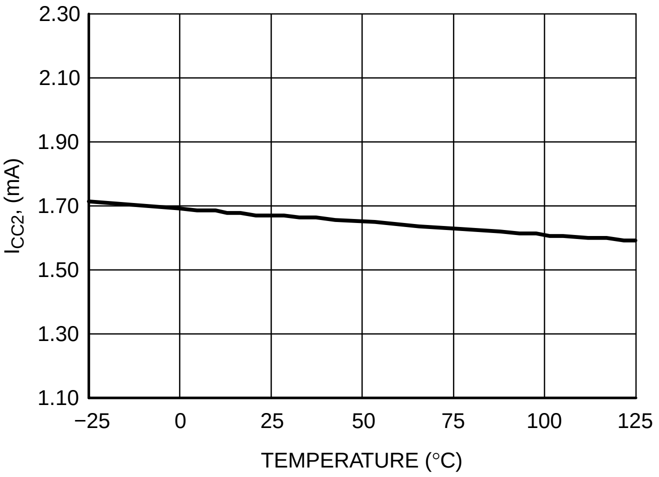


Figure 6. Current Consumption (1.0 nF Load) versus Temperature

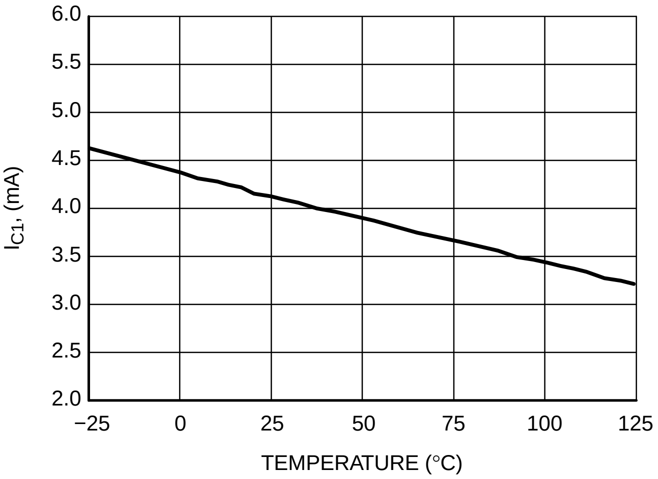


Figure 7. HV Current Source at V_{CC} = 10 V versus temperature

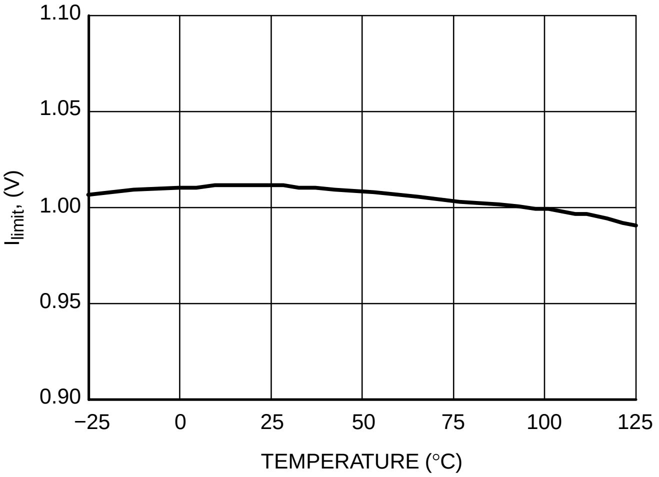


Figure 8. Maximum Current Setpoint versus Temperature

TYPICAL CHARACTERISTICS

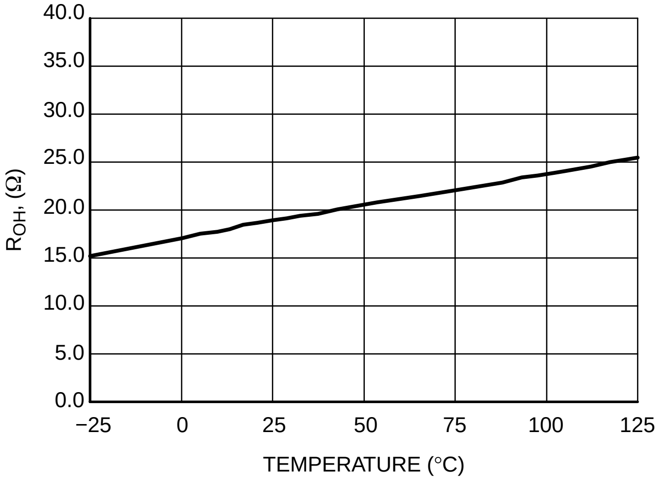


Figure 9. Drive Source Resistance versus Temperature

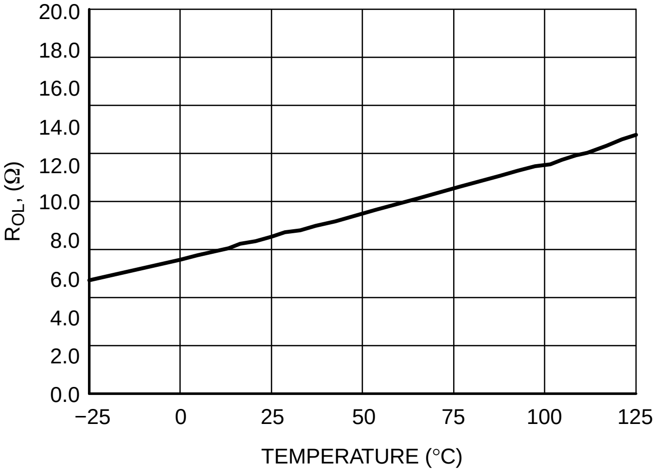


Figure 10. Drive Sink Resistance versus Temperature

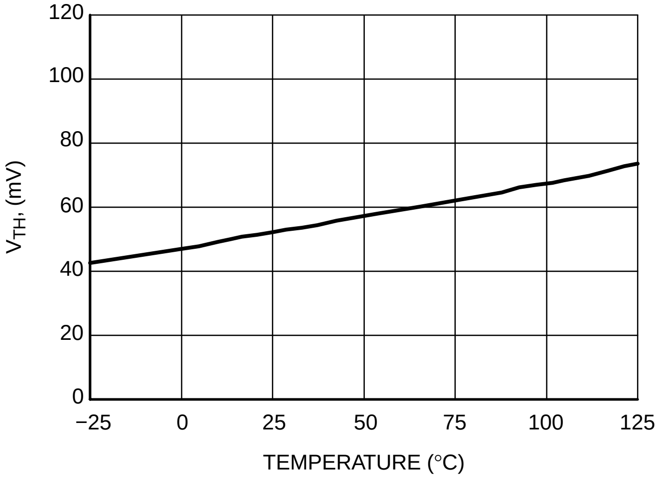


Figure 11. Demagnetization Detection Threshold versus Temperature

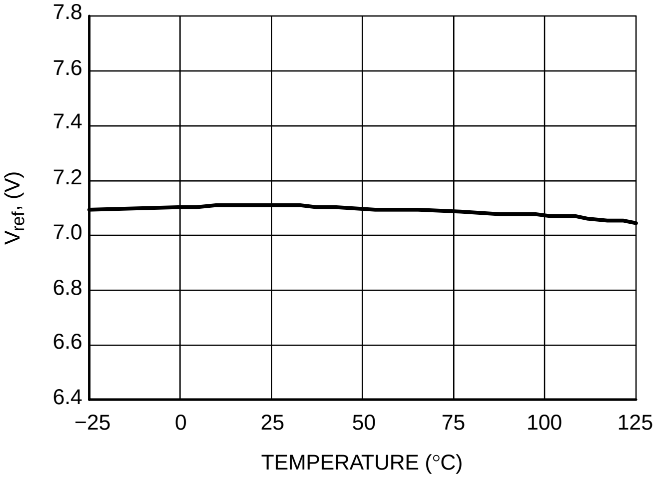


Figure 12. OVP Threshold versus Temperature

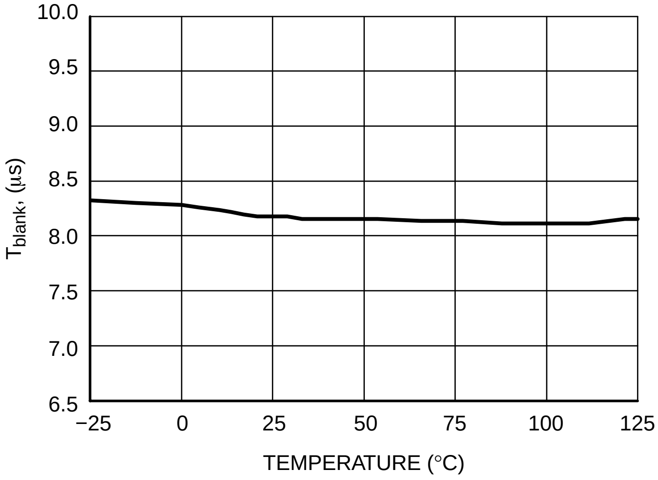


Figure 13. Minimum T_{OFF} versus Temperature

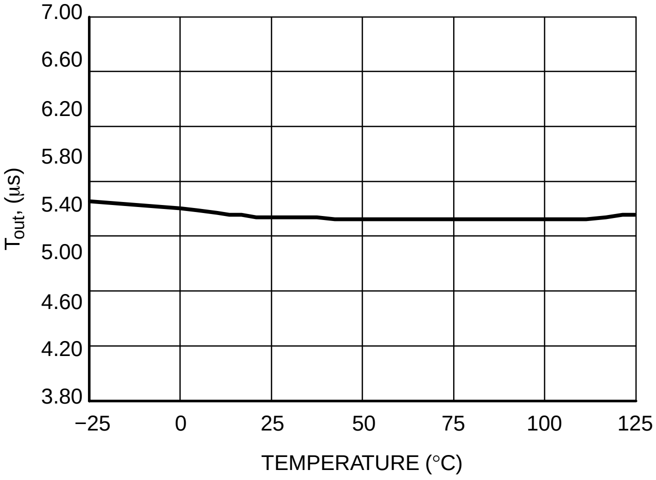


Figure 14. Demagnetization Detection Timeout versus Temperature

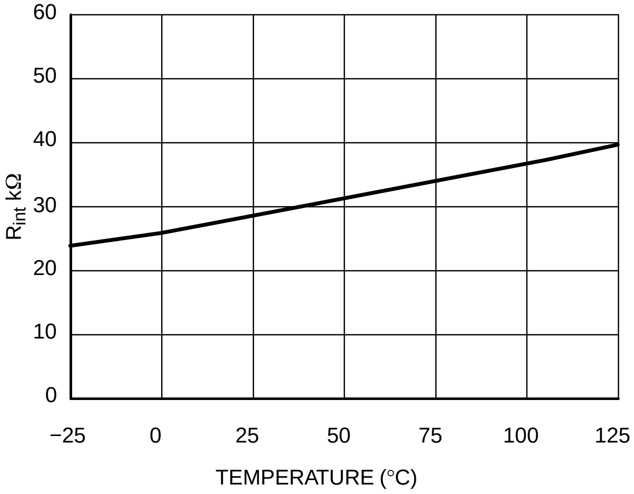


Figure 15. DMG Pin Internal Resistance versus Temperature

APPLICATION INFORMATION

INTRODUCTION

The NCP1377 implements a standard current mode architecture where the switch−off time is dictated by the peak current setpoint, whereas the core reset detection triggers the turn−on event. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost AC−DC adapters, consumer electronics, auxiliary supplies, etc. Due to its high−performance high−voltage technology, the NCP1377 incorporates all the necessary components/features needed to build a rugged and reliable Switchmode Power Supply (SMPS):

- *Transformer Core Reset Detection:* Borderline/critical operation is ensured whatever the operating conditions are. As a result, there are virtually no primary switch turn−on losses and no secondary diode recovery losses. The converter also stays a first−order system and accordingly eases the feedback loop design.
- *Quasi−Resonant Operation:* By delaying the turn−on event, it is possible to restart the MOSFET in the minimum of the drain−source wave, ensuring reduced EMI/video noise perturbations. In nominal power conditions, the NCP1377 operates in Borderline Conduction Mode (BCM) also called Critical Conduction Mode.
- *Undervoltage Lockout (UVLO):* When Vcc falls below Vcc_{min} pulses are stopped and the IC consumption drops down to a few hundred of µA. When Vcc reaches the latchoff level (5.6 V typical), the startup current source is activated and brings Vcc back to Vcc_{on} where the IC attempts to startup.
- *Overvoltage Protection (OVP):* By sampling the plateau voltage on the demagnetization winding, the NCP1377 goes into latched fault condition whenever an overvoltage condition is detected. The controller stays fully latched in this position until the Vcc is cycled down to 4.0 V, e.g. when the user unplugs the power supply from the mains outlet and replugs it.
- *External Latch Trip Point:* By externally forcing a level on the OVP greater than the internal setpoint, it is possible to latchoff the IC, e.g. with a signal coming from a temperature sensor.
- *Adjustable Skip Cycle Level:* By offering the ability to tailor the level at which the skip cycle takes place, the designer can make sure that the skip operation only occurs at low peak current. This point guarantees a noise−free operation with cheap transformer. This option also offers the ability to fix the maximum switching frequency when entering light load conditions.
- *Overcurrent Protection (OCP):* NCP1377 enters burst mode as soon as the power supply undergoes an overload which is detected through the sense of the auxiliary voltage. As detailed above, as soon as Vcc crosses the undervoltage lockout level (Vcc_{min} in the electrical table), all pulses are stopped and the device enters a safe low power operation which prevents from any lethal thermal runaway. By monitoring the Vcc level, the startup current source is activated ON and OFF to create a kind of burst mode where the SMPS tries to restart. If the fault has gone, the SMPS resumes operation. On the other hand, if the fault is still there, the burst sequence starts again.

Startup Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 4.0 mA) is biased and charges up the Vcc capacitor. When the voltage on this Vcc capacitor reaches the Vcc_{ON} level (typically 12.5 V), the current source turns off and no longer wastes any power. At this time, the Vcc capacitor only supplies the controller and the auxiliary supply is supposed to take over before Vcc collapses below Vcc_{min}. Figure 16 shows the internal arrangement of this structure.

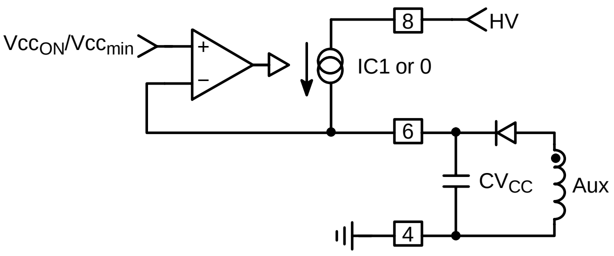


Figure 16. The Current Source Brings Vcc Above Vcc_{ON} and Then Turns Off

Once the power supply has started, the Vcc shall be constrained below 16 V, which is the maximum rating on pin 6. Figure 17 portrays a typical NCP1377 startup sequence with a Vcc regulated at 12.5 V.

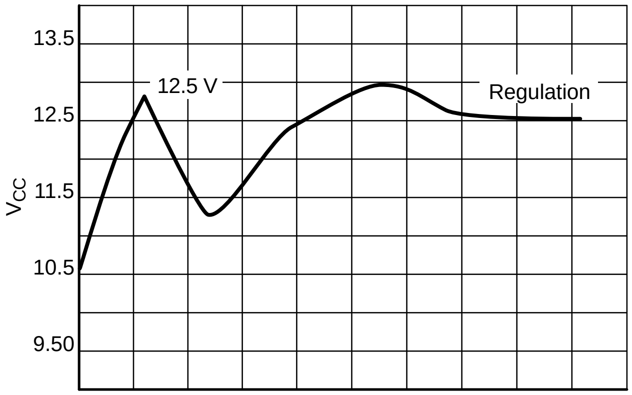


Figure 17. A Typical Startup Sequence for the NCP1377

Skipping Cycle Mode

The NCP1377 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so−called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 18) and follows the following formula: $\frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw \cdot D_{burst}$ with:

Lp = Primary inductance

Fsw = Switching frequency within the burst

Ip = Peak current at which skip cycle occurs

D_{burst} = Burst width/burst recurrence

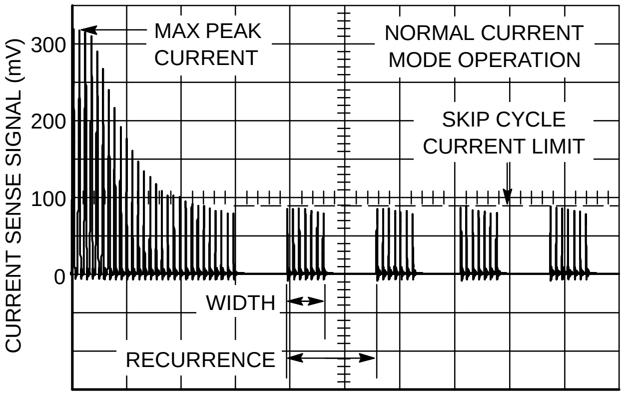


Figure 18. The Skip Cycle Takes Place at Low Peak Currents which Guarantees Noise−Free Operation

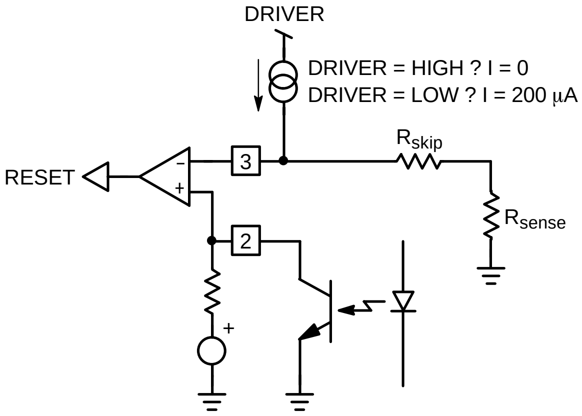


Figure 19. A Patented Method Allows for Skip Level Selection via a Series Resistor Inserted in Series with the Current

The skip level selection is done through a simple resistor inserted between the current sense input and the sense element. Everytime the NCP1377 output driver goes low, a 200 μA source forces a current to flow through the sense pin (Figure 19): when the driver is high, the current source is off and the current sense information is normally processed. As soon as the driver goes low, the current source delivers 200 μA and develops a ground referenced voltage across Rskip. If this voltage is below the feedback voltage, the current sense comparator stays in the low state and the internal latch can be triggered by the next clock cycle. Now, if because of a low load mode the feedback voltage is below Rskip level, then the current sense comparator permanently resets the latch and the next clock cycle (given by the demagnetization detection) is ignored: we are skipping cycles as shown by Figure 18. As soon as the feedback voltage goes up again, there can be two situations: the recurrent period is small and a new demagnetization detection (next wave) signal triggers the NCP1377. To the opposite, in low output power conditions, no more ringing waves are present on the drain and the toggling of the current sense comparator alone initiates a new cycle start. Figure 20 depicts these two different situations.

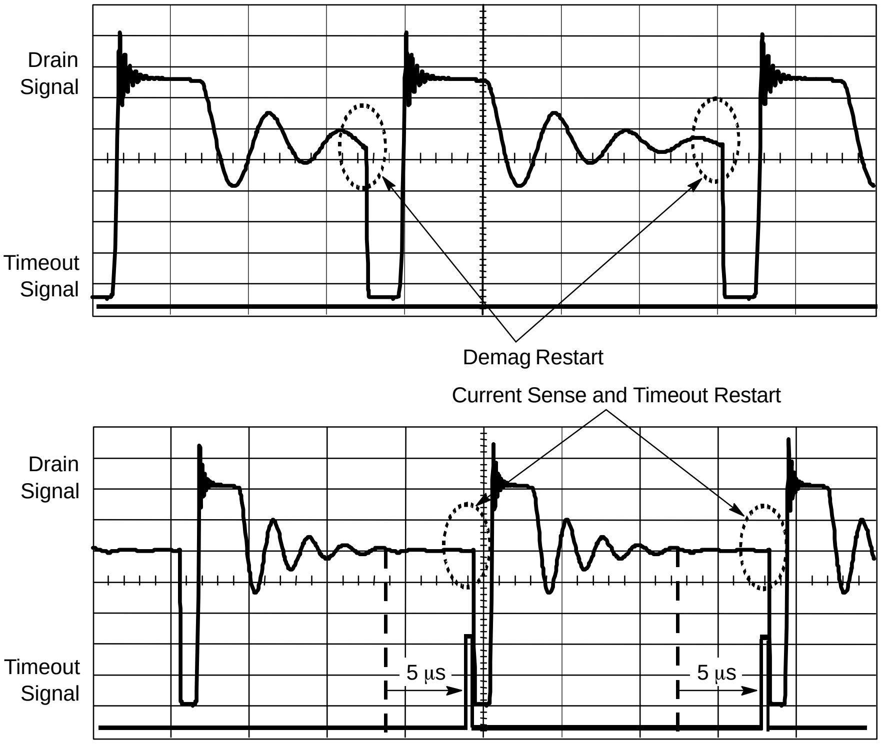


Figure 20. When the primary natural ringing becomes too low, the internal TimeOut together with the sense comparator initiates a new cycle when FB passes the skip level.

Demagnetization Detection

The core reset detection is done by monitoring the voltage activity on the auxiliary winding. This voltage features a FLYBACK polarity. The typical detection level is fixed at 50 mV as exemplified by Figure 21.

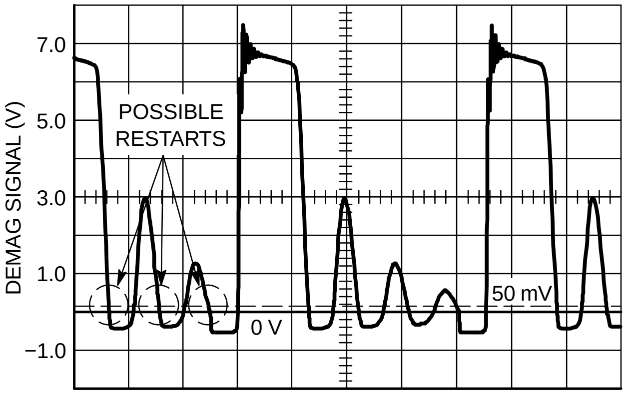


Figure 21. Core Reset Detection is Done through a Dedicated Auxiliary Winding Monitoring

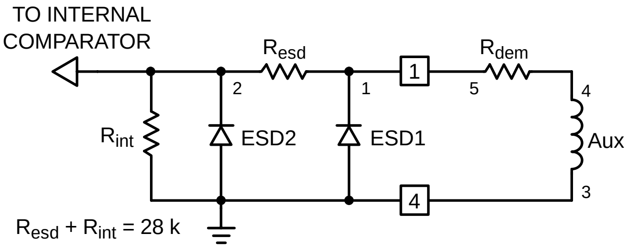


Figure 22. Internal Pad Implementation

An internal timer prevents any restart within 8.0 μs further to the driver going−low transition for NCP1377, and 3.0 μs for NCP1377B. This prevents the switching frequency to exceed (1.0/T_{ON} + T_{blank}) but also avoid false leakage inductance tripping at turn−off. In some cases, the leakage inductance kick is so energetic, that a slight filtering is necessary.

The NCP1377 demagnetization detection pad features a specific component arrangement as detailed by Figure 22. In this picture, the zener diodes network protect the IC against any potential ESD discharge that could appear on the pins. The first ESD diode connected to the pad, exhibits a parasitic capacitance. When this parasitic capacitance (10 pF typically) is combined with Rdem, a restart delay is created and the possibility to switch right in the drain−source wave exists. This guarantees QR operation with all the associated benefits (low EMI, no turn−on losses etc.). Rdem should be calculated to limit the maximum current flowing through pin 1 to less than +3.0 mA/−2.0 mA: If during turn−on, the auxiliary winding delivers 30 V (at the highest line level), then the minimum Rdem value is defined by: 30 + 0.7/3.0 mA = 10.2 kΩ. This value will be further increased, e.g. to introduce a restart delay and also a slight filtering in case of high leakage energy.

Figure 23 portrays a typical Vds shot at nominal output power.

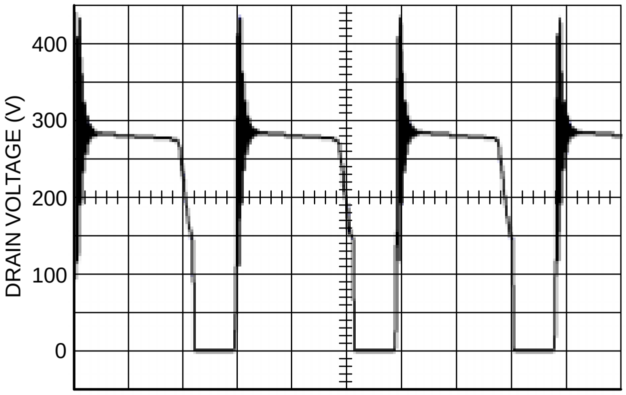


Figure 23. The NCP1377 Operates in Borderline/Critical Operation

Overvoltage Protection

The overvoltage protection works by sampling the plateau voltage after the turn−off sequence. A 4.5 μs delay for NCP1377 and 1.5 μs for NCP1377B guarantees a clean plateau, providing that the leakage inductance ringing has been fully damped. If this would not be the case, the designer should install a small RC damper across the transformer primary inductance connections. Figure 24 shows where the sampling occurs on the auxiliary winding.

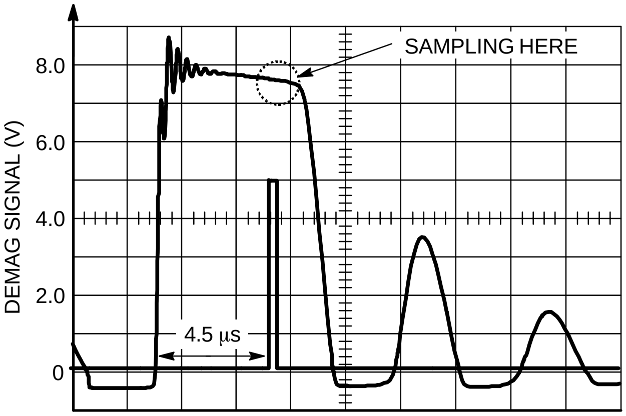


Figure 24. A Voltage Sample is Taken 4.5 μs After the Turn−Off Sequence

When an OVP condition has been detected, the NCP1377 enters a latchoff phase and stops all switching operations. The controller stays fully latched in this position and the startup source being still active, it keeps the Vcc going up and down between 12.5 V and 5.6 V. This state lasts until the Vcc is cycled down to 4.0 V, e.g. when the user unplugs the power supply from the mains outlet.

By default, the OVP comparator is biased to a 5.0 V reference level and pin1 is routed via a divide by a 1.44 network. As a result, when Vpin1 reaches 7.2 V, the OVP comparator is triggered. The threshold can thus be adjusted by either modifying the power winding to auxiliary winding turn ratios to match this 7.2 V level or insert a resistor from pin1 to ground to cope with your design requirement.

Latching Off the NCP1377

In certain cases, it can be very convenient to externally shut down permanently the NCP1377 via a dedicated signal, e.g. coming from a temperature sensor (Figure 25). The reset occurs when the user unplugs the power supply from the mains outlet. To trigger the latchoff by an external signal, a simple PNP transistor can do the work, as Figure 26 shows.

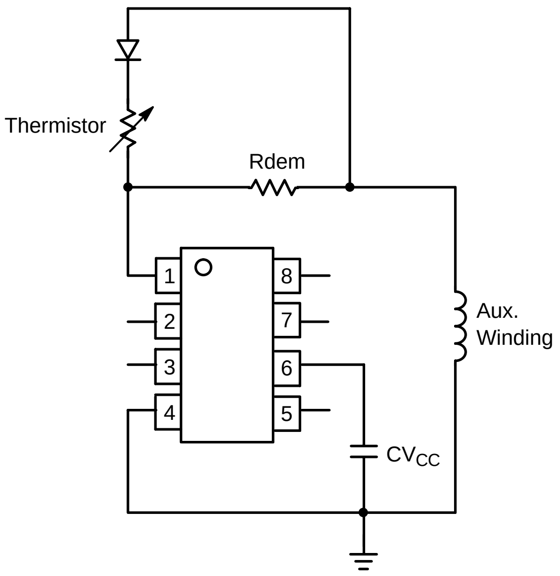


Figure 25. A simple arrangement triggers the latchoff as soon as the temperature exceeds a given setpoint.

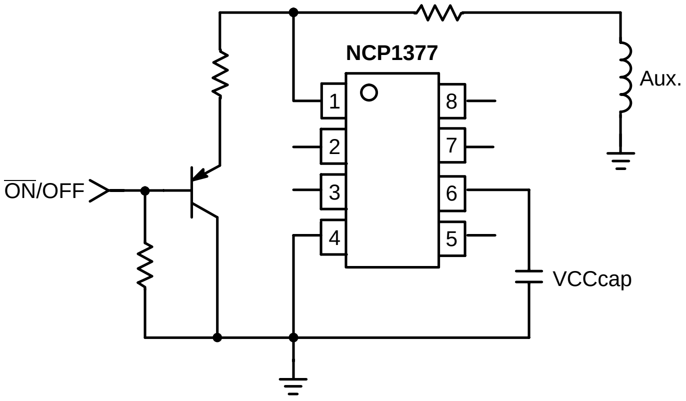


Figure 26. A simple transistor arrangement triggers the latchoff as soon as the temperature exceeds a given setpoint.

Shutting Off the NCP1377

Shutdown can easily be implemented through a simple NPN bipolar transistor as depicted by Figure 27. When OFF, Q1 is transparent to the operation. When forward biased, the transistor pulls the FB pin to ground (Vcesat ≈ 200 mV) and permanently disables the IC. A small time constant on the transistor base will avoid false triggering (Figure 27).

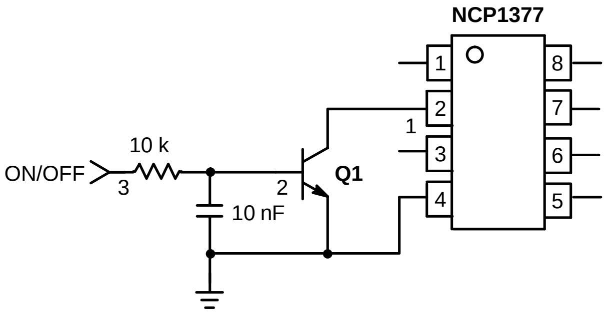


Figure 27. A Simple Bipolar Transistor Totally Disables the IC

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short−circuit protection. A short−circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the auxiliary voltage also decreases because it also operates in Flyback and thus duplicates the output voltage, providing the leakage inductance between windings is kept low. To account for this situation and properly protect the power supply, NCP1377 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low Duty Cycle. The system auto−recovers when the fault condition disappears.

During the startup phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. The auxiliary voltage takes place after a few switching cycles and self−supplies the IC. In presence of a short circuit on the output, the auxiliary voltage will go down until it crosses the undervoltage lockout level of typically 7.5 V. When this happens, NCP1377 immediately stops the switching pulses and unbiases all unnecessary logical blocks. The overall consumption drops, while keeping the gate grounded, and the Vcc slowly falls down. As soon as Vcc reaches typically 5.6 V, the startup source turns−on again and a new startup sequence occurs, bringing Vcc toward 12.5 V as an attempt to restart. If the default has gone, then the power supply normally restarts. If not, a new protective burst is initiated, shielding the SMPS from any runaway. Figure 28 portrays the typical operating signals in short circuit.

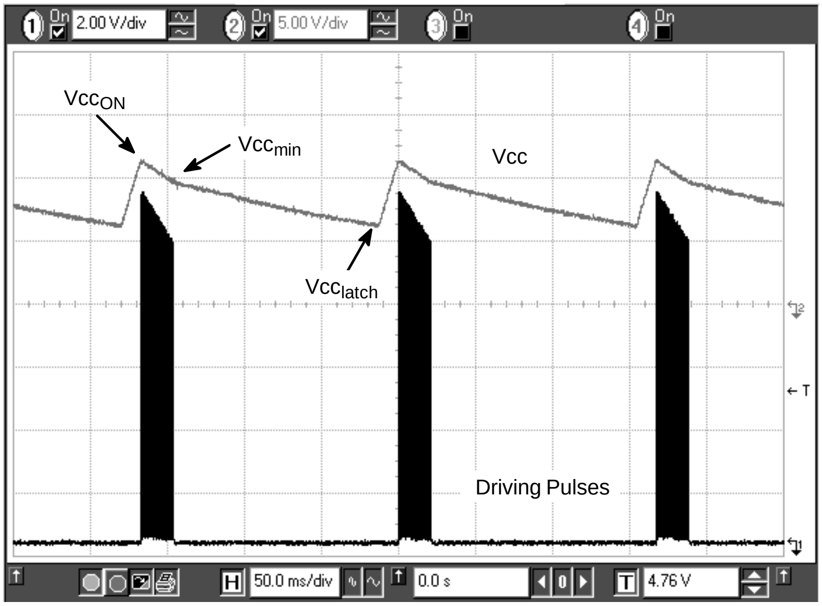


Figure 28. Typical Waveforms in Short Circuit Conditions

Soft−Start

The NCP1377 features an internal 1.0 ms Soft−Start to soften the constraints occurring in the power supply during startup. It is activated during the power on sequence. As soon as Vcc reaches Vcc_{ON} , the peak current is gradually increased from nearly zero up to the maximum clamping level (e.g. 1.0 V). The Soft−Start is also activated during the overcurrent burst (OCP) sequence. Every restart attempt is followed by a Soft−Start activation. Generally speaking, the Soft−Start will be activated when Vcc ramps up either from zero (fresh power−on sequence) or 5.6 V, the latchoff voltage occurring during OCP.

Calculating the Vcc Capacitor

The Vcc capacitor can be calculated knowing the IC consumption as soon as Vcc reaches Vcc_{ON}. Suppose that a NCP1377 is used and drives a MOSFET with a 30 nC total gate charge (Qg). The total average current is thus made of Icc1 (1.0 mA) plus the driver current, Fsw x Qg or 1.8 mA. The total current is therefore 2.8 mA. The ΔV available to fully startup the circuit (e.g. never reach the 7.5 V UVLO during power on) is 12.5 – 7.5 = 5.0 V. We have a capacitor which then needs to supply the NCP1377 with 2.8 mA during a given time until the auxiliary supply takes over. Suppose that this time was measured at around 15 ms. CV_{CC} is calculated using the equation $C = \frac{\Delta t \cdot i}{\Delta V}$ or $C \geq 8.6\ \mu F$. Select a 22 µF/16 V and this will fit. During the latchoff phase, the current consumption drops to ICC3 or 220 µA. We can now calculate how long this latchoff phase will last: (7.5–5.6) x 22 µ/220 u = 190 ms.

Protecting Pin 8 Against Negative Spikes

As any CMOS controller, NCP1377 is sensitive to negative voltages that could appear on its pins. To avoid any adverse latchup of the IC, we strongly recommend to insert a resistor R_{HV} in series with pin8. This resistor prevents from adversely latching the controller in case of negative spikes appearing on the bulk capacitor during the power−off sequence. A typical value of 6.8 kΩ/0.5 W is suitable. This resistor does not dissipate any power since it only sees current during the startup sequence and during overload. Calculations actually involve the minimum voltage on pin8 necessary to fully activate the current source. This minimum voltage being 40 V, therefore R_{HV} shall be less than: ($Vbulk_{min}$–40)/6.0 m.

Operating Shots

Following are some oscilloscope shots captured at Vin = 120 VDC with a transformer featuring a 800 µH primary inductance.

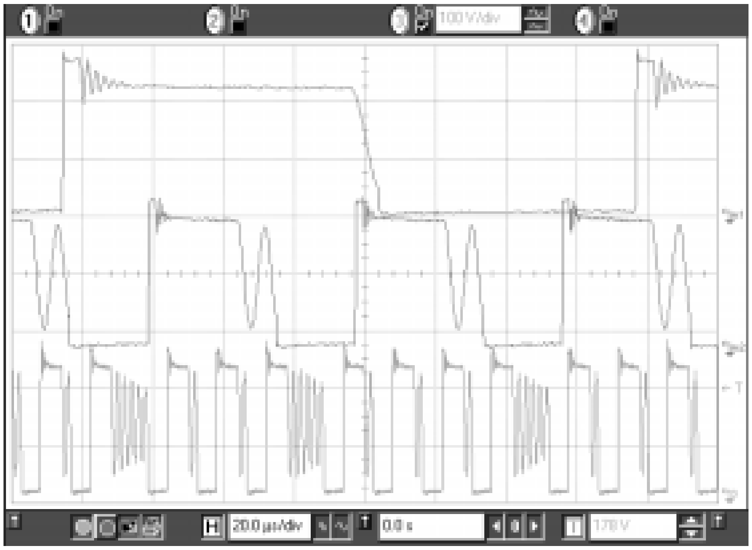


Figure 29. This plot gathers waveforms captured at three different operating points:

1st Upper Plot: Free run, valley switching operation, Pout = 26 W.

2nd Middle Plot: Min Toff clamps the switching frequency and selects the second valley.

3rd Lowest Plot: The skip slices the second valley pattern and will further expand the burst as Pout goes low.

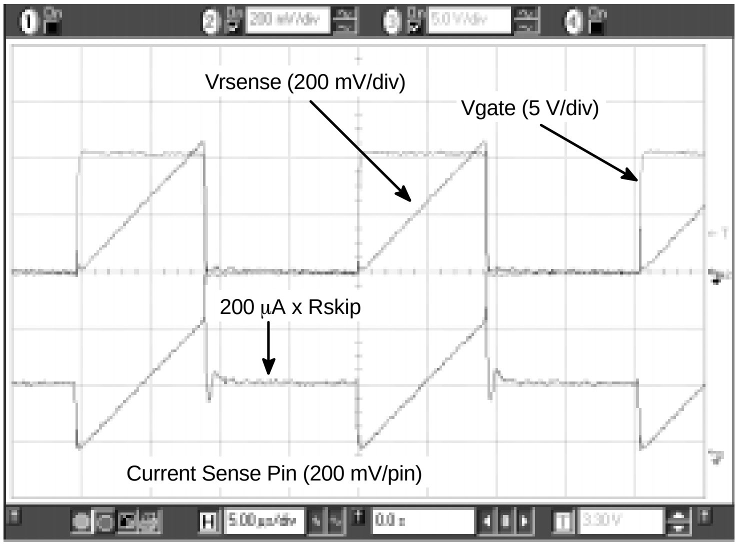


Figure 30. This picture explains how the 200 µA internal offset current creates the skip cycle level.

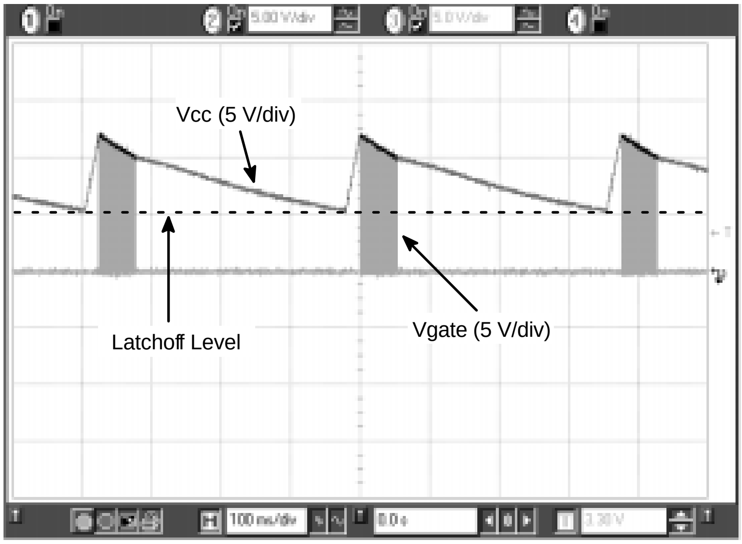
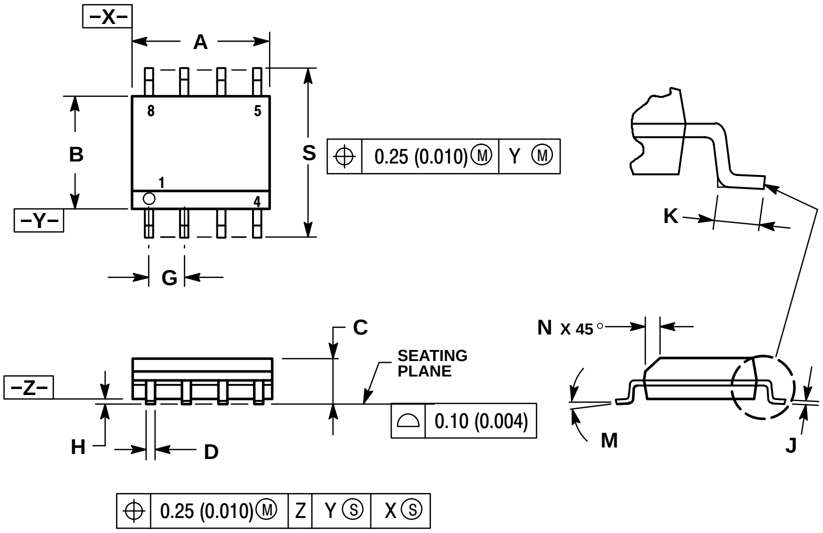


Figure 31. The short−circuit protection forces the IC to enter burst in presence of a secondary overload.

PACKAGE DIMENSIONS

SOIC−8

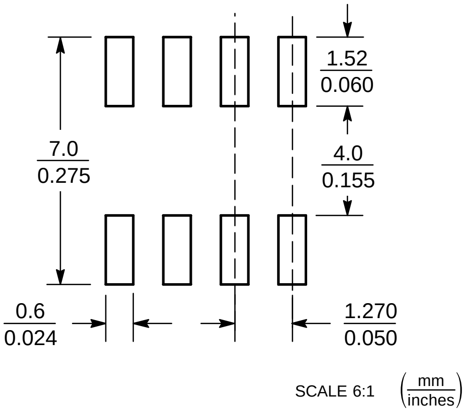
D SUFFIX
CASE 751−07
ISSUE AC



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

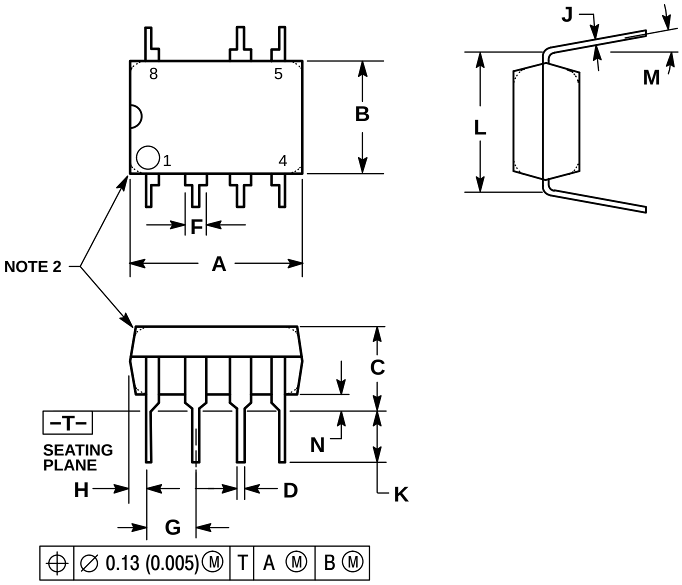
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

PDIP−7
P SUFFIX
CASE 626B−01
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
5. DIMENSIONS A AND B ARE DATUMS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	9.40	10.16
B	6.10	6.60
C	3.94	4.45
D	0.38	0.51
F	1.02	1.78
G	2.54 BSC	
H	0.76	1.27
J	0.20	0.30
K	2.92	3.43
L	7.62 BSC	
M	−−−	10 °
N	0.76	1.01

The product described herein (NCP1377), may be covered by one or more of the following U.S. patents: 6,362,067, 6,385,060, 6,385,061, 6,429,709, 6,587,357, 6,633,193. There may be other patents pending.

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