NCP1540

Product Preview

3.5 A High Efficiency Step-Down DC-DC Converter

The NCP1540 is a high efficiency step−down buck regulator with an integrated high side MOSFET. An internal 110 mΩ N−channel MOSFET power switch enables delivering of up to 3.5 A continuous load currents with up to >90% efficiency. The NCP1540 features current−mode pulse−width modulation (PWM) control with feed forward compensation and operates at fixed switching frequency of 385 kHz. The wide input voltage range device is capable of producing an output voltage as low as 1.2 V.

The NCP1540 incorporates an externally compensated error amplifier and a programmable soft−start function. Protection features include output overload and short circuit protection and under voltage lockout (UVLO).

Features

- Wide Input Voltage Range from 4.5 V to 28 V
- Adjustable Output Voltage Down to 1.2 V
- Guaranteed 3.5 A DC Output Current
- Up to >90% Efficiency enabled by 110 mΩ integrated MOSFET Switch
- Fixed 385 kHz Switching Frequency
- Improved Line Regulation and Transient Response
- Error Amplifier with External Compensation
- Enable / Disable Capability
- Low Power Shutdown Mode (typ 20 μA @ 12 V)
- Externally Programmable Soft−Start
- Undervoltage Lock−Out
- Thermal Shutdown
- Cycle−by−Cycle Overcurrent Protection
- Hiccup−Mode Short Circuit Protection

Typical Applications

- LCD and PDP TV
- On−Card Switching Regulators
- Computer Peripherals
- Distributed Power Systems

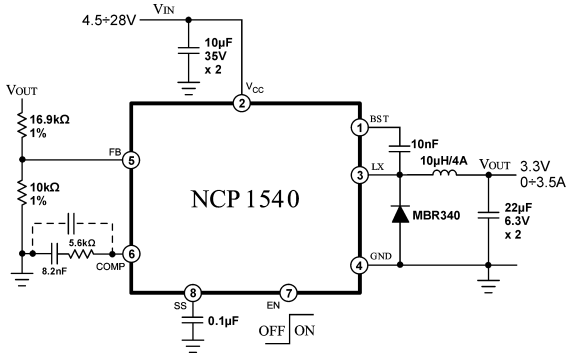

Figure 1. Typical Application Circuit

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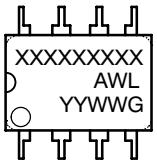
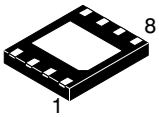
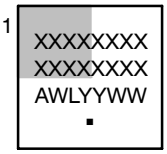
MARKING DIAGRAMS

PDIP−8
P SUFFIX
CASE 626





DFN8
MN SUFFIX
CASE 506BG



xxxx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G/▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP1540PR2G	PDIP−8 (Pb−Free)	98 / Tube
NCP1540MNR2G	DFN8 (Pb−Free)	2500/Tape & Reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

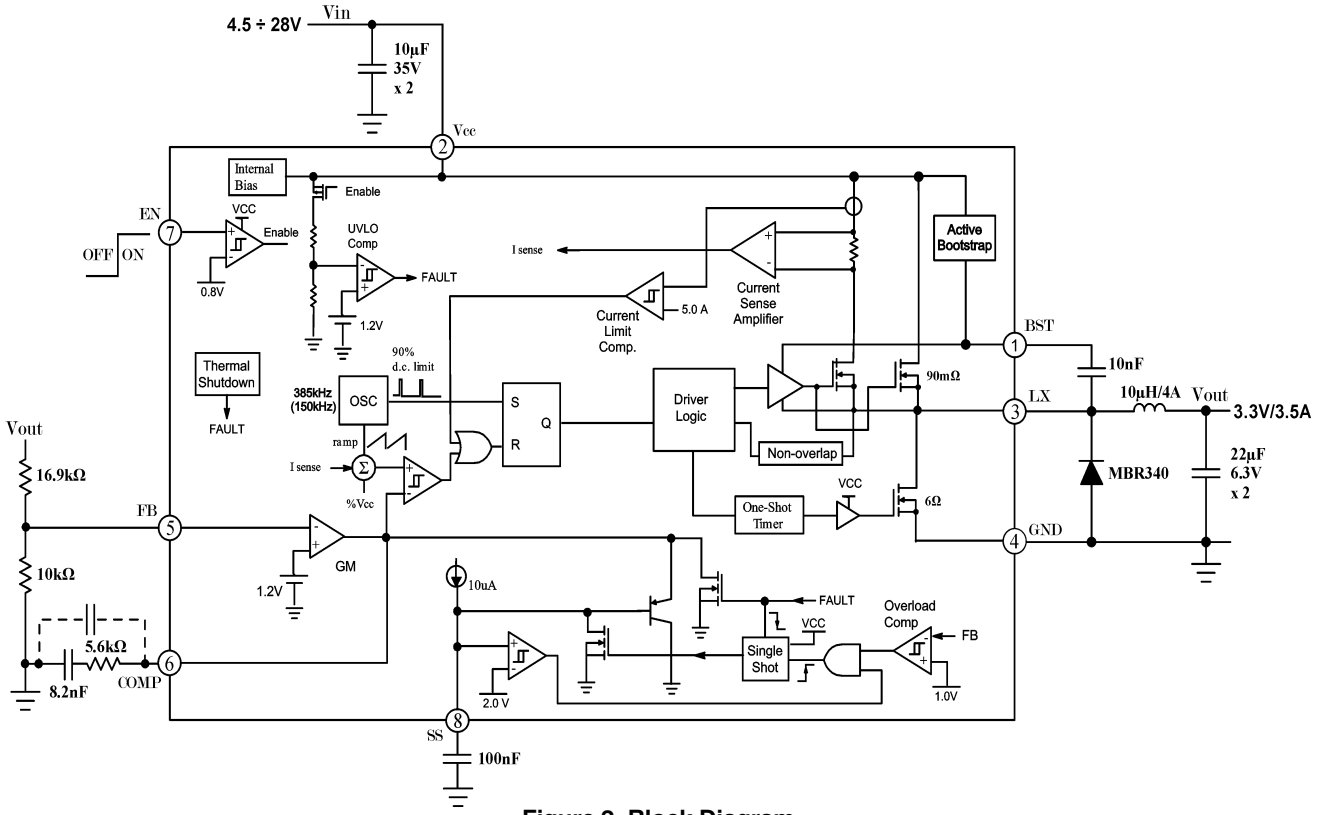


Figure 2. Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	BST	Supply rail for the floating top gate driver. Connect a capacitor (C_{BST}) between this BST pin and the LX pin. Recommended C_{BST} capacitor value is in the range from 0.01 μF to 0.1 μF. Ensure that C_{BST} is placed near the IC.
2	VCC	Power Input. VCC supplies the power to the IC, as well as the power switch.
3	LX	Power Switch Output. Connect Inductor from LX node to the output capacitor and load.
4	GND	Ground pin of the IC
5	FB	This pin is the inverting input to the error amplifier. Connect this pin to the output resistor divider (if used) or directly to Vout.
6	COMP	Compensation Pin. This is the output of the error amplifier (EA) and the non−inverting input of the PWM comparator. Use this pin with respect to ground to compensate the voltage−control feedback loop. This pin should not be shorted to ground to disable switching.
7	EN	Enable input to the regulator. Pull this pin low to disable the device. Pull this pin high to enable the device.
8	SS	Soft−start control input to the regulator. An internal current source charges external capacitor connected to this pin to set the soft−start time. A 0.1 μF capacitor sets a soft−start time of 10 ms.
	EP	Exposed Pad. Connect this pad to GND pin 4. Exposed Pad also serves as a thermal contact to the PC Board.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Main Supply Voltage	V_{CC}	−0.3	40 (Note 1)	V
Bootstrap Supply Voltage	V_{BST}	−0.3	40 (Note 1)	V
Bootstrap Supply Voltage (Note 2)	V_{BST} vs V_{LX}	−0.3	13.2	V
LX Pin Voltage	V_{LX}	−0.7 −5V for < 50 nsec	V_{CC} (Note 1)	V
LX Pin Source Current	I_{LX}		Internally limited	A
EN Pin Input Voltage	V_{EN}	−0.3	V_{CC}	V
All other pins	−	−0.3	5.5	V

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient (Note 3,4)	$R_{\theta JA}$	TBD	°C/W
Thermal Resistance, Junction−to−Case (Note 3,4)	$R_{\theta JC}$	TBD	°C/W
Operating Ambient Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C
Junction Operating Temperature	T_J	−40 to 150	°C
ESD Withstand Voltage (Note 5) Human Body Model Machine Model	V_{ESD}	 2.0 200	 kV V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Approaching the absolute maximum rating for the V_{CC} pin may cause the voltage on the LX and BST pin to exceed the absolute maximum rating.
2. Dynamic operation with C_{BST} bootstrap capacitor connected between LX and BST pins. Loading BST pin with other external voltage is not allowed.
3. According JEDEC standard JESD22−A108B.
4. 1 in^2 , 2 oz Cu board.
5. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) +/−2.0 kV per JEDEC standard: JESD22−A114
   Machine Model (MM) +/−200V per JEDEC standard: JESD22−A115
   Latch−up current maximum rating: +/−100mA per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, −40°C < T_J < 125°C (Note 6) for min/max values, T_J = 25°C for typical values, unless otherwise noted).

Characteristic	Conditions	Min	Typ	Max	Unit
Recommended Operating Conditions					
Input Voltage Range		4.5		28	V
Bootstrap Voltage Range	VLX = V_{CC}	VCC + 3.5		40	V
Supply Current					
Quiescent Supply Current	V_{EN} = 2.6 V, V_{FB} = 1.4 V, No Switching		2.0	3.0	mA
Boost Quiescent Current	V_{FB} = 1.4 V, No Switching, V(BST−LX) = 12 V		140		μA
Shutdown Supply Current	V_{EN} = 0 V		20	30	μA
Under Voltage Lockout					
UVLO Threshold	V_{CC} Rising	3.85	4.2	4.4	V
UVLO Hysteresis			500		mV
Switching Regulator					
Feedback Voltage	T_J = 25°C −40°C < T_J < 125°C	1.176 1.164	1.2 1.2	1.224 1.236	V
Oscillator Frequency	T_J = −40°C to 125°C	308	385	460	kHz
Comp Pin Operating Voltage Range		1.0		2.9	V
Minimum Duty Cycle	V_{COMP} = 0.8 V		0		%
Maximum Duty Cycle	V_{COMP} = 2.1 V	85			%
High Side MOSFET $R_{DS(on)}$	V_{CC}=12 V, I_{LX} = 1 A		110	190	mΩ
High Side Leakage Current	V_{EN} = 0 V, V_{LX} = 0 V			10	μA
Low Side MOSFET $R_{DS(on)}$	V_{CC}=12 V, I_{LX} = −0.1 A		6.0	TBD	Ω
Low Side Leakage Current	V_{EN} = 0 V, V_{LX} = V_{CC} −1 V			10	μA
Low Side MOSFET On Time		200	300	400	ns
Current Limit Set Point		4.5	5.0	5.5	A
Current Loop Transient Response	(Note 7)		100		nsec
Error Amplifier (GM)					
Transconductance	(Note 7)	0.85	1.0	1.15	mmho
DC Gain	(Note 7)	60	65	70	dB
Unity Gain Bandwidth	(Note 7)		4.0		MHz
Output Sink Current	V_{FB} = 1.4 V, V_{COMP} = 2.0 V	TBD	100	TBD	μA
Output Source Current	V_{FB} = 1.0 V, V_{COMP} = 1.0 V	TBD	100	TBD	μA
FB Bias Current			0.1	1	μA
Soft−Start					
Soft−Start Period	V_{FB} < 1.2 V, C_{SS} = 0.1 μF		10		ms
Soft−Start Source Current		8.5	10	11.5	μA
Enable					
Enable Threshold (Rising)		0.6	0.7	1.0	V
Enable Threshold (Falling)		0.3	0.5	0.7	V
Enable Hysteresis			0.2		V
Enable Pin Input Current	V_{EN} = 0.3 V		1.0	10	μA
Thermal Shutdown					
Overtemperature Shutdown Trip Point	Temperature rising (Note 7)		160		°C

6. Power dissipation limits must be observed.
7. Guaranteed by design.

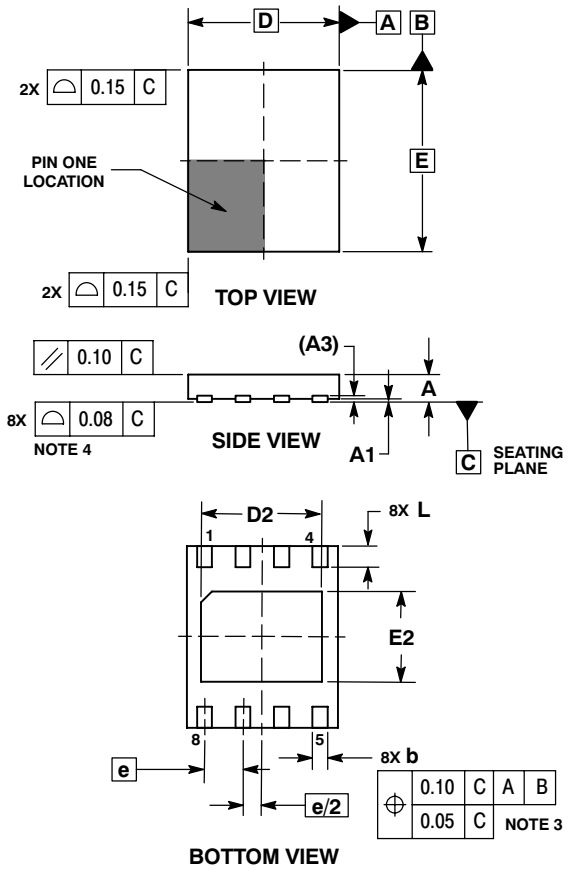
DETAILED DESCRIPTION

The NCP1540 is a current−mode step−down regulator. It regulates input voltages from 4.5 V to 28 V down to an output voltage as low as 1.2 V, and is able to supply up to 3.5 A of continuous load current.

The NCP1540 uses current−mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal error amplifier. The output current of the transconductance error amplifier is presented at COMP where a network compensates the regulation control system. The voltage at COMP is compared to the internally measured switch current to control the output voltage. The converter uses an internal N−Channel MOSFET switch to step−down the input voltage to the regulated output voltage. Since the MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between LX and BST drives the gate. The capacitor is internally charged when LX is low. An internal 6 Ω switch from LX to GND is used to insure that LX is pulled to GND when it is low to fully charge the BST capacitor.

PACKAGE DIMENSIONS

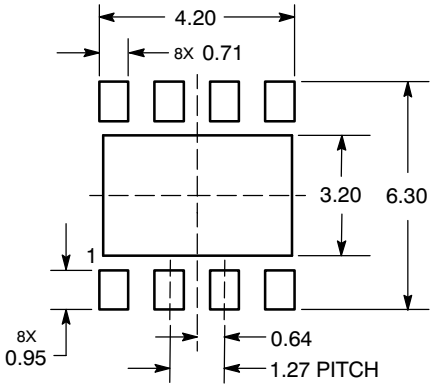
DFN8 5x6, 1.27P
CASE 506BG−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.45	0.55
D	5.00 BSC	
D2	3.90	4.10
E	6.00 BSC	
E2	2.90	3.10
e	1.27 BSC	
L	0.60	0.80

SOLDERING FOOTPRINT*

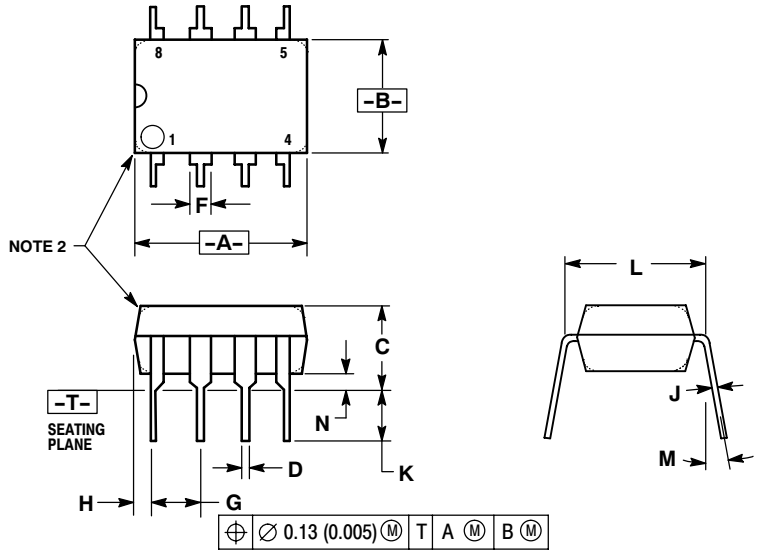


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

PDIP−8
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

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