Highly-Integrated Green-Mode PWM Controller **SG6741**

FEATURES

- High-voltage start-up
- Low operating current (4mA)
- Linearly decreasing PWM frequency to 22kHz
- Frequency hopping to reduce EMI emission
- Peak-current-mode control
- Cycle-by-cycle current limiting
- Leading-edge blanking
- Synchronized slope compensation
- Gate output maximum voltage clamp (18V)
- V_{DD} over-voltage protection (auto restart)
- V_{DD} under-voltage lockout (UVLO)
- Internal open-loop protection
- Constant power limit (full AC input range)

APPLICATIONS

General-purpose switch-mode power supplies and flyback power converters, including:

- Power adapters
- Open-frame SMPS

DESCRIPTION

The highly integrated SG6741 series of PWM controllers provides several features to enhance the performance of flyback converters.

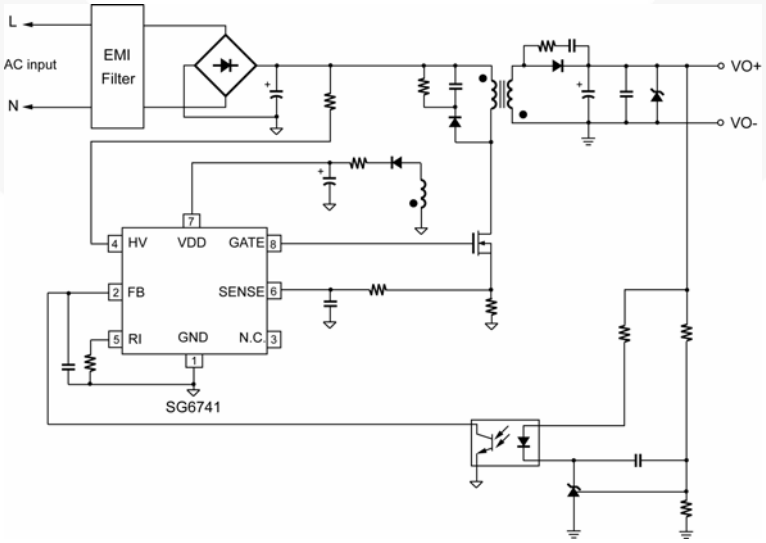
To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency at light-load conditions. To avoid acoustic-noise problems, the minimum PWM frequency is set above 22KHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage start-up circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, SG6741 is manufactured using the BiCMOS process, which allows operating current as low as 4mA.

SG6741 integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. Its built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary internal line compensation ensures constant output power limit over a wide range of AC input voltages, from 90VAC to 264VAC.

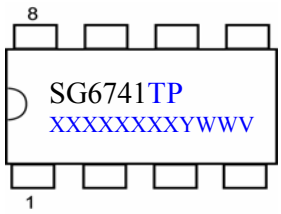
SG6741 provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety when an open-loop or output short-circuit failure occurs. PWM output is disabled until V_{DD} drops below the UVLO lower limit; then the controller starts again. As long as V_{DD} exceeds about 26V, the internal OVP circuit is triggered.

SG6741 is available in an 8-pin DIP or SOP package.

TYPICAL APPLICATION

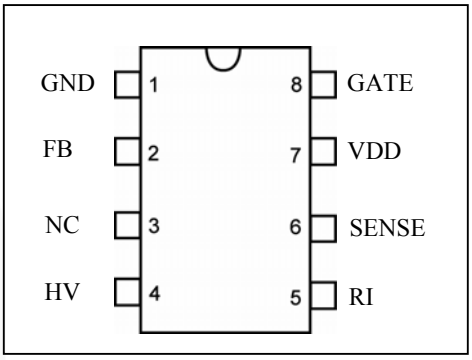


MARKING INFORMATION



T: S = SOP
P: Z =Lead Free
Null=regular package
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION



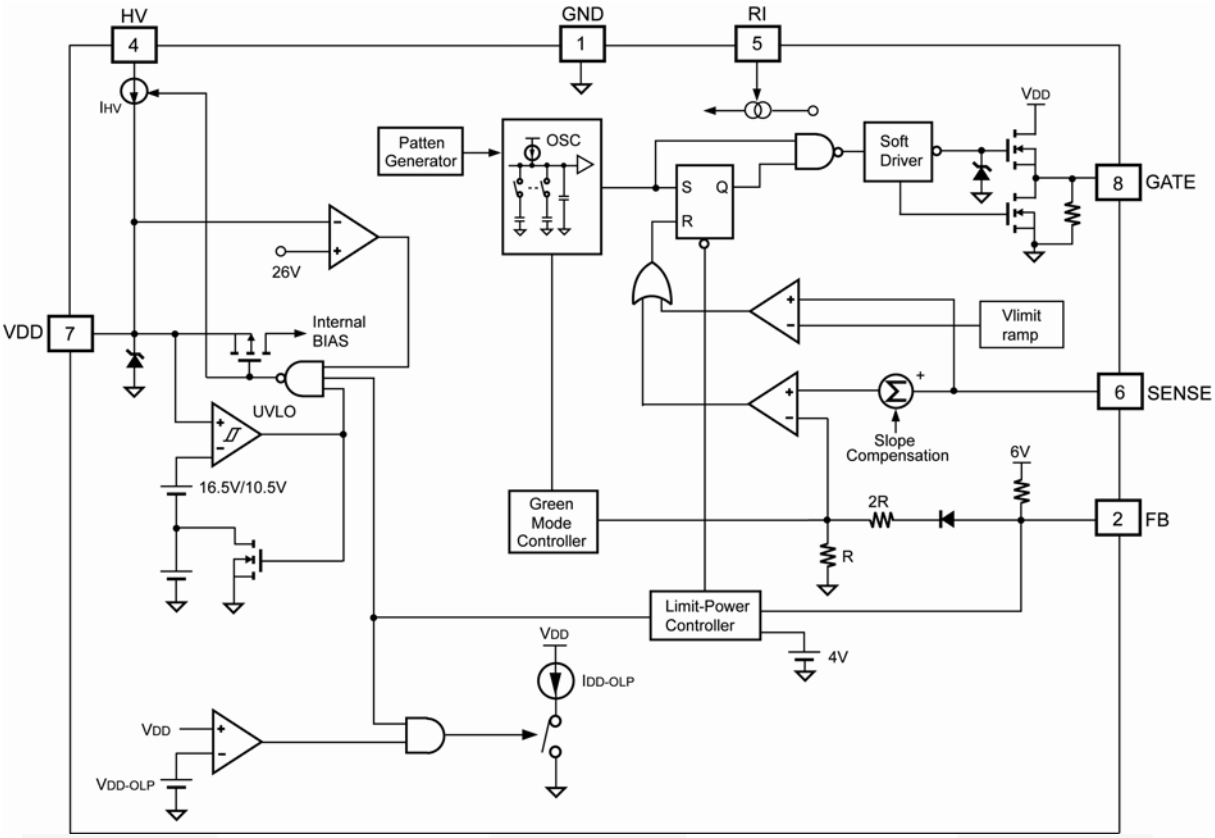
ORDERING INFORMATION

Part Number	Pb-Free	Package
SG6741SZ		SOP-8

PIN DESCRIPTIONS

Pin No.	Symbol	Function	Description
1	GND	Ground	Ground.
2	FB	Feedback	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the current-sense signal on the SENSE pin.
3	NC	NA	NC pin.
4	HV	Start-up Input	For start-up, this pin is pulled high to the line input or bulk capacitor via resistors.
5	RI	Reference Setting	A resistor connected from the RI pin to GND pin provides the SG6741 with a constant current source. This determines the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor (R_I) results in a 65kHz center PWM frequency.
6	SENSE	Current Sense	Current sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
7	VDD	Power Supply	Power supply. The internal protection circuit disables PWM output as long as V_{DD} exceeds the OVP trigger point.
8	GATE	Driver Output	The totem-pole output driver. Soft driving waveform is implemented for improved EMI.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
V_{DD}	Supply Voltage	30		V
V_{HV}	Input Voltage to HV Pin	500		V
V_L	Input Voltage to FB, SENSE, Pin	-0.3 to 7		V
P_D	Power Dissipation, T_A < 50°C	DIP	800	mW
		SOP	400	mW
$R_{\Theta JA}$	Thermal Resistance, Junction-to-Air	DIP	82.5	°C/W
		SOP	141	°C/W
T_J	Operating Junction Temperature	-40 to +125		°C
T_{STG}	Storage Temperature Range	-55 to +150		°C
T_L	Lead Temperature (Wave soldering or IR, 10 seconds)	260		°C
ESD	Electrostatic Discharge Capability, Human Body Model (All pins except HV pin)	3		KV
	Electrostatic Discharge Capability, Machine Model (All pins except HV pin)	250		V

*All voltage values, except differential voltages, are given with respect to the GND pin.

*Stresses above those listed may cause permanent damage to the device.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
T_A	Operating Ambient Temperature	-20 to +85	°C

*For proper operation

ELECTRICAL CHARACTERISTICS

$12V \le V_{DD} \le 25V$; $-20°C \le T_A \le 85°C$, unless otherwise noted.

V_{DD} Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD-OP}	Continuously Operating Voltage				22	V
V_{DD-ON}	Start Threshold Voltage		15.5	16.5	17.5	V
V_{DD-OFF}	Minimum Operating Voltage		9.5	10.5	11.5	V
I_{DD-ST}	Start-up Current	V_{DD-ON} – 0.16V			30	µA
I_{DD-OP}	Operating Supply Current	V_{DD}=15V, GATE open		4	5	mA
I_{DD-OLP}	Internal Sink Current	V_{DD-OLP} +0.1V	50	70	90	µA
V_{DD-OLP}	I_{DD-OLP} Off Voltage		6.5	7.5	8.0	V
V_{DD-OVP}	V_{DD} Over-Voltage Protection	(Auto Restart)	25	26	27	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage-protection Debounce Time	(Auto Restart)	100	180	260	µs

HV Section

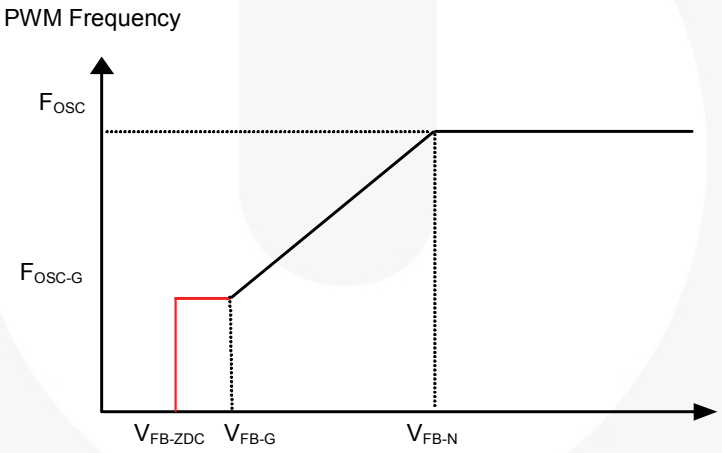
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{HV}	Supply Current Drawn from Pin HV	V_{AC}=90V(V_{DC}=120V), V_{DD}=10µF		2		mA
I_{HV-LC}	Leakage Current After Start-up	HV=500V, V_{DD}=V_{DD-OFF} +1V		1	20	µA

Oscillator Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{OSC}	Frequency in Nominal Mode	Center Frequency	62	65	68	kHz
		Hopping Range	±3.7	±4.2	±4.7	
t_{HOP}	Hopping Period			4.4		ms
F_{OSC-G}	Green-Mode Frequency		16	18	21	kHz
F_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11V to 22V			5	%
F_{DT}	Frequency Variation vs. Temp. Deviation	T_A=-20 to 85℃			5	%

Feedback Input Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
A_V	Input Voltage to Current-Sense Attenuation		1/3.75	1/3.20	1/2.75	V/V
Z_{FB}	Input Impedance		4		7	kΩ
$V_{FB-OPEN}$	FB Output High Voltage	FB Pin Open	5.5			V
V_{FB-OLP}	FB Open-Loop Trigger Level		3.7	4.0	4.3	V
t_{D-OLP}	Delay Time, FB Pin Open-Loop Protection	R_I=26kΩ	50	56	62	ms
V_{FB-N}	Green-Mode Entry FB Voltage		1.9	2.1	2.3	V
V_{FB-G}	Green-Mode Ending FB Voltage			V_{FB-N} -0.5		V
V_{FB-ZDC}	Zero Duty Cycle Input Voltage		V_{FB-G} -0.25	V_{FB-G} -0.20	V_{FB-G} -0.10	V



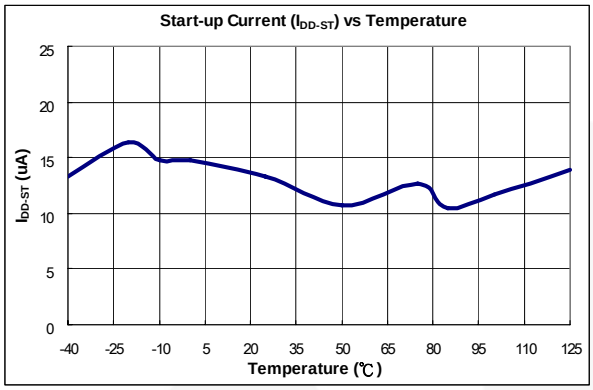
Current-Sense Section

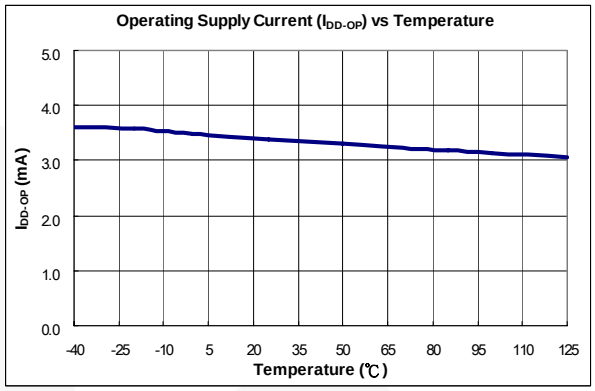
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_{SENSE}	Input Impedance			12		KΩ
V_{STHFL}	Current Limit Flatten Threshold Voltage		0.87	0.90	0.93	V
V_{STHVA}	Current Limit Valley Threshold Voltage	V_{STHFL}–V_{STHVA}	0.18	0.22	0.26	V
t_{PD}	Delay to Output			100	200	ns
t_{LEB}	Leading-Edge Blanking Time		275	350	425	ns
V_{S-SCP}	Threshold Voltage for SENSE Short-Circuit Protection			0.15		V
t_{D-SSCP}	Delay Time for SENSE Short-Circuit Protection	V_{SENSE}<0.15V, R_I=26kΩ		180		μs

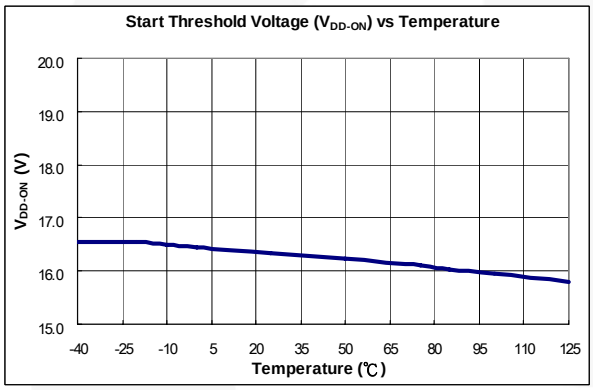
Gate Section

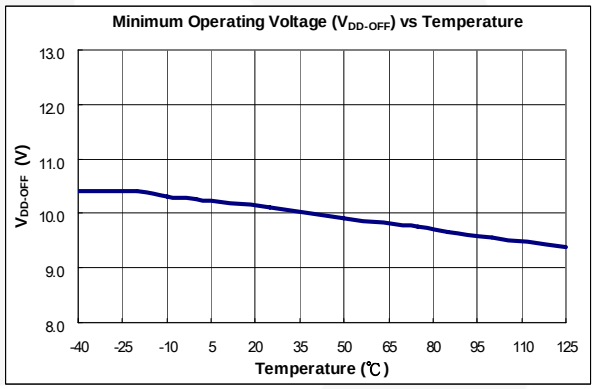
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DCY_{MAX}	Maximum Duty Cycle		70	75	80	%
V_{GATE-L}	Gate Low Voltage	V_{DD}=15V, I_O=50mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=12.5V, I_O=50mA	8			V
tr	Gate Rising Time	V_{DD}=15V, C_L=1nF	150	250	350	ns
tf	Gate Falling Time	V_{DD}=15V, C_L=1nF	30	50	90	ns
$I_{GATE-SOURCE}$	Gate Source Current	V_{DD}=15V, GATE=6V	250			mA
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22V			18	V

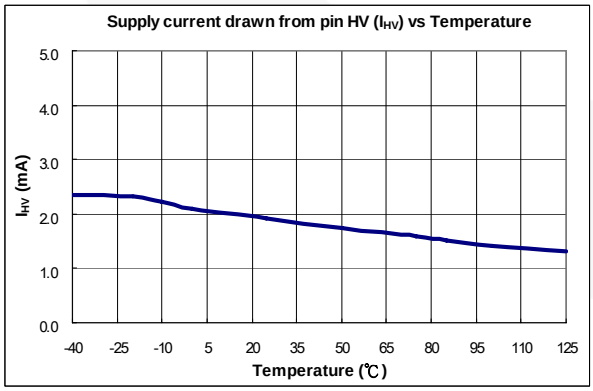
TYPICAL CHARACTERISTIC

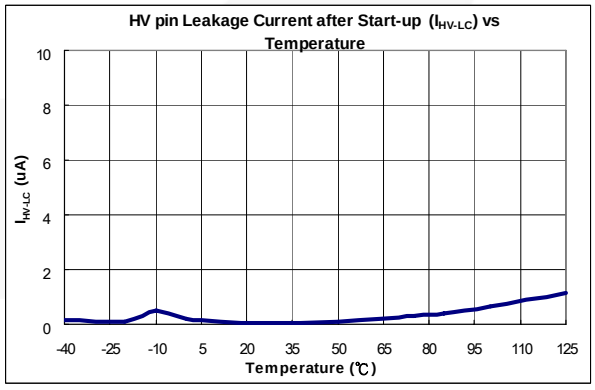


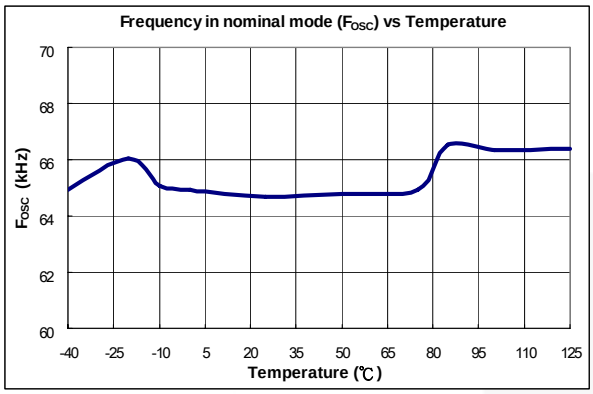


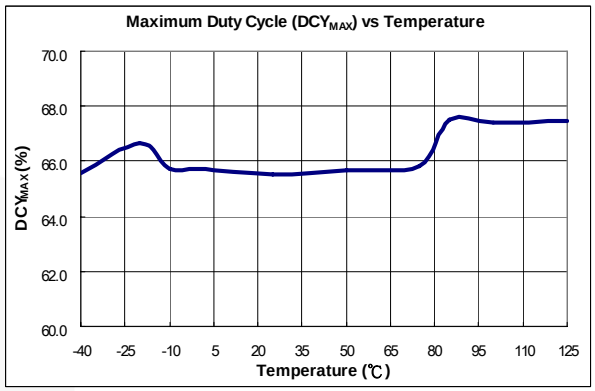









Frequency in nominal mode (F_{OSC}) vs Temperature
70
68
66
64
62
60
Fosc (kHz)
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Maximum Duty Cycle (DCY_{MAX}) vs Temperature
70.0
68.0
66.0
64.0
62.0
60.0
DCYMAX (%)
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

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Operation Description

Start-up Current

For start-up, the HV pin is connected to the line input or bulk capacitor through an external resistor, R_{HV}, which is recommended as 100KΩ. Typical start-up current drawn from pin HV is 2mA and it charges the hold-up capacitor through the resistor R_{HV}. When the V_{DD} capacitor level reaches V_{DD-ON}, the start-up current switches off. At that moment, the V_{DD} capacitor only supplies the SG6741 to maintain the V_{DD} before the auxiliary winding of the main transformer to carry on provide the operating current.

Operating Current

Operating current is around 4mA. The low operating current enables better efficiency and reduces the requirement of V_{DD} hold-up capacitance.

Green-Mode Operation

The patented green-mode function provides an off-time modulation to reduce switching frequency in light-load and no-load conditions. The on time is limited for better abnormal or brownout protection. VFB, which is derived from the voltage feedback loop, is used as the reference. Once VFB is lower than the threshold voltage, switching frequency is continuously decreased to the minimum green-mode frequency, around 22KHz (R_I=26KΩ).

Oscillator Operation

A resistor connected from the RI pin to GND generates a constant current source for the SG6741 controller. This current is used to determine the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor, R_I, results in a corresponding 65KHz PWM frequency. The relationship between R_I and the switching frequency is:

$$f_{PWM} = \frac{1690}{R_I\ (K\Omega)} (KHz) \quad \text{----------} \quad (1)$$

The range of the PWM oscillation frequency is designed as 47kHz ~ 109kHz.

Current Sensing / PWM Current Limiting

Peak-current-mode control is utilized in SG6741 to regulate output voltage and provide pulse-by-pulse current limiting. The switch current is detected by a sense resistor into the SENSE pin. The PWM duty cycle is determined by this current-sense signal and V_{FB}, the feedback voltage. When the voltage on the SENSE pin reaches around $V_{COMP} = (V_{FB}–1.2)/3.2$, the switch cycle is terminated immediately. V_{COMP} is internally clamped to a variable voltage around 0.85V for output power limit.

Leading-Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16.5V/10.5V. During start-up, the hold-up capacitor must be charged to 16.5V through the start-up resistor so that IC is enabled. The hold-up capacitor continues to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 10.5V during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during start-up.

Gate Output / Soft Driving

The SG6741 BiCMOS output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode to protect power MOSFET transistors against undesirable gate over-voltage. A soft driving waveform is implemented to minimize EMI.

Built-in Slope Compensation

The sensed voltage across the current-sense resistor is used for peak-current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillation. SG6741 inserts a synchronized positive-going ramp at every switching cycle.

Constant Output Power Limit

When the SENSE voltage, across the sense resistor R_S, reaches the threshold voltage around 0.9V, the output GATE drive is turned off after a small delay, t_{PD}. This delay introduces an additional current, proportional to $t_{PD} \bullet V_{IN} / L_P$. The delay is nearly constant, regardless of the input voltage V_{IN}. Higher input voltage results in a larger additional current and the output power limit is also higher than that under low input line voltage. To compensate this variation for wide AC input range, a sawtooth power-limiter is designed to solve the unequal power-limit problem. The power limiter is designed as a positive ramp signal and is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs.

V_{DD} Over-Voltage Protection

V_{DD} over-voltage protection has been built in to prevent damage due to abnormal conditions. Once the V_{DD} voltage is over the V_{DD} over-voltage protection voltage (V_{DD-OVP}), and lasts for $t_{D-VDDOVP}$, the PWM pulses is disabled until the V_{DD} voltage drops below the UVLO, then starts up again. Over-voltage conditions are usually caused by open feedback loops.

Limited Power Control

The FB voltage increases every time the output of the power supply is shorted or overloaded. If the FB voltage remains higher than a built-in threshold for longer than t_{D-OLP}, PWM output is turned off. As PWM output is turned off, the supply voltage V_{DD} begins decreasing.

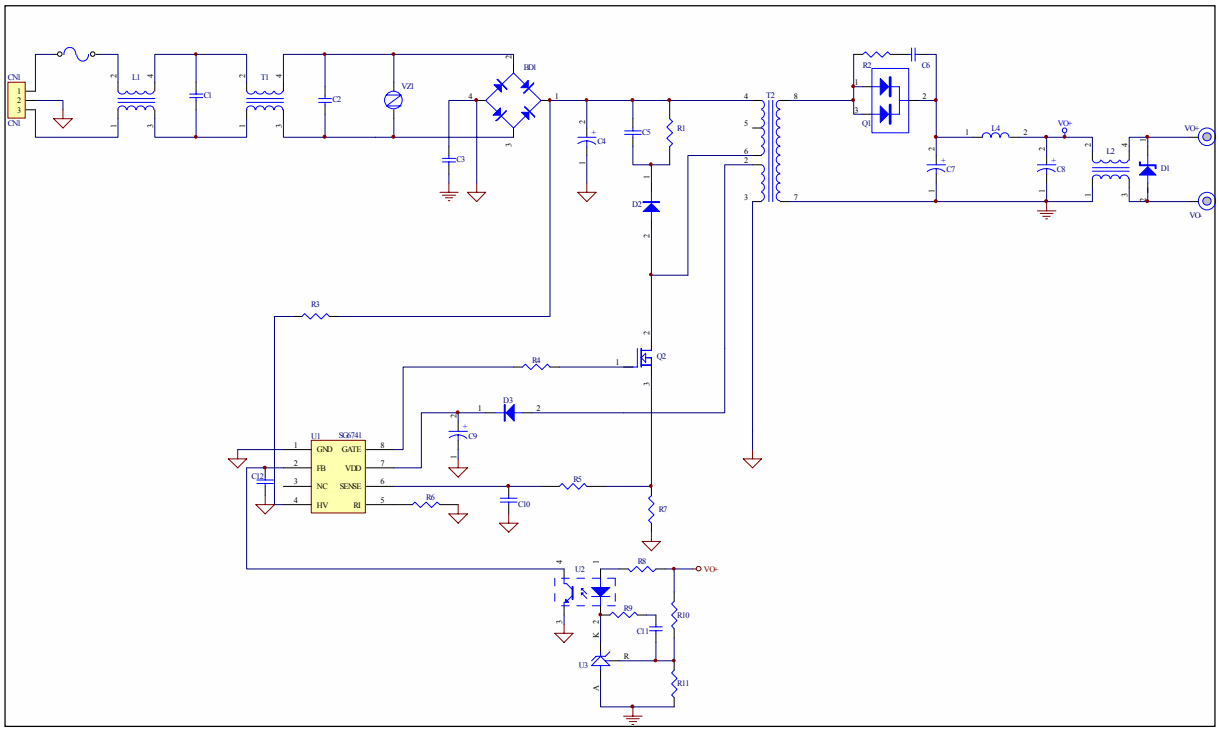
When V_{DD} goes below the turn-off threshold (eg, 10.5V) the controller totally shuts down. V_{DD} is charged up to the turn-on threshold voltage of 16V through the start-up resistor until PWM output is restarted. This protection is activated as long as the overloading condition persists. This prevents the power supply from overheating.

Noise Immunity

Noise on the current sense or control signal may cause significant pulse width jitter, particularly in the continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near to the SG6741, and increasing the power MO gate resistance improves performance.

REFERENCE CIRCUIT

CIRCUIT (12V/5A)

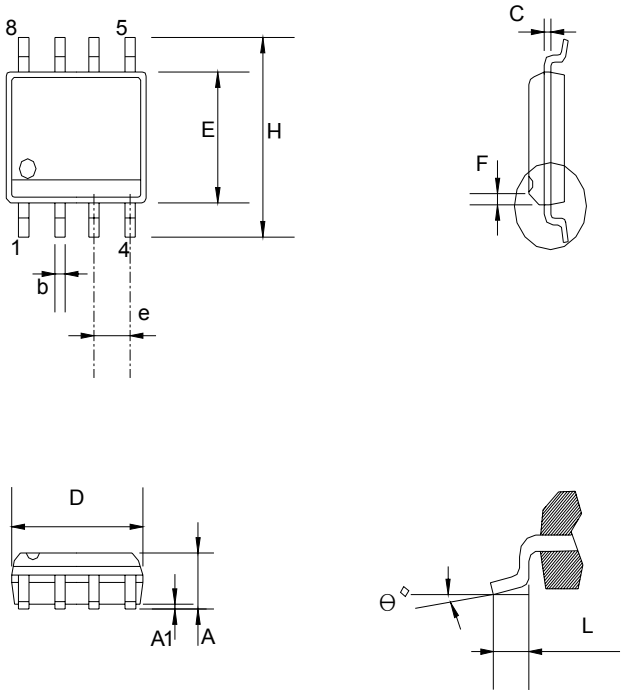


BOM

Reference	Component	Reference	Component
BD1	BD 4A/600V	Q2	MOS 7A/600V
C1	XC 0.68μF/300V	R1	R 100Kohm 1/2W
C2	XC 0.1μF/300V	R2	R 47ohm 1/4W
C3	YC 222pF/Y1	R3	R 100Kohm 1/2W
C4	EC 120μF/400V	R4	R 20ohm 1/8W
C5	CC 0.01μF/500V	R5	R 100ohm 1/8W
C6	CC 102pF/100V	R6	R 33Kohm 1/8W
C7	EC 1000μF/25V	R7	R 0.3ohm 2W
C8	EC 470μF/25V	R8	R 680ohm 1/8W
C9	EC 22μF/50V	R9	R 4.7Kohm 1/8W
C10	CC 470pF/50V	R10	R 150Kohm 1/8W
C11	CC 222pF/50V	R11	R 39Kohm 1/8W
C12	CC 103pF/50V	T1	10mH
D1	Zener Diode 15V 1/2W (option)	T2	600μH(PQ2620)
D2	BYV95C	U1	IC SG6741
D3	FR103	U2	IC PC817
F1	FUSE 4A/250V	U3	IC TL431
L1	900μH	VZ1	VZ 9G
Q1	STP20-100CT		

PACKAGE INFORMATION

8PINS-SOP(S)



Dimensions

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053		0.069
A1	0.101		0.254	0.004		0.010
b		0.406			0.016	
c		0.203			0.008	
D	4.648		4.978	0.183		0.196
E	3.810		3.987	0.150		0.157
e	1.016	1.270	1.524	0.040	0.050	0.060
F		0.381X45°			0.015X45°	
H	5.791		6.197	0.228		0.244
L	0.406		1.270	0.016		0.050
θ°	0°		8°	0°		8°

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MicroPak™
MillerDrive™
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Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
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the power franchise
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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