

## Features

- In-System Programmable PROMs for Configuration of Xilinx® FPGAs
- Low-Power Advanced CMOS NOR Flash Process
- Endurance of 20,000 Program/Erase Cycles
- Operation over Full Industrial Temperature Range (–40°C to +85°C)
- IEEE Standard 1149.1/1532 Boundary-Scan (JTAG) Support for Programming, Prototyping, and Testing
- JTAG Command Initiation of Standard FPGA Configuration
- Cascadable for Storing Longer or Multiple Bitstreams
- Dedicated Boundary-Scan (JTAG) I/O Power Supply ( $V_{CCJ}$ )
- I/O Pins Compatible with Voltage Levels Ranging From 1.5V to 3.3V
- Design Support Using the Xilinx Alliance ISE® and Foundation™ ISE Series Software Packages
- XCF01S/XCF02S/XCF04S
  - ◆ 3.3V Supply Voltage
  - ◆ Serial FPGA Configuration Interface (up to 33 MHz)
  - ◆ Available in Small-Footprint VO20 and VOG20 Packages
- XCF08P/XCF16P/XCF32P
  - ◆ 1.8V Supply Voltage
  - ◆ Serial or Parallel FPGA Configuration Interface (up to 33 MHz)
  - ◆ Available in Small-Footprint VO48, VOG48, FS48, and FSG48 Packages
  - ◆ Design Revision Technology Enables Storing and Accessing Multiple Design Revisions for Configuration
  - ◆ Built-In Data Decompressor Compatible with Xilinx Advanced Compression Technology

## Description

Xilinx introduces the Platform Flash series of in-system programmable configuration PROMs. Available in 1 to 32 Megabit (Mbit) densities, these PROMs provide an easy-to-use, cost-effective, and reprogrammable method for storing large Xilinx FPGA configuration bitstreams. The Platform Flash PROM series includes both the 3.3V XCFxxS PROM and the 1.8V XCFxxP PROM. The XCFxxS version includes 4-Mbit, 2-Mbit, and 1-Mbit PROMs that support Master

Serial and Slave Serial FPGA configuration modes (Figure 1, page 2). The XCFxxP version includes 32-Mbit, 16-Mbit, and 8-Mbit PROMs that support Master Serial, Slave Serial, Master SelectMAP, and Slave SelectMAP FPGA configuration modes (Figure 2, page 2). A summary of the Platform Flash PROM family members and supported features is shown in Table 1.

Table 1: Platform Flash PROM Features

| Device | Density | $V_{CCINT}$ | $V_{CCO}$ Range | $V_{CCJ}$ Range | Packages                 | Program In-system via JTAG | Serial Config. | Parallel Config. | Design Revisioning | Compression |
|--------|---------|-------------|-----------------|-----------------|--------------------------|----------------------------|----------------|------------------|--------------------|-------------|
| XCF01S | 1 Mbit  | 3.3V        | 1.8V – 3.3V     | 2.5V – 3.3V     | VO20/VOG20               | ✓                          | ✓              |                  |                    |             |
| XCF02S | 2 Mbit  | 3.3V        | 1.8V – 3.3V     | 2.5V – 3.3V     | VO20/VOG20               | ✓                          | ✓              |                  |                    |             |
| XCF04S | 4 Mbit  | 3.3V        | 1.8V – 3.3V     | 2.5V – 3.3V     | VO20/VOG20               | ✓                          | ✓              |                  |                    |             |
| XCF08P | 8 Mbit  | 1.8V        | 1.5V – 3.3V     | 2.5V – 3.3V     | VO48/VOG48<br>FS48/FSG48 | ✓                          | ✓              | ✓                | ✓                  | ✓           |
| XCF16P | 16 Mbit | 1.8V        | 1.5V – 3.3V     | 2.5V – 3.3V     | VO48/VOG48<br>FS48/FSG48 | ✓                          | ✓              | ✓                | ✓                  | ✓           |
| XCF32P | 32 Mbit | 1.8V        | 1.5V – 3.3V     | 2.5V – 3.3V     | VO48/VOG48<br>FS48/FSG48 | ✓                          | ✓              | ✓                | ✓                  | ✓           |

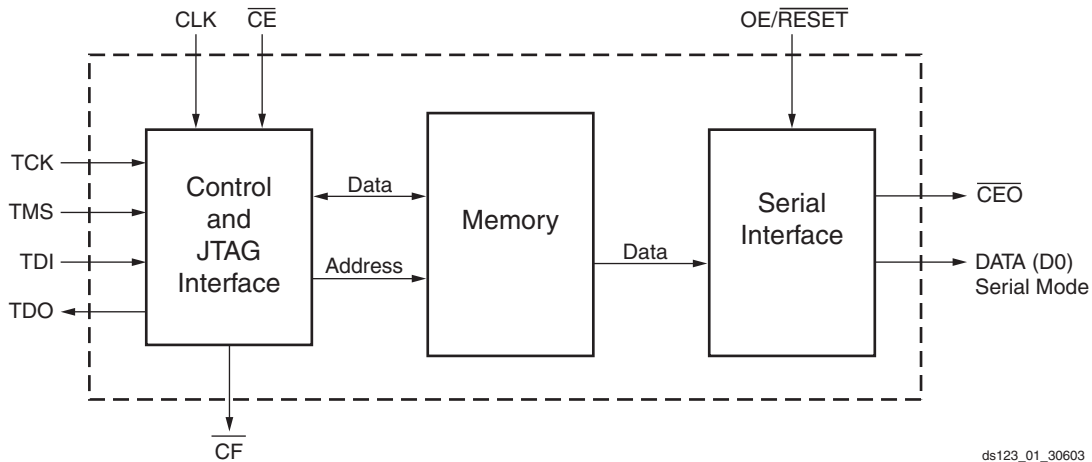


Figure 1: XCFxxS Platform Flash PROM Block Diagram

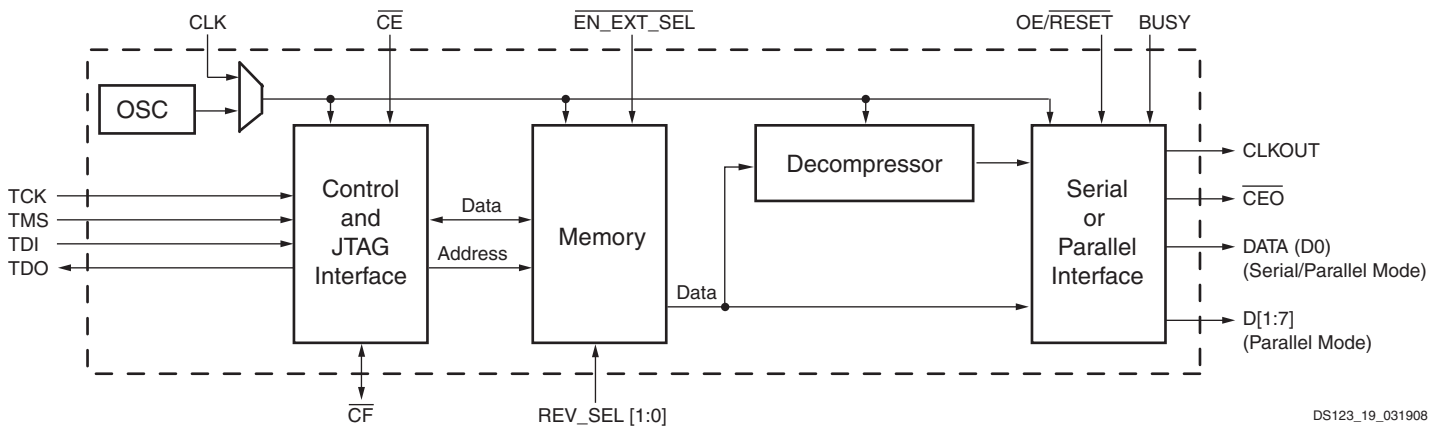


Figure 2: XCFxxP Platform Flash PROM Block Diagram

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. With  $\overline{CF}$  High, a short access time after  $\overline{CE}$  and OE are enabled, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. New data is available a short access time after each rising clock edge. The FPGA generates the appropriate number of clock pulses to complete the configuration.

When the FPGA is in Slave Serial mode, the PROM and the FPGA are both clocked by an external clock source, or optionally, for the XCFxxP PROM only, the PROM can be used to drive the FPGA's configuration clock.

The XCFxxP version of the Platform Flash PROM also supports Master SelectMAP and Slave SelectMAP (or Slave Parallel) FPGA configuration modes. When the FPGA is in Master SelectMAP mode, the FPGA generates a configuration clock that drives the PROM. When the FPGA is in Slave SelectMAP Mode, either an external oscillator generates the configuration clock that drives the PROM and the FPGA, or optionally, the XCFxxP PROM can be used to drive the FPGA's configuration clock. With BUSY Low and  $\overline{CF}$  High, after  $\overline{CE}$  and OE are enabled, data is available on the PROMs DATA (D0-D7) pins. New data is available a short access time after each rising clock edge. The data is clocked into the FPGA on the following rising edge of the

CCLK. A free-running oscillator can be used in the Slave Parallel/Slave SelectMAP mode.

The XCFxxP version of the Platform Flash PROM provides additional advanced features. A built-in data decompressor supports utilizing compressed PROM files, and design revisioning allows multiple design revisions to be stored on a single PROM or stored across several PROMs. For design revisioning, external pins or internal control bits are used to select the active design revision.

Multiple Platform Flash PROM devices can be cascaded to support the larger configuration files required when targeting larger FPGA devices or targeting multiple FPGAs daisy chained together. When utilizing the advanced features for the XCFxxP Platform Flash PROM, such as design revisioning, programming files which span cascaded PROM devices can only be created for cascaded chains containing only XCFxxP PROMs. If the advanced XCFxxP features are not enabled, then the cascaded chain can include both XCFxxP and XCFxxS PROMs.

The Platform Flash PROMs are compatible with all of the existing FPGA device families. A reference list of Xilinx FPGAs and the respective compatible Platform Flash PROMs is given in Table 2, page 3. A list of Platform Flash PROMs and their capacities is given in Table 3, page 4.

**Table 2: Xilinx FPGAs and Compatible Platform Flash PROMs**

| FPGA                                 | Configuration Bitstream | Platform Flash PROM <sup>(1)</sup>             |
|--------------------------------------|-------------------------|--|
| <b>Virtex<sup>®</sup>-5 LX FPGAs</b> |                         |  |
| XC5VLX30                             | 8,374,016               | XCF08P   |
| XC5VLX50                             | 12,556,672              | XCF16P   |
| XC5VLX85                             | 21,845,632              | XCF32P   |
| XC5VLX110                            | 29,124,608              | XCF32P   |
| XC5VLX155                            | 41,048,064              | XCF128X <sup>(4)</sup> or XCF32P+XCF08P        |
| XC5VLX220                            | 53,139,456              | XCF128X <sup>(4)</sup> or XCF32P+XCF32P        |
| XC5VLX330                            | 79,704,832              | XCF128X <sup>(4)</sup> or XCF32P+XCF32P+XCF16P |
| <b>Virtex-5 LXT FPGAs</b>            |                         |  |
| XC5VLX20T                            | 6,251,200               | XCF08P   |
| XC5VLX30T                            | 9,371,136               | XCF16P   |
| XC5VLX50T                            | 14,052,352              | XCF16P   |
| XC5VLX85T                            | 23,341,312              | XCF32P   |
| XC5VLX110T                           | 31,118,848              | XCF32P   |
| XC5VLX155T                           | 43,042,304              | XCF128X <sup>(4)</sup> or XCF32P+XCF16P        |
| XC5VLX220T                           | 55,133,696              | XCF128X <sup>(4)</sup> or XCF32P+XCF32P        |
| XC5VLX330T                           | 82,696,192              | XCF128X <sup>(4)</sup> or XCF32P+XCF32P+XCF16P |
| <b>Virtex-5 SXT FPGAs</b>            |                         |  |
| XC5VSX35T                            | 13,349,120              | XCF16P   |
| XC5VSX50T                            | 20,019,328              | XCF32P   |
| XC5VSX95T                            | 35,716,096              | XCF128X <sup>(4)</sup> or XCF32P+XCF08P        |
| XC5VSX240T                           | 79,610,368              | XCF128X <sup>(4)</sup> or XCF32P+XCF32P+XCF16P |
| <b>Virtex-5 FXT FPGAs</b>            |                         |  |
| XC5VFX30T                            | 13,517,056              | XCF16P   |
| XC5VFX70T                            | 27,025,408              | XCF32P   |
| XC5VFX100T                           | 39,389,696              | XCF128X <sup>(4)</sup> or XCF32P+XCF08P        |
| XC5VFX130T                           | 49,234,944              | XCF128X <sup>(4)</sup> or XCF32P+XCF16P        |
| XC5VFX200T                           | 70,856,704              | XCF128X <sup>(4)</sup> or XCF32P+XCF32P+XCF08P |
| <b>Virtex-4 LX FPGAs</b>             |                         |  |
| XC4VLX15                             | 4,765,568               | XCF08P   |
| XC4VLX25                             | 7,819,904               | XCF08P   |
| XC4VLX40                             | 12,259,712              | XCF16P   |
| XC4VLX60                             | 17,717,632              | XCF32P   |

**Table 2: Xilinx FPGAs and Compatible Platform Flash PROMs (Cont'd)**

| FPGA                                 | Configuration Bitstream | Platform Flash PROM <sup>(1)</sup> |
|--------------------------------------|-------------------------|------------------------------------|
| XC4VLX80                             | 23,291,008              | XCF32P                             |
| XC4VLX100                            | 30,711,680              | XCF32P                             |
| XC4VLX160                            | 40,347,008              | XCF32P+XCF08P                      |
| XC4VLX200                            | 51,367,808              | XCF32P+XCF32P                      |
| <b>Virtex-4 FX FPGAs</b>             |                         |                                    |
| XC4VFX12                             | 4,765,568               | XCF08P                             |
| XC4VFX20                             | 7,242,624               | XCF08P                             |
| XC4VFX40                             | 14,936,192              | XCF16P                             |
| XC4VFX60                             | 21,002,880              | XCF32P                             |
| XC4VFX100                            | 33,065,408              | XCF32P                             |
| XC4VFX140                            | 47,856,896              | XCF32P+XCF16P                      |
| <b>Virtex-4 SX FPGAs</b>             |                         |                                    |
| XC4VSX25                             | 9,147,648               | XCF16P                             |
| XC4VSX35                             | 13,700,288              | XCF16P                             |
| XC4VSX55                             | 22,749,184              | XCF32P                             |
| <b>Virtex-II Pro X FPGAs</b>         |                         |                                    |
| XC2VPX20                             | 8,214,560               | XCF08P                             |
| XC2VPX70                             | 26,098,976              | XCF32P                             |
| <b>Virtex-II Pro FPGAs</b>           |                         |                                    |
| XC2VP2                               | 1,305,376               | XCF02S                             |
| XC2VP4                               | 3,006,496               | XCF04S                             |
| XC2VP7                               | 4,485,408               | XCF08P                             |
| XC2VP20                              | 8,214,560               | XCF08P                             |
| XC2VP30                              | 11,589,920              | XCF16P                             |
| XC2VP40                              | 15,868,192              | XCF16P                             |
| XC2VP50                              | 19,021,344              | XCF32P                             |
| XC2VP70                              | 26,098,976              | XCF32P                             |
| XC2VP100                             | 34,292,768              | XCF32P <sup>(2)</sup>              |
| <b>Virtex-II FPGAs<sup>(3)</sup></b> |                         |                                    |
| XC2V40                               | 470,048                 | XCF01S                             |
| XC2V80                               | 732,576                 | XCF01S                             |
| XC2V250                              | 1,726,880               | XCF02S                             |
| XC2V500                              | 2,767,520               | XCF04S                             |
| XC2V1000                             | 4,089,504               | XCF04S                             |
| XC2V1500                             | 5,667,488               | XCF08P                             |
| XC2V2000                             | 7,501,472               | XCF08P                             |
| XC2V3000                             | 10,505,120              | XCF16P                             |
| XC2V4000                             | 15,673,248              | XCF16P                             |
| XC2V6000                             | 21,865,376              | XCF32P                             |
| XC2V8000                             | 29,081,504              | XCF32P                             |

**Table 2: Xilinx FPGAs and Compatible Platform Flash PROMs (Cont'd)**

| FPGA                                | Configuration Bitstream | Platform Flash PROM <sup>(1)</sup> |
|-------------------------------------|-------------------------|------------------------------------|
| <b>Virtex-E FPGAs</b>               |                         |                                    |
| XCV50E                              | 630,048                 | XCF01S                             |
| XCV100E                             | 863,840                 | XCF01S                             |
| XCV200E                             | 1,442,016               | XCF02S                             |
| XCV300E                             | 1,875,648               | XCF02S                             |
| XCV400E                             | 2,693,440               | XCF04S                             |
| XCV405E                             | 3,430,400               | XCF04S                             |
| XCV600E                             | 3,961,632               | XCF04S                             |
| XCV812E                             | 6,519,648               | XCF08P                             |
| XCV1000E                            | 6,587,520               | XCF08P                             |
| XCV1600E                            | 8,308,992               | XCF08P                             |
| XCV2000E                            | 10,159,648              | XCF16P                             |
| XCV2600E                            | 12,922,336              | XCF16P                             |
| XCV3200E                            | 16,283,712              | XCF16P                             |
| <b>Virtex FPGAs</b>                 |                         |                                    |
| XCV50                               | 559,200                 | XCF01S                             |
| XCV100                              | 781,216                 | XCF01S                             |
| XCV150                              | 1,040,096               | XCF01S                             |
| XCV200                              | 1,335,840               | XCF02S                             |
| XCV300                              | 1,751,808               | XCF02S                             |
| XCV400                              | 2,546,048               | XCF04S                             |
| XCV600                              | 3,607,968               | XCF04S                             |
| XCV800                              | 4,715,616               | XCF08P                             |
| XCV1000                             | 6,127,744               | XCF08P                             |
| <b>Spartan<sup>®</sup>-3A FPGAs</b> |                         |                                    |
| XC3S50A                             | 437,312                 | XCF01S                             |
| XC3S200A                            | 1,196,128               | XCF02S                             |
| XC3S400A                            | 1,886,560               | XCF02S                             |
| XC3S700A                            | 2,732,640               | XCF04S                             |
| XC3S1400A                           | 4,755,296               | XCF08P                             |
| <b>Spartan-3A DSP FPGAs</b>         |                         |                                    |
| XC3SD1800A                          | 8,197,280               | XCF08P                             |
| XC3SD3400A                          | 11,718,304              | XCF16P                             |
| <b>Spartan-3E FPGAs</b>             |                         |                                    |
| XC3S100E                            | 581,344                 | XCF01S                             |
| XC3S250E                            | 1,353,728               | XCF02S                             |
| XC3S500E                            | 2,270,208               | XCF04S                             |
| XC3S1200E                           | 3,841,184               | XCF04S                             |
| XC3S1600E                           | 5,969,696               | XCF08P                             |

**Table 2: Xilinx FPGAs and Compatible Platform Flash PROMs (Cont'd)**

| FPGA                     | Configuration Bitstream | Platform Flash PROM <sup>(1)</sup> |
|--------------------------|-------------------------|------------------------------------|
| <b>Spartan-3 FPGAs</b>   |                         |                                    |
| XC3S50                   | 439,264                 | XCF01S                             |
| XC3S200                  | 1,047,616               | XCF01S                             |
| XC3S400                  | 1,699,136               | XCF02S                             |
| XC3S1000                 | 3,223,488               | XCF04S                             |
| XC3S1500                 | 5,214,784               | XCF08P                             |
| XC3S2000                 | 7,673,024               | XCF08P                             |
| XC3S4000                 | 11,316,864              | XCF16P                             |
| XC3S5000                 | 13,271,936              | XCF16P                             |
| <b>Spartan-IIE FPGAs</b> |                         |                                    |
| XC2S50E                  | 630,048                 | XCF01S                             |
| XC2S100E                 | 863,840                 | XCF01S                             |
| XC2S150E                 | 1,134,496               | XCF02S                             |
| XC2S200E                 | 1,442,016               | XCF02S                             |
| XC2S300E                 | 1,875,648               | XCF02S                             |
| XC2S400E                 | 2,693,440               | XCF04S                             |
| XC2S600E                 | 3,961,632               | XCF04S                             |
| <b>Spartan-II FPGAs</b>  |                         |                                    |
| XC2S15                   | 197,696                 | XCF01S                             |
| XC2S30                   | 336,768                 | XCF01S                             |
| XC2S50                   | 559,200                 | XCF01S                             |
| XC2S100                  | 781,216                 | XCF01S                             |
| XC2S150                  | 1,040,096               | XCF01S                             |
| XC2S200                  | 1,335,840               | XCF02S                             |

**Notes:**

1. If design revisioning or other advanced feature support is required, the XCFxxP can be used as an alternative to the XCF01S, XCF02S, or XCF04S.
2. Assumes the Platform Flash XCFxxP PROM advanced compression feature or **BitGen -compress** option is used and the compression method successfully fits the bitstream within the suggested PROM.
3. The largest non-debug bitstream size is specified for each FPGA. Refer to the appropriate FPGA user guides for information on CONFIG STEPPING constraints or BitGen options (such as **-g FreezeDCI:Yes**) that affect bitstream size.
4. For information about the XCF128X, see [DS617](#), *Platform Flash XL High-Density Configuration and Storage Device*.

**Table 3: Platform Flash PROM Capacity**

| Platform Flash PROM | Configuration Bits | Platform Flash PROM | Configuration Bits |
|---------------------|--------------------|---------------------|--------------------|
| XCF01S              | 1,048,576          | XCF08P              | 8,388,608          |
| XCF02S              | 2,097,152          | XCF16P              | 16,777,216         |
| XCF04S              | 4,194,304          | XCF32P              | 33,554,432         |

## Programming

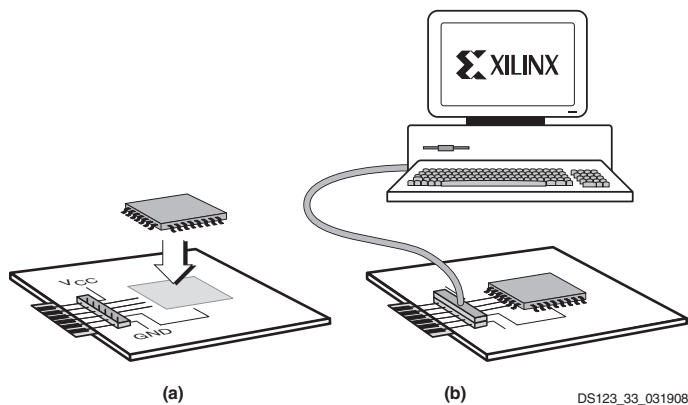
The Platform Flash PROM is a reprogrammable NOR flash device (refer "[Quality and Reliability Characteristics](#)," page 28 for the program/erase specifications).

Reprogramming requires an erase followed by a program operation. A verify operation is recommended after the program operation to validate the correct transfer of data from the programmer source to the Platform Flash PROM.

Several programming solutions are available.

### In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be daisy-chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in [Figure 3](#). In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The programming data sequence is delivered to the device using either Xilinx iMPACT software and a Xilinx download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format, including automatic test equipment. During in-system programming, the  $\overline{CEO}$  output is driven High. All other outputs are held in a high-impedance state or held at clamp levels during in-system programming. In-system programming is fully supported across the recommended operating voltage and temperature ranges.



**Figure 3: JTAG In-System Programming Operation**

(a) Solder Device to PCB

(b) Program Using Download Cable

Embedded, in-system programming reference designs, such as [XAPP058](#), *Xilinx In-System Programming Using an Embedded Microcontroller*, are available on the Xilinx web page for [PROM Programming and Data Storage Application Notes](#). See the [UG161](#), *Platform Flash PROM User Guide*, for an advanced update methodology that uses the Design Revisioning feature in the Platform Flash XCFxxP PROMs.

### OE/RESET

The 1/2/4 Mbit XCFxxS Platform Flash PROMs in-system programming algorithm results in issuance of an internal device reset that causes OE/RESET to pulse Low.

### External Programming

In traditional manufacturing environments, third-party device programmers can program Platform Flash PROMs with an initial memory image before the PROMs are assembled onto boards. Contact a preferred third-party programmer vendor for Platform Flash PROM support information. A sample list of third-party programmer vendors with Platform Flash PROM support is available on the Xilinx web page for [Third-Party Programmer Device Support](#).

Pre-programmed PROMs can be assembled onto boards using the typical soldering process guidelines in the [UG112](#), *Device Package User Guide*. A pre-programmed PROM's memory image can be updated after board assembly using an in-system programming solution.

### Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 20,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

See the [UG116](#), *Xilinx Device Reliability Report*, for device quality, reliability, and process node information.

## Design Security

The Xilinx in-system programmable Platform Flash PROM devices incorporate advanced data security features to fully protect the FPGA programming data against unauthorized reading via JTAG. The XCFxxP PROMs can also be programmed to prevent inadvertent writing via JTAG.

Table 4 and Table 5 show the security settings available for the XCFxxS PROM and XCFxxP PROM, respectively.

### Read Protection

The read protect security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. Read protection does not prevent write operations. For the XCFxxS PROM, the read protect security bit is set for the entire device, and resetting the read protect security bit requires erasing the entire device. For the XCFxxP PROM the read protect security bit can be set for individual design revisions, and resetting the read protect bit requires erasing the particular design revision.

### Write Protection

The XCFxxP PROM device also allows the user to write protect (or lock) a particular design revision or PROM option settings. Write protection helps to prevent an inadvertent JTAG instruction from modifying an area by write protecting the area and by locking the erase instruction. The write-protection setting can be cleared by erasing the protected area. However, an XSC\_UNLOCK instruction must first be issued to the XCFxxP PROM to unlock the ISC\_ERASE instruction. Refer to the XCFxxP PROM BSDL file for the XSC\_UNLOCK and ISC\_ERASE instructions.

**Caution!** The iMPACT software always issues a XSC\_UNLOCK when performing an Erase operation on an XCFxxP PROM and, thus, always unlocks the write protection.

Table 4: XCFxxS Device Data Security Options

| Read Protect    | Read/Verify Inhibited | Program Inhibited | Erase Inhibited |
|-----------------|-----------------------|-------------------|-----------------|
| Reset (default) |                       |                   |                 |
| Set             | ✓                     |                   |                 |

Table 5: XCFxxP Design Revision Data Security Options

| Read Protect    | Write Protect   | Read/Verify Inhibited | Program Inhibited | Erase Inhibited |
|-----------------|-----------------|-----------------------|-------------------|-----------------|
| Reset (default) | Reset (default) |                       |                   |                 |
| Reset (default) | Set             |                       | ✓                 | ✓               |
| Set             | Reset (default) | ✓                     |                   |                 |
| Set             | Set             | ✓                     | ✓                 | ✓               |



## IEEE 1149.1 Boundary-Scan (JTAG)

The Platform Flash PROM family is compatible with the IEEE 1149.1 Boundary-Scan standard and the IEEE 1532 in-system configuration standard. A Test Access Port (TAP) and registers are provided to support all required Boundary-Scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the Platform Flash PROM device. Table 6 lists the required and optional Boundary-Scan instructions supported in the

Platform Flash PROMs. Refer to the IEEE Std. 1149.1 specification for a complete description of Boundary-Scan architecture and the required and optional instructions.

**Caution!** The XCFxxP JTAG TAP pause states are not fully compliant with the JTAG 1149.1 specification. If a temporary pause of a JTAG shift operation is required, then stop the JTAG TCK clock and maintain the JTAG TAP within the JTAG Shift-IR or Shift-DR TAP state. Do not transition the XCFxxP JTAG TAP through the JTAG Pause-IR or Pause-DR TAP state to temporarily pause a JTAG shift operation.

Table 6: Platform Flash PROM Boundary-Scan Instructions

| Boundary-Scan Command                            | XCFxxS IR[7:0] (hex) | XCFxxP IR[15:0] (hex) | Instruction Description   |
|--|----------------------|-----------------------|---|
| <b>Required Instructions</b>                     |                      |                       |   |
| BYPASS   | FF                   | FFFF                  | Enables BYPASS  |
| SAMPLE/PRELOAD                                   | 01                   | 0001                  | Enables Boundary-Scan SAMPLE/PRELOAD operation  |
| EXTEST   | 00                   | 0000                  | Enables Boundary-Scan EXTEST operation  |
| <b>Optional Instructions</b>                     |                      |                       |   |
| CLAMP  | FA                   | 00FA                  | Enables Boundary-Scan CLAMP operation   |
| HIGHZ  | FC                   | 00FC                  | Places all outputs in high-impedance state simultaneously   |
| IDCODE   | FE                   | 00FE                  | Enables shifting out 32-bit IDCODE  |
| USERCODE   | FD                   | 00FD                  | Enables shifting out 32-bit USERCODE  |
| <b>Platform Flash PROM Specific Instructions</b> |                      |                       |   |
| CONFIG   | EE                   | 00EE                  | Initiates FPGA configuration by pulsing $\overline{CF}$ pin Low once. (For the XCFxxP this command also resets the selected design revision based on either the external REV_SEL[1:0] pins or on the internal design revision selection bits.) <sup>(1)</sup> |

### Notes:

- For more information see "Initiating FPGA Configuration," page 16.

## Instruction Register

The Instruction Register (IR) for the Platform Flash PROM is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI.

### XCFxxS Instruction Register (8 bits wide)

The Instruction Register (IR) for the XCFxxS PROM is eight bits wide and is connected between TDI and TDO during an instruction scan sequence. The detailed composition of the instruction capture pattern is illustrated in Table 7, page 8. The instruction capture pattern shifted out of the XCFxxS device includes IR[7:0]. IR[7:5] are reserved bits and are set to a logic 0. The ISC Status field, IR[4], contains logic 1 if the device is currently in In-System Configuration (ISC) mode; otherwise, it contains logic 0. The Security field, IR[3], contains logic 1 if the device has been programmed with the security option turned on; otherwise, it contains logic 0. IR[2] is unused, and is set to '0'. The remaining bits IR[1:0] are set to '01' as defined by IEEE Std. 1149.1.

### XCFxxP Instruction Register (16 bits wide)

The Instruction Register (IR) for the XCFxxP PROM is sixteen bits wide and is connected between TDI and TDO during an instruction scan sequence. The detailed composition of the instruction capture pattern is illustrated in Table 8, page 8.

The instruction capture pattern shifted out of the XCFxxP device includes IR[15:0]. IR[15:9] are reserved bits and are set to a logic 0. The ISC Error field, IR[8:7], contains a 10 when an ISC operation is a success; otherwise a 01 when an In-System Configuration (ISC) operation fails. The Erase/Program (ER/PROG) Error field, IR[6:5], contains a 10 when an erase or program operation is a success; otherwise a 01 when an erase or program operation fails. The Erase/Program (ER/PROG) Status field, IR[4], contains a logic 0 when the device is busy performing an erase or programming operation; otherwise, it contains a logic 1. The ISC Status field, IR[3], contains logic 1 if the device is currently in In-System Configuration (ISC) mode; otherwise, it contains logic 0. The DONE field, IR[2], contains logic 1 if the sampled design revision has been successfully programmed; otherwise, a logic 0 indicates incomplete programming. The remaining bits IR[1:0] are set to 01 as defined by IEEE Std. 1149.1.

**Table 7: XCFxxS Instruction Capture Values Loaded into IR as part of an Instruction Scan Sequence**

|       |          |            |          |       |         |       |
|-------|----------|------------|----------|-------|---------|-------|
| TDI → | IR[7:5]  | IR[4]      | IR[3]    | IR[2] | IR[1:0] | → TDO |
|       | Reserved | ISC Status | Security | 0     | 0 1     |       |

**Table 8: XCFxxP Instruction Capture Values Loaded into IR as part of an Instruction Scan Sequence**

|       |          |           |               |                |            |       |         |       |
|-------|----------|-----------|---------------|----------------|------------|-------|---------|-------|
| TDI → | IR[15:9] | IR[8:7]   | IR[6:5]       | IR[4]          | IR[3]      | IR[2] | IR[1:0] | → TDO |
|       | Reserved | ISC Error | ER/PROG Error | ER/PROG Status | ISC Status | DONE  | 0 1     |       |

## Boundary-Scan Register

The Boundary-Scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output pin on the Platform Flash PROM has two register stages which contribute to the Boundary-Scan register, while each input pin has only one register stage. The bidirectional pins have a total of three register stages which contribute to the Boundary-Scan register. For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the High-Z enable state of the output pin. For each input pin, a single register stage controls and observes the input state of the pin. The bidirectional pin combines the three bits, the input stage bit is first, followed by the output stage bit and finally the output enable stage bit. The output enable stage bit is closest to TDO.

See [Table 13, page 38](#) and [Table 14, page 40](#) for the Boundary-Scan bit order for all connected device pins, or see the appropriate BSDL file for the complete Boundary-Scan bit order description under the "attribute BOUNDARY\_REGISTER" section in the BSDL file. The bit assigned to Boundary-Scan cell 0 is the LSB in the Boundary-Scan register, and is the register bit closest to TDO.

## Identification Registers

### IDCODE Register

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32 bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG. [Table 9](#) lists the IDCODE register values for the Platform Flash PROMs.

The IDCODE register has the following binary format:

```
vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1
```

where

- v = the die version number
- f = the PROM family code
- a = the specific Platform Flash PROM product ID
- c = the Xilinx manufacturer's ID

The LSB of the IDCODE register is always read as logic 1 as defined by IEEE Std. 1149.1.

**Table 9: IDCODES Assigned to Platform Flash PROMs**

| Device | IDCODE <sup>(1)</sup> (hex) |
|--------|-----------------------------|
| XCF01S | <v>5044093                  |
| XCF02S | <v>5045093                  |
| XCF04S | <v>5046093                  |
| XCF08P | <v>5057093                  |
| XCF16P | <v>5058093                  |
| XCF32P | <v>5059093                  |

#### Notes:

- The <v> in the IDCODE field represents the device's revision code (in hex) and can vary.

### USERCODE Register

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the Platform Flash PROM. If the device is blank or was not loaded during programming, the USERCODE register contains FFFFFFFFh.

### Customer Code Register

For the XCFxxP Platform Flash PROM, in addition to the USERCODE, a unique 32-byte Customer Code can be assigned to each design revision enabled for the PROM. The Customer Code is set during programming, and is typically used to supply information about the design revision contents. A private JTAG instruction is required to read the Customer Code. If the PROM is blank, or the Customer Code for the selected design revision was not loaded during programming, or if the particular design revision is erased, the Customer Code contains all ones.



## Platform Flash PROM TAP Characteristics

The Platform Flash PROM family performs both in-system programming and IEEE 1149.1 Boundary-Scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the Platform Flash PROM TAP are described as follows.

### TAP Timing

Figure 4 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both Boundary-Scan and ISP operations.

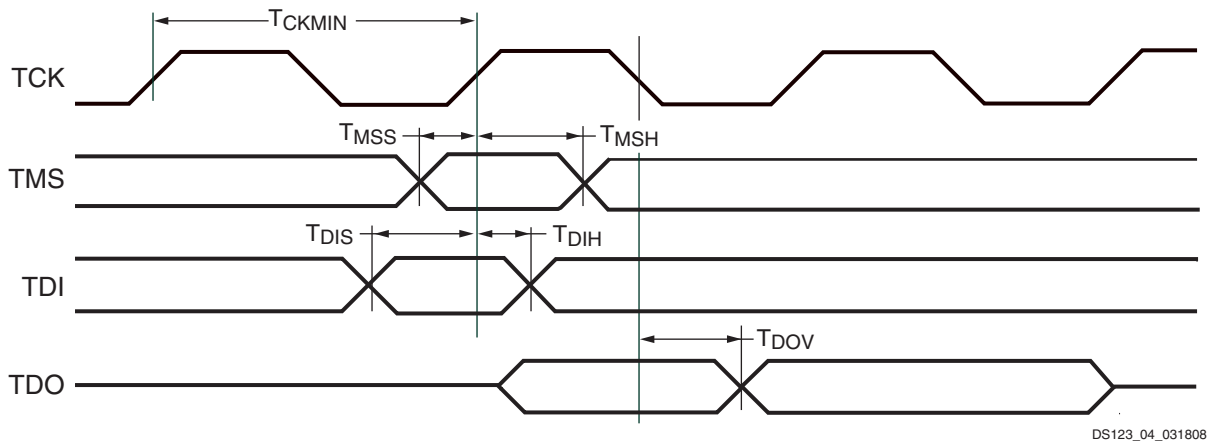


Figure 4: Test Access Port Timing

### TAP AC Parameters

Table 10 shows the timing parameters for the TAP waveforms shown in Figure 4.

Table 10: Test Access Port Timing Parameters

| Symbol      | Description  | Min | Max | Units |
|-------------|--|-----|-----|-------|
| $T_{CKMIN}$ | TCK minimum clock period when $V_{CCJ} = 2.5V$ or $3.3V$ | 67  | –   | ns    |
| $T_{MSS}$   | TMS setup time when $V_{CCJ} = 2.5V$ or $3.3V$           | 8   | –   | ns    |
| $T_{MSH}$   | TMS hold time when $V_{CCJ} = 2.5V$ or $3.3V$            | 25  | –   | ns    |
| $T_{DIS}$   | TDI setup time when $V_{CCJ} = 2.5V$ or $3.3V$           | 8   | –   | ns    |
| $T_{DIH}$   | TDI hold time when $V_{CCJ} = 2.5V$ or $3.3V$            | 25  | –   | ns    |
| $T_{DOV}$   | TDO valid delay when $V_{CCJ} = 2.5V$ or $3.3V$          | –   | 22  | ns    |

## Additional Features for the XCFxxP

### Internal Oscillator

The 8/16/32 Mbit XCFxxP Platform Flash PROMs include an optional internal oscillator which can be used to drive the CLKOUT and DATA pins on FPGA configuration interface. The internal oscillator can be enabled when programming the PROM, and the oscillator can be set to either the default frequency or to a slower frequency ("[XCFxxP PROM as Configuration Master with Internal Oscillator as Clock Source](#)," page 35).

### CLKOUT

The 8/16/32 Mbit XCFxxP Platform Flash PROMs include the programmable option to enable the CLKOUT signal which allows the PROM to provide a source synchronous clock aligned to the data on the configuration interface. The CLKOUT signal is derived from one of two clock sources: the CLK input pin or the internal oscillator. The input clock source is selected during the PROM programming sequence. Output data is available on the rising edge of CLKOUT.

The CLKOUT signal is enabled during programming, and is active when  $\overline{CE}$  is Low and  $OE/\overline{RESET}$  is High. On  $\overline{CE}$  rising edge transition, if  $OE/\overline{RESET}$  is High and the PROM terminal count has not been reached, then CLKOUT remains active for an additional eight clock cycles before being disabled. On a  $OE/\overline{RESET}$  falling edge transition, CLKOUT is immediately disabled. When disabled, the CLKOUT pin is put into a high-impedance state and should be pulled High externally to provide a known state.

When cascading Platform Flash PROMs with CLKOUT enabled, after completing its data transfer, the first PROM disables CLKOUT and drives the  $\overline{CEO}$  pin enabling the next PROM in the PROM chain. The next PROM begins driving the CLKOUT signal once that PROM is enabled and data is available for transfer.

During high-speed parallel configuration without compression, the FPGA drives the BUSY signal on the configuration interface. When BUSY is asserted High, the PROMs internal address counter stops incrementing, and the current data value is held on the data outputs. While BUSY is High, the PROM continues driving the CLKOUT signal to the FPGA, clocking the FPGA's configuration logic. When the FPGA deasserts BUSY, indicating that it is ready to receive additional configuration data, the PROM begins driving new data onto the configuration interface.

### Decompression

The 8/16/32 Mbit XCFxxP Platform Flash PROMs include a built-in data decompressor compatible with Xilinx advanced compression technology. Compressed Platform Flash PROM files are created from the target FPGA bitstream(s) using the iMPACT software. Only Slave Serial and Slave SelectMAP (parallel) configuration modes are supported for

FPGA configuration when using a XCFxxP PROM programmed with a compressed bitstream. Compression rates vary depending on several factors, including the target device family and the target design contents.

The decompression option is enabled during the PROM programming sequence. The PROM decompresses the stored data before driving both clock and data onto the FPGA's configuration interface. If Decompression is enabled, then the Platform Flash clock output pin (CLKOUT) must be used as the clock signal for the configuration interface, driving the target FPGA's configuration clock input pin (CCLK). Either the PROM's CLK input pin or the internal oscillator must be selected as the source for CLKOUT. Any target FPGA connected to the PROM must operate as slave in the configuration chain, with the configuration mode set to Slave Serial mode or Slave SelectMap (parallel) mode.

When decompression is enabled, the CLKOUT signal becomes a controlled clock output with a reduced maximum frequency. When decompressed data is not ready, the CLKOUT pin is put into a high-Z state and must be pulled High externally to provide a known state.

The BUSY input is automatically disabled when decompression is enabled.

See the "Decompression Setups" section in the *Platform Flash PROM User Guide* for setup details.

### Design Revisioning

Design Revisioning allows the user to create up to four unique design revisions on a single PROM or stored across multiple cascaded PROMs. Design Revisioning is supported for the 8/16/32 Mbit XCFxxP Platform Flash PROMs in both serial and parallel modes. Design Revisioning can be used with compressed PROM files, and also when the CLKOUT feature is enabled. The PROM programming files along with the revision information files (.cfi) are created using the iMPACT software. The .cfi file is required to enable design revision programming in iMPACT.

A single design revision is composed of from 1 to  $n$  8-Mbit memory blocks. If a single design revision contains less than 8 Mbits of data, then the remaining space is padded with all ones. A larger design revision can span several 8-Mbit memory blocks, and any space remaining in the last 8-Mbit memory block is padded with all ones.

- A single 32-Mbit PROM contains four 8-Mbit memory blocks, and can therefore store up to four separate design revisions: one 32-Mbit design revision, two 16-Mbit design revisions, three 8-Mbit design revisions, four 8-Mbit design revisions, and so on.
- Because of the 8-Mbit minimum size requirement for each revision, a single 16-Mbit PROM can only store

up to two separate design revisions: one 16-Mbit design revision, one 8-Mbit design revision, or two 8-Mbit design revisions.

- A single 8-Mbit PROM can store only one 8-Mbit design revision.

Larger design revisions can be split over several cascaded PROMs. For example, two 32-Mbit PROMs can store up to four separate design revisions: one 64-Mbit design revision, two 32-Mbit design revisions, three 16-Mbit design revisions, four 16-Mbit design revisions, and so on. When cascading one 16-Mbit PROM and one 8-Mbit PROM, there are 24 Mbits of available space, and therefore up to three separate design revisions can be stored: one 24-Mbit design revision, two 8-Mbit design revisions, or three 8-Mbit design revisions.

See [Figure 5](#) for a few basic examples of how multiple revisions can be stored. The design revision partitioning is handled automatically during file generation in iMPACT.

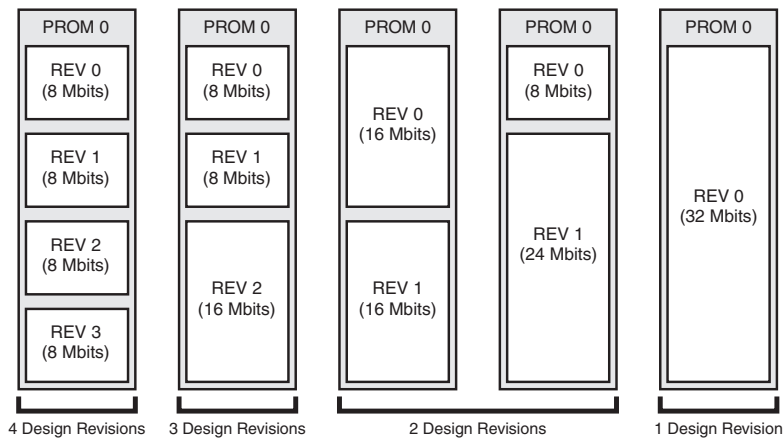
During the PROM file creation, each design revision is assigned a revision number:

Revision 0 = '00'  
Revision 1 = '01'  
Revision 2 = '10'  
Revision 3 = '11'

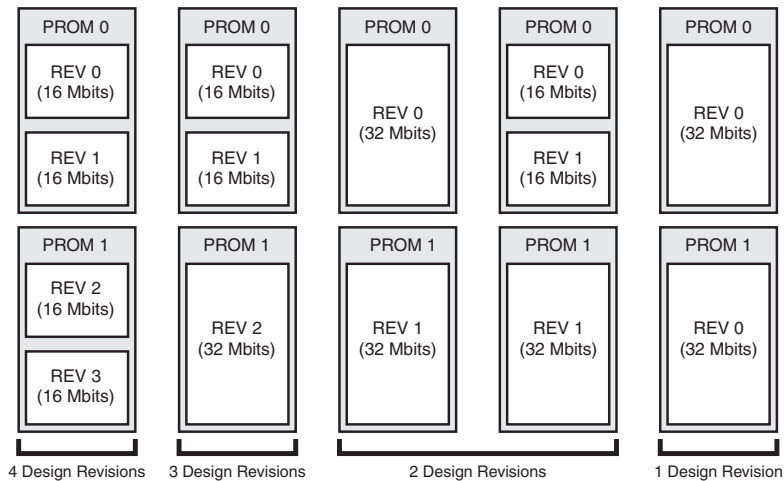
After programming the Platform Flash PROM with a set of design revisions, a particular design revision can be selected using the external REV\_SEL[1:0] pins or using the internal programmable design revision control bits. The EN\_EXT\_SEL pin determines if the external pins or internal bits are used to select the design revision. When EN\_EXT\_SEL is Low, design revision selection is controlled by the external Revision Select pins, REV\_SEL[1:0]. When EN\_EXT\_SEL is High, design revision selection is controlled by the internal programmable Revision Select control bits. During power up, the design revision selection inputs (pins or control bits) are sampled internally. After power up, the design revision selection inputs are sampled again when any of the following events occur:

- On the rising edge of  $\overline{CE}$ .
- On the falling edge of OE/ $\overline{RESET}$  (when  $\overline{CE}$  is Low).
- On the rising edge of  $\overline{CF}$  (when  $\overline{CE}$  is Low).
- When reconfiguration is initiated by using the JTAG CONFIG instruction.

The data from the selected design revision is then presented on the FPGA configuration interface.



(a) Design Revision storage examples for a single XCF32P PROM



(b) Design Revision storage examples spanning two XCF32P PROMs

ds123\_20\_102103

Figure 5: Design Revision Storage Examples

## PROM to FPGA Configuration Mode and Connections Summary

The FPGA's I/O, logical functions, and internal interconnections are established by the configuration data contained in the FPGA's bitstream. The bitstream is loaded into the FPGA either automatically upon power up, or on command, depending on the state of the FPGA's mode pins. Xilinx Platform Flash PROMs are designed to download directly to the FPGA configuration interface. FPGA configuration modes which are supported by the XCFxxS Platform Flash PROMs include: Master Serial and Slave Serial. FPGA configuration modes which are supported by the XCFxxP Platform Flash PROMs include: Master Serial, Slave Serial, Master SelectMAP, and Slave SelectMAP. Below is a short summary of the supported FPGA configuration modes. See the respective FPGA data sheet for device configuration details, including which configuration modes are supported by the targeted FPGA device.

### FPGA Master Serial Mode

In Master Serial mode, the FPGA automatically loads the configuration bitstream in bit-serial form from external memory synchronized by the configuration clock (CCLK) generated by the FPGA. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Master Serial configuration mode. Master Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines (INIT and DONE) are required to configure an FPGA. Data from the PROM is read out sequentially on a single data line (DIN), accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The serial bitstream data must be set up at the FPGA's DIN input pin a short time before each rising edge of the FPGA's internally generated CCLK signal.

Typically, a wide range of frequencies can be selected for the FPGA's internally generated CCLK which always starts at a slow default frequency. The FPGA's bitstream contains configuration bits which can switch CCLK to a higher frequency for the remainder of the Master Serial configuration sequence. The desired CCLK frequency is selected during bitstream generation.

Connecting the FPGA device to the configuration PROM for Master Serial Configuration Mode ([Figure 6, page 17](#)):

- The DATA output of the PROM(s) drive the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The  $\overline{CEO}$  output of a PROM drives the  $\overline{CE}$  input of the next PROM in a daisy chain (if any).
- The OE/ $\overline{RESET}$  pins of all PROMs are connected to the INIT\_B (or INIT) pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.

- The PROM  $\overline{CE}$  input can be driven from the DONE pin. The  $\overline{CE}$  input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded.  $\overline{CE}$  can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary  $I_{CC}$  active supply current ("[DC Characteristics Over Operating Conditions](#)," page 29).
- The PROM  $\overline{CF}$  pin is typically connected to the FPGA's PROG\_B (or  $\overline{PROGRAM}$ ) input. For the XCFxxP only, the  $\overline{CF}$  pin is a bidirectional pin. If the XCFxxP  $\overline{CF}$  pin is not connected to the FPGA's PROG\_B (or  $\overline{PROGRAM}$ ) input, then the pin should be tied High.

### FPGA Slave Serial Mode

In Slave Serial mode, the FPGA loads the configuration bitstream in bit-serial form from external memory synchronized by an externally supplied clock. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Slave Serial configuration mode. Slave Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines (INIT and DONE) are required to configure an FPGA. Data from the PROM is read out sequentially on a single data line (DIN), accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The serial bitstream data must be set up at the FPGA's DIN input pin a short time before each rising edge of the externally provided CCLK.

Connecting the FPGA device to the configuration PROM for Slave Serial Configuration Mode ([Figure 7, page 18](#)):

- The DATA output of the PROM(s) drive the DIN input of the lead FPGA device.
- The PROM CLKOUT (for XCFxxP only) or an external clock source drives the FPGA's CCLK input.
- The  $\overline{CEO}$  output of a PROM drives the  $\overline{CE}$  input of the next PROM in a daisy chain (if any).
- The OE/ $\overline{RESET}$  pins of all PROMs are connected to the INIT\_B (or INIT) pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM  $\overline{CE}$  input can be driven from the DONE pin. The  $\overline{CE}$  input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded.  $\overline{CE}$  can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary  $I_{CC}$  active supply current ("[DC Characteristics Over Operating Conditions](#)," page 29).
- The PROM  $\overline{CF}$  pin is typically connected to the FPGA's PROG\_B (or  $\overline{PROGRAM}$ ) input. For the XCFxxP only, the  $\overline{CF}$  pin is a bidirectional pin. If the XCFxxP  $\overline{CF}$  pin is not connected to the FPGA's PROG\_B (or  $\overline{PROGRAM}$ ) input, then the pin should be tied High.



## Serial Daisy Chain

Multiple FPGAs can be daisy-chained for serial configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally to the FPGA's DOUT pin. Typically the data on the DOUT pin changes on the falling edge of CCLK, although for some devices the DOUT pin changes on the rising edge of CCLK. Consult the respective device data sheets for detailed information on a particular FPGA device. For clocking the daisy-chained configuration, either the first FPGA in the chain can be set to Master Serial, generating the CCLK, with the remaining devices set to Slave Serial (Figure 8, page 19), or all the FPGA devices can be set to Slave Serial and an externally generated clock can be used to drive the FPGA's configuration interface (Figure 7, page 18 or Figure 12, page 23).

## FPGA Master SelectMAP (Parallel) Mode (XCFxxP PROM Only)

In Master SelectMAP mode, byte-wide data is written into the FPGA, typically with a BUSY flag controlling the flow of data, synchronized by the configuration clock (CCLK) generated by the FPGA. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Master SelectMAP configuration mode. The configuration interface typically requires a parallel data bus, a clock line, and two control lines (INIT and DONE). In addition, the FPGA's Chip Select, Write, and BUSY pins must be correctly controlled or monitored to enable SelectMAP configuration. The configuration data is read from the PROM byte by byte on pins [D0..D7], accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The bitstream data must be set up at the FPGA's [D0..D7] input pins a short time before each rising edge of the FPGA's internally generated CCLK signal. If BUSY is asserted (High) by the FPGA, the configuration data must be held until BUSY goes Low. The FPGA's active-Low Chip Select ( $\overline{CS}$  or CS\_B) and active-Low Write ( $\overline{WRITE}$  or RDWR\_B) signals must be tied to ground to enable the FPGA's SelectMAP configuration process.

The Master SelectMAP configuration interface is clocked by the FPGA's internal oscillator. Typically, a wide range of frequencies can be selected for the internally generated CCLK which always starts at a slow default frequency. The FPGA's bitstream contains configuration bits which can switch CCLK to a higher frequency for the remainder of the Master SelectMAP configuration sequence. The desired CCLK frequency is selected during bitstream generation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained using the persist option.

Connecting the FPGA device to the configuration PROM for Master SelectMAP (Parallel) Configuration Mode (Figure 9, page 20):

- The DATA outputs of the PROM(s) drive the [D0..D7] input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The  $\overline{CEO}$  output of a PROM drives the  $\overline{CE}$  input of the next PROM in a daisy chain (if any).
- The OE/ $\overline{RESET}$  pins of all PROMs are connected to the INIT\_B pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM  $\overline{CE}$  input can be driven from the DONE pin. The  $\overline{CE}$  input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded.  $\overline{CE}$  can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary  $I_{CC}$  active supply current ("DC Characteristics Over Operating Conditions," page 29).
- For high-frequency parallel configuration, the BUSY pins of all PROMs are connected to the FPGA's BUSY output (when the FPGA has a BUSY pin and when the use of the FPGA BUSY pin is required). This connection assures that the next data transition for the PROM is delayed until the FPGA is ready for the next configuration data byte. For FPGA BUSY pin requirements, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- The PROM  $\overline{CF}$  pin is typically connected to the FPGA's PROG\_B (or PROGRAM) input. For the XCFxxP only, the  $\overline{CF}$  pin is a bidirectional pin. If the XCFxxP  $\overline{CF}$  pin is not connected to the FPGA's PROG\_B (or PROGRAM) input, then the pin should be tied High.

## FPGA Slave SelectMAP (Parallel) Mode (XCFxxP PROM Only)

In Slave SelectMAP mode, byte-wide data is written into the FPGA, typically with a BUSY flag controlling the flow of data, synchronized by an externally supplied configuration clock (CCLK). Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Slave SelectMAP configuration mode. The configuration interface typically requires a parallel data bus, a clock line, and two control lines (INIT and DONE). In addition, the FPGA's Chip Select, Write, and BUSY pins must be correctly controlled or monitored to enable SelectMAP configuration. The configuration data is read from the PROM byte by byte on pins [D0..D7], accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The bitstream data must be set up at the FPGA's [D0..D7] input pins a short time before each rising edge of the provided

CCLK. If BUSY is asserted (High) by the FPGA, the configuration data must be held until BUSY goes Low. The FPGA's active-Low Chip Select ( $\overline{CS}$  or CS\_B) and active-Low Write ( $\overline{WRITE}$  or RDWR\_B) signals must be tied to ground to enable the FPGA's SelectMAP configuration process.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained using the persist option.

Connecting the FPGA device to the configuration PROM for Slave SelectMAP (Parallel) Configuration Mode (Figure 10, page 21):

- The DATA outputs of the PROM(s) drives the [D0..D7] inputs of the lead FPGA device.
- The PROM CLKOUT (for XCFxxP only) or an external clock source drives the FPGA's CCLK input.
- The  $\overline{CEO}$  output of a PROM drives the  $\overline{CE}$  input of the next PROM in a daisy chain (if any).
- The OE/ $\overline{RESET}$  pins of all PROMs are connected to the INIT\_B pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM  $\overline{CE}$  input can be driven from the DONE pin. The  $\overline{CE}$  input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded.  $\overline{CE}$  can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary  $I_{CC}$  active supply current ("DC Characteristics Over Operating Conditions," page 29).
- For high-frequency parallel configuration, the BUSY pins of all PROMs are connected to the FPGA's BUSY output (when the FPGA has a BUSY pin and when the use of the FPGA BUSY pin is required). This connection assures that the next data transition for the PROM is delayed until the FPGA is ready for the next configuration data byte. For FPGA BUSY pin requirements, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- The PROM  $\overline{CF}$  pin is typically connected to the FPGA's PROG\_B (or PROGRAM) input. For the XCFxxP only, the  $\overline{CF}$  pin is a bidirectional pin. If the XCFxxP  $\overline{CF}$  pin is not connected to the FPGA's PROG\_B (or PROGRAM) input, then the pin should be tied High.

## FPGA SelectMAP (Parallel) Device Chaining (XCFxxP PROM Only)

Multiple Virtex-II FPGAs can be configured using the SelectMAP mode, and be made to start up simultaneously. To configure multiple devices in this way, wire the individual CCLK, DONE, INIT, Data ([D0..D7]), Write ( $\overline{WRITE}$  or RDWR\_B), and BUSY pins of all the devices in parallel. If all

devices are to be configured with the same bitstream, readback is not being used, and the CCLK frequency selected does not require the use of the BUSY signal, the CS\_B pins can be connected to a common line so all of the devices are configured simultaneously (Figure 10).

With additional control logic, the individual devices can be loaded separately by asserting the CS\_B pin of each device in turn and then enabling the appropriate configuration data. The PROM can also store the individual bitstreams for each FPGA for SelectMAP configuration in separate design revisions. When design revisioning is utilized, additional control logic can be used to select the appropriate bitstream by asserting the  $\overline{EN\_EXT\_SEL}$  pin, and using the REV\_SEL[1:0] pins to select the required bitstream, while asserting the CS\_B pin for the FPGA the bitstream is targeting (Figure 13, page 24).

For clocking the parallel configuration chain, either the first FPGA in the chain can be set to Master SelectMAP, generating the CCLK, with the remaining devices set to Slave SelectMAP, or all the FPGA devices can be set to Slave SelectMAP and an externally generated clock can be used to drive the configuration interface. Again, the respective device data sheets should be consulted for detailed information on a particular FPGA device, including which configuration modes are supported by the targeted FPGA device.

## Cascading Configuration PROMs

When configuring multiple FPGAs in a serial daisy chain, configuring multiple FPGAs in a SelectMAP parallel chain, or configuring a single FPGA requiring a larger configuration bitstream, cascaded PROMs provide additional memory (Figure 8, page 19, Figure 11, page 22, Figure 12, page 23, and Figure 12, page 23). Multiple Platform Flash PROMs can be concatenated by using the  $\overline{CEO}$  output to drive the  $\overline{CE}$  input of the downstream device. The clock signal and the data outputs of all Platform Flash PROMs in the chain are interconnected. After the last data from the first PROM is read, the first PROM asserts its  $\overline{CEO}$  output Low and drives its outputs to a high-impedance state. The second PROM recognizes the Low level on its  $\overline{CE}$  input and immediately enables its outputs.

After configuration is complete, address counters of all cascaded PROMs are reset if the PROM OE/ $\overline{RESET}$  pin goes Low or  $\overline{CE}$  goes High.

When utilizing the advanced features for the XCFxxP Platform Flash PROM, including the clock output (CLKOUT) option, decompression option, or design revisioning, programming files which span cascaded PROM devices can only be created for cascaded chains containing only XCFxxP PROMs. If the advanced features are not used, then cascaded PROM chains can contain both XCFxxP and XCFxxS PROMs.

## Initiating FPGA Configuration

The options for initiating FPGA configuration via the Platform Flash PROM include:

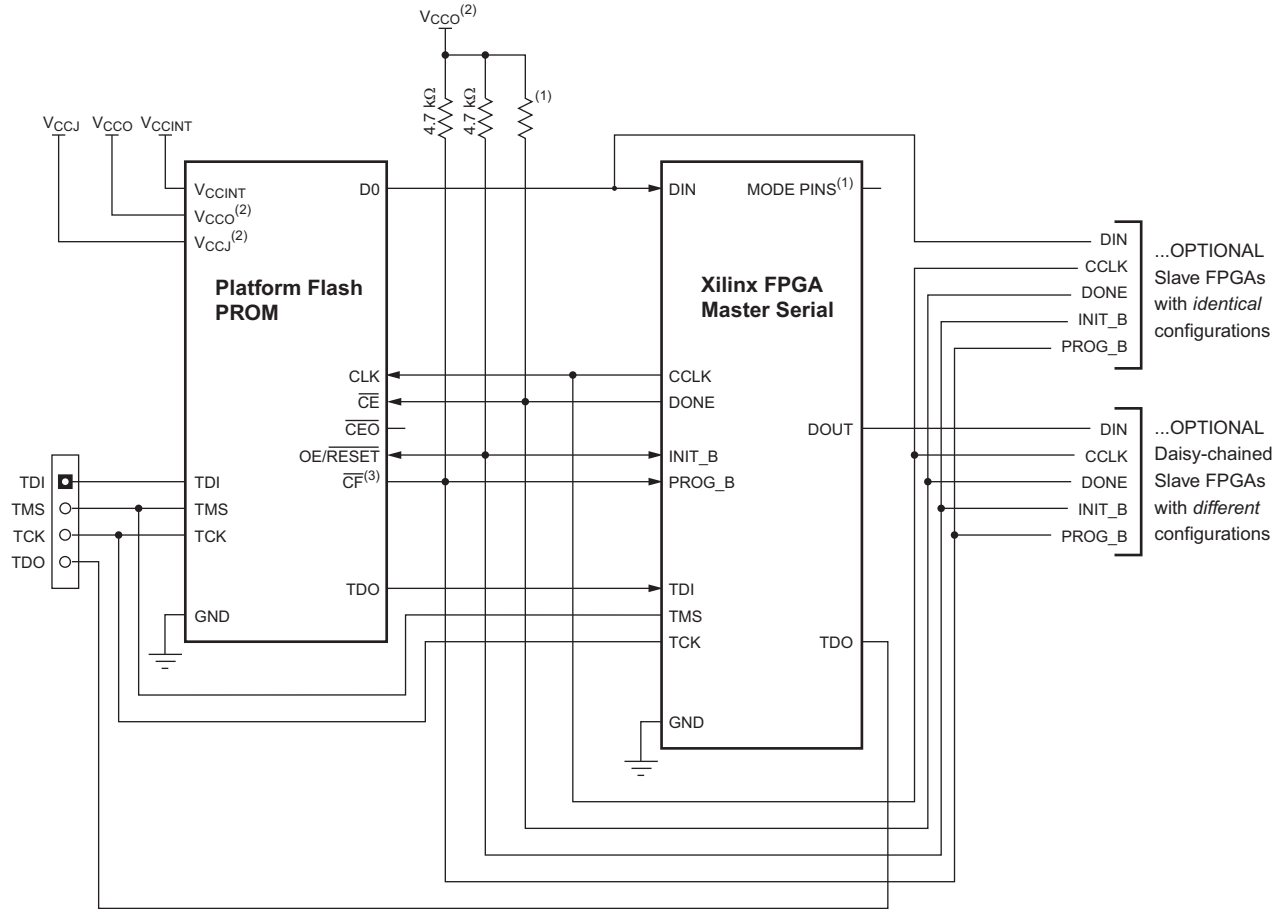
- Automatic configuration on power up
- Applying an external PROG\_B (or  $\overline{\text{PROGRAM}}$ ) pulse
- Applying the JTAG CONFIG instruction

Following the FPGA's power-on sequence or the assertion of the PROG\_B (or  $\overline{\text{PROGRAM}}$ ) pin the FPGA's configuration memory is cleared, the configuration mode is selected, and the FPGA is ready to accept a new configuration bitstream. The FPGA's PROG\_B pin can be controlled by an external source, or alternatively, the Platform Flash PROMs incorporate a  $\overline{\text{CF}}$  pin that can be tied to the FPGA's PROG\_B pin. Executing the CONFIG instruction through JTAG pulses the  $\overline{\text{CF}}$  output Low once for 300-500 ns, resetting the FPGA and initiating configuration.

The iMPACT software can issue the JTAG CONFIG command to initiate FPGA configuration by setting the "Load FPGA" option.

When using the XCFxxP Platform Flash PROM with design revisioning enabled, the  $\overline{\text{CF}}$  pin should always be connected to the PROG\_B (or  $\overline{\text{PROGRAM}}$ ) pin on the FPGA to ensure that the current design revision selection is sampled when the FPGA is reset. The XCFxxP PROM samples the current design revision selection from the external REV\_SEL pins or the internal programmable Revision Select bits on the rising edge of  $\overline{\text{CF}}$ . When the JTAG CONFIG command is executed, the XCFxxP samples the new design revision selection before initiating the FPGA configuration sequence. When using the XCFxxP Platform Flash PROM without design revisioning, if the  $\overline{\text{CF}}$  pin is not connected to the FPGA PROG\_B (or  $\overline{\text{PROGRAM}}$ ) pin, then the XCFxxP  $\overline{\text{CF}}$  pin must be tied High.

## Configuration PROM-to-FPGA Device Interface Connection Diagrams

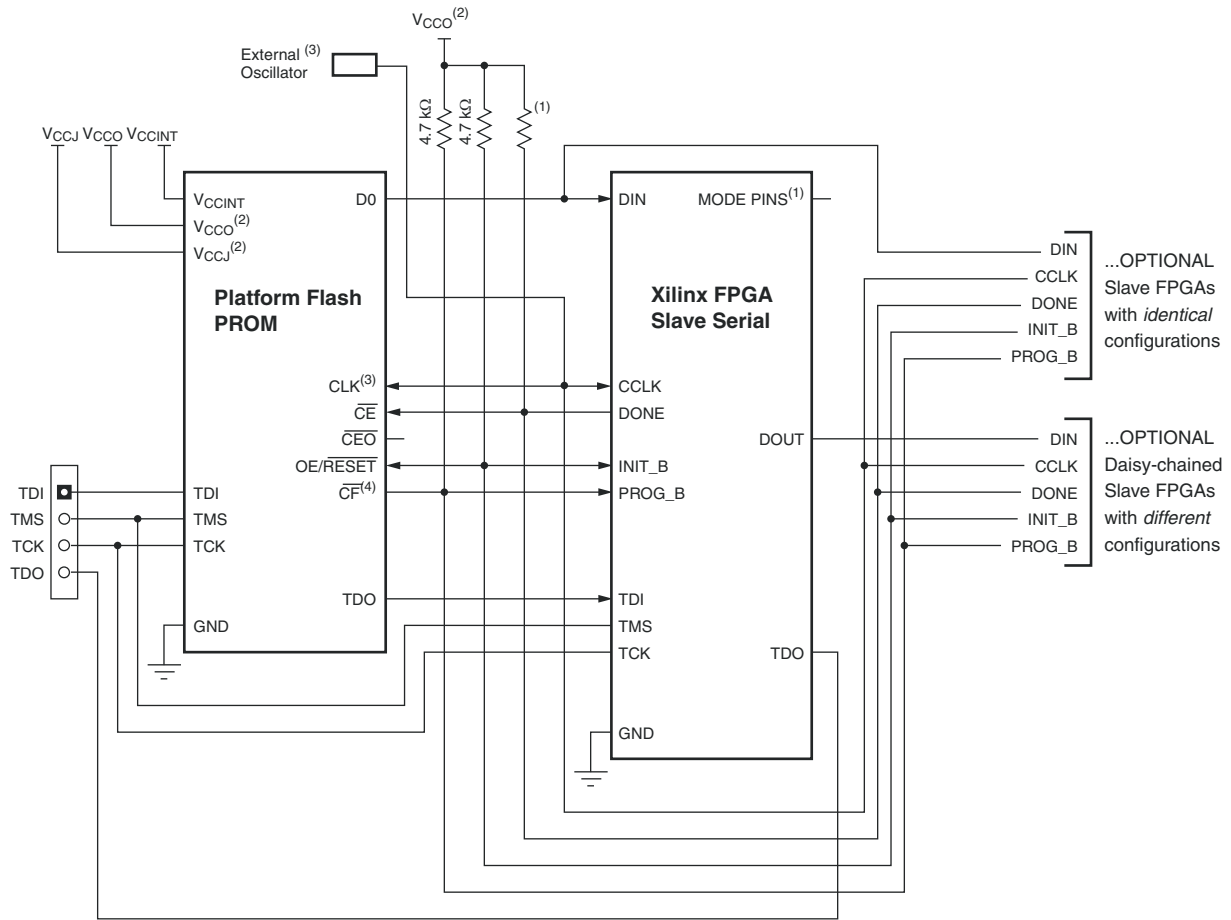


Notes:

- 1 For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- 2 For compatible voltages, refer to the appropriate data sheet.
- 3 For the XCFxxS the CF pin is an output pin. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROG\_B, then it must be tied to V<sub>CCO</sub> via a 4.7 kΩ pull-up resistor.

ds123\_11\_111106

Figure 6: Configuring in Master Serial Mode



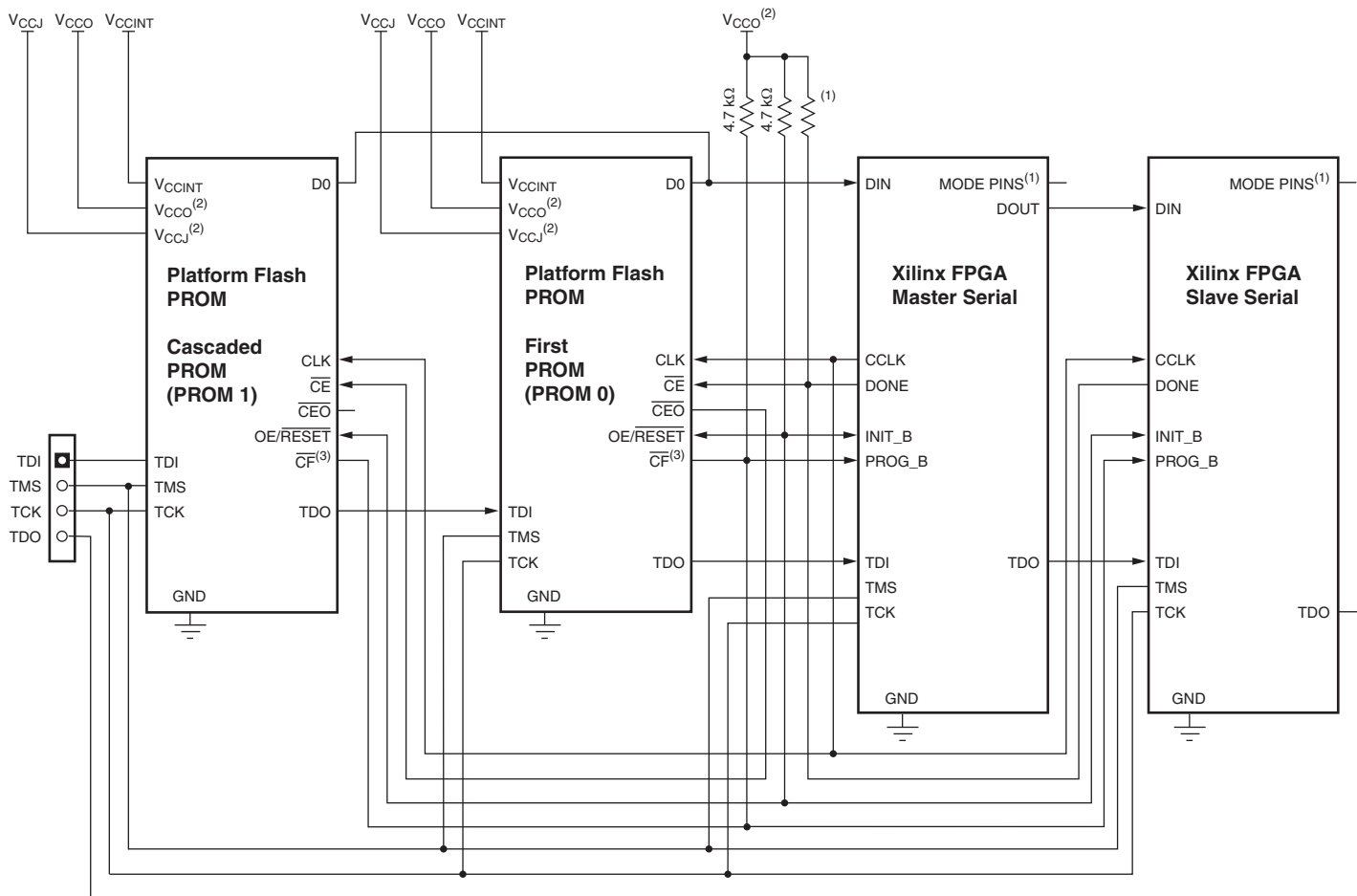
Notes:

- 1 For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- 2 For compatible voltages, refer to the appropriate data sheet.
- 3 In Slave Serial mode, the configuration interface can be clocked by an external oscillator, or optionally—for the XCFxxP Platform Flash PROM only—the CLKOUT signal can be used to drive the FPGA's configuration clock (CCLK). If the XCFxxP PROM's CLKOUT signal is used, then CLKOUT must be tied to a 4.7kΩ resistor pulled up to V<sub>CCO</sub>.
- 4 For the XCFxxS the  $\overline{CF}$  pin is an output pin. For the XCFxxP the  $\overline{CF}$  pin is a bidirectional pin. For the XCFxxP, if  $\overline{CF}$  is not connected to PROG\_B, then it must be tied to V<sub>CCO</sub> via a 4.7 kΩ pull-up resistor.

ds123\_12\_110707

Figure 7: Configuring in Slave Serial Mode



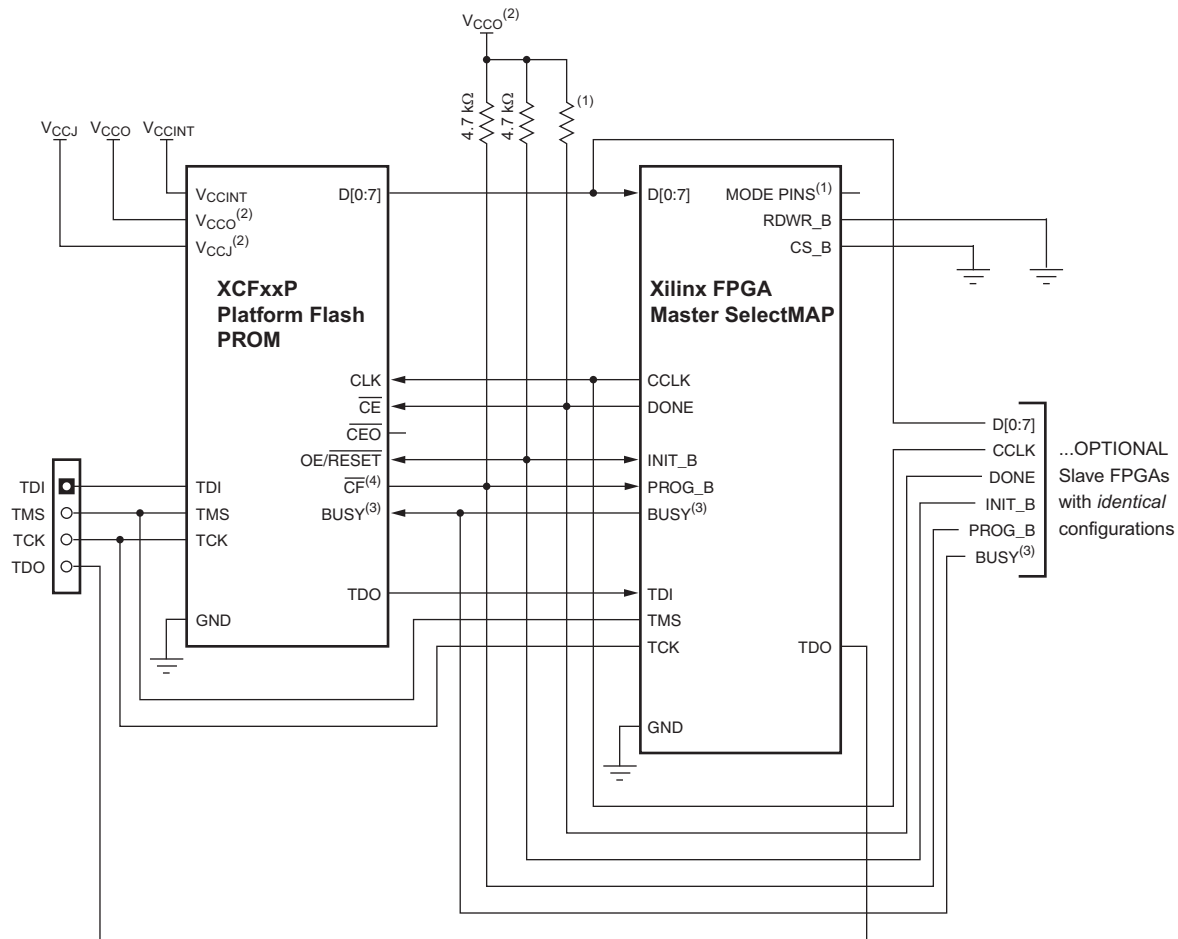


Notes:

- 1 For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- 2 For compatible voltages, refer to the appropriate data sheet.
- 3 For the XCFxxS the CF pin is an output pin. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROG\_B, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.

ds123\_13\_093006

Figure 8: Configuring Multiple Devices in Master/Slave Serial Mode

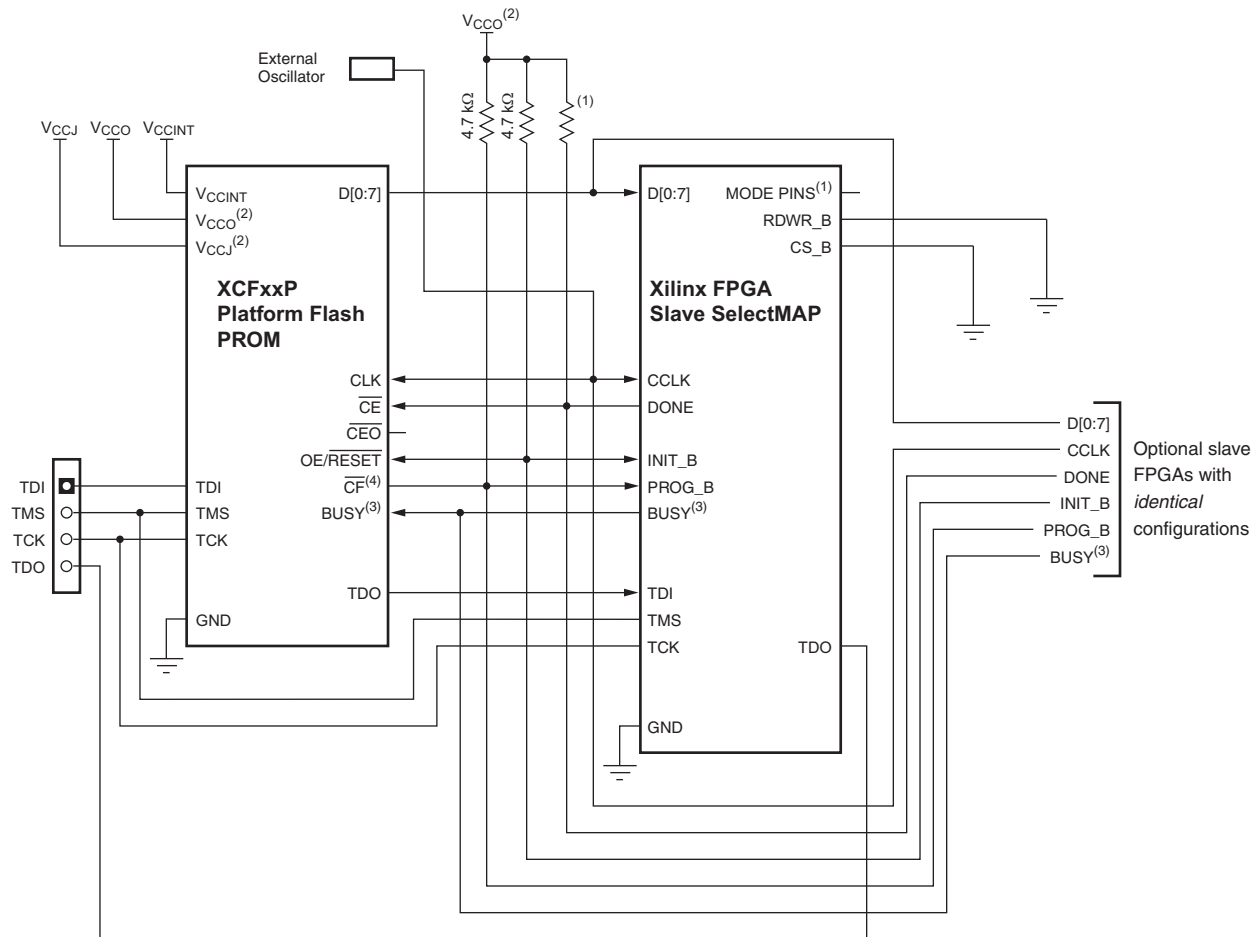


Notes:

- 1 For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- 2 For compatible voltages, refer to the appropriate data sheet.
- 3 The BUSY pin is only available with the XCFxxP Platform Flash PROM (only certain FPGA families require the BUSY pin connection for high-frequency SelectMAP mode configuration). For FPGAs that do not have a BUSY pin or do not use their BUSY pin during configuration, the Platform Flash PROM BUSY pin should be unconnected or grounded. For BUSY pin requirements, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- 4 For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROG\_B, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.

ds123\_14\_110707

Figure 9: Configuring in Master SelectMAP Mode

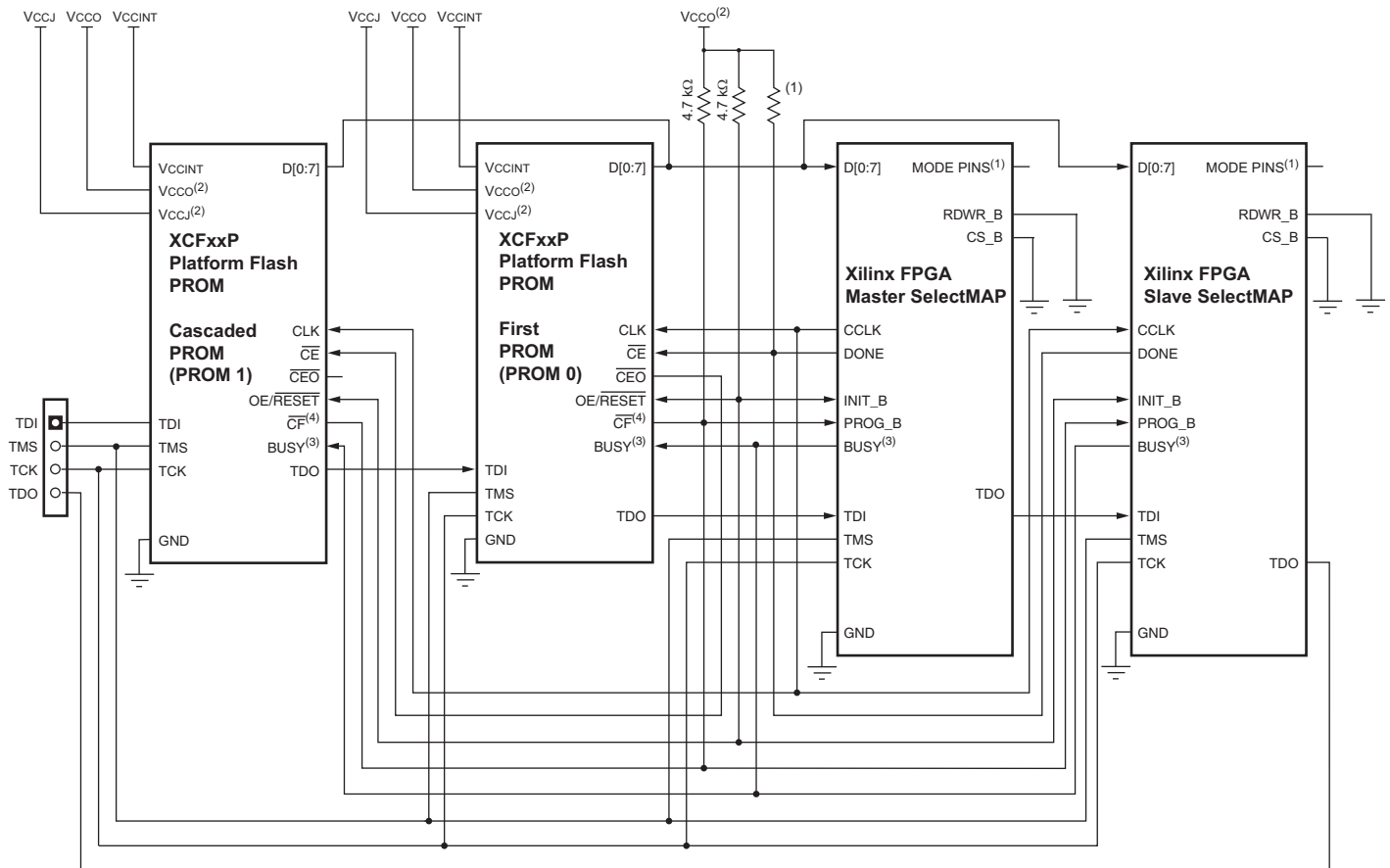


Notes:

- 1 For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- 2 For compatible voltages, refer to the appropriate data sheet.
- 3 The BUSY pin is only available with the XCFxxP Platform Flash PROM (only certain FPGA families require the BUSY pin connection for high-frequency SelectMAP mode configuration). For FPGAs that do not have a BUSY pin or do not use their BUSY pin during configuration, the Platform Flash PROM BUSY pin should be unconnected or grounded. For BUSY pin requirements, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- 4 For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROG\_B, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.

ds123\_15\_110707

Figure 10: Configuring in Slave SelectMAP Mode

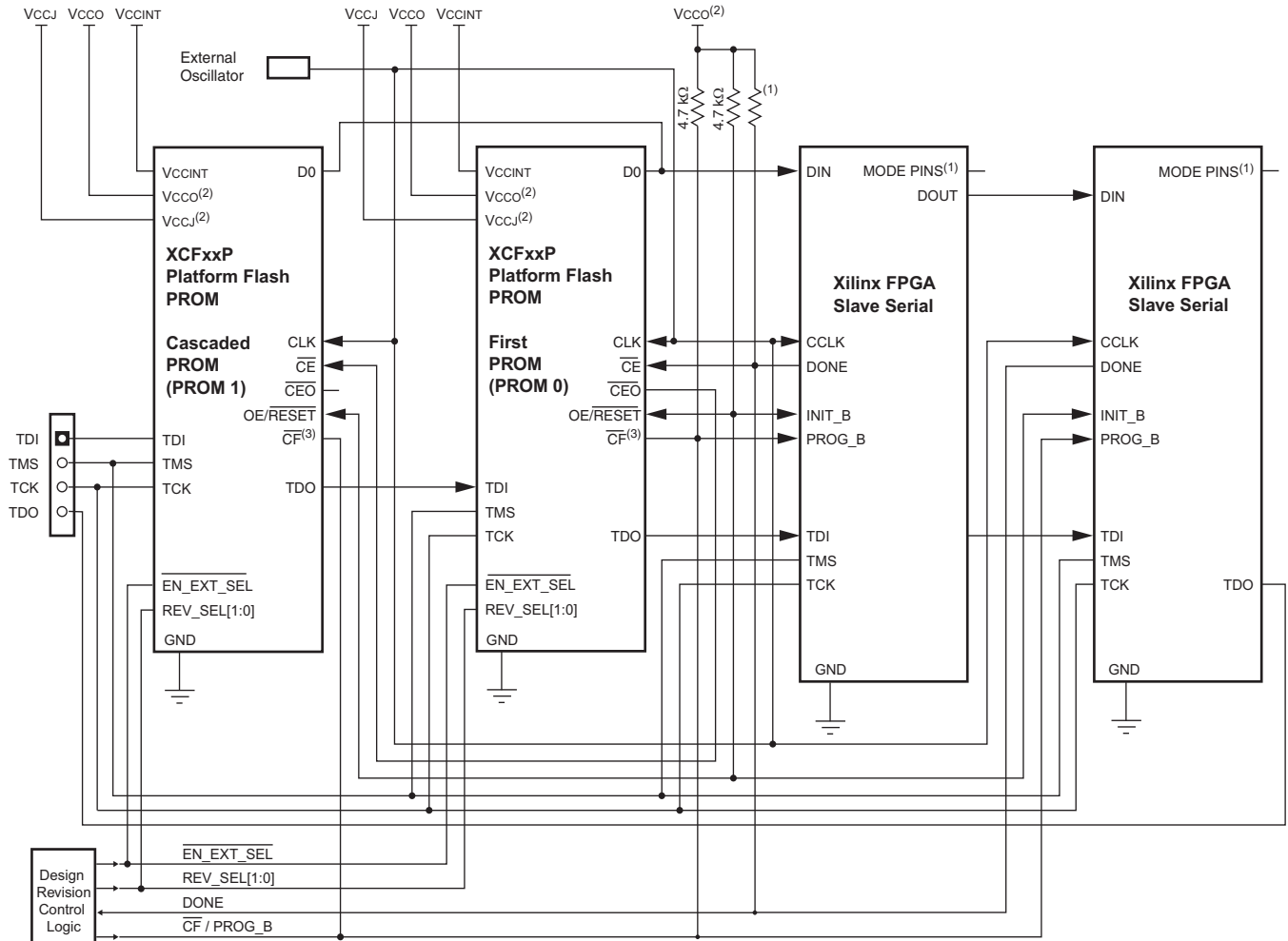


Notes:

- 1 For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- 2 For compatible voltages, refer to the appropriate data sheet.
- 3 The BUSY pin is only available with the XCFxxP Platform Flash PROM (only certain FPGA families require the BUSY pin connection for high-frequency SelectMAP mode configuration). For FPGAs that do not have a BUSY pin or do not use their BUSY pin during configuration, the Platform Flash PROM BUSY pin should be unconnected or grounded. For BUSY pin requirements, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
- 4 For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROG\_B, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.

DS123\_16\_110707

Figure 11: Configuring Multiple Devices with Identical Patterns in Master/Slave SelectMAP Mode



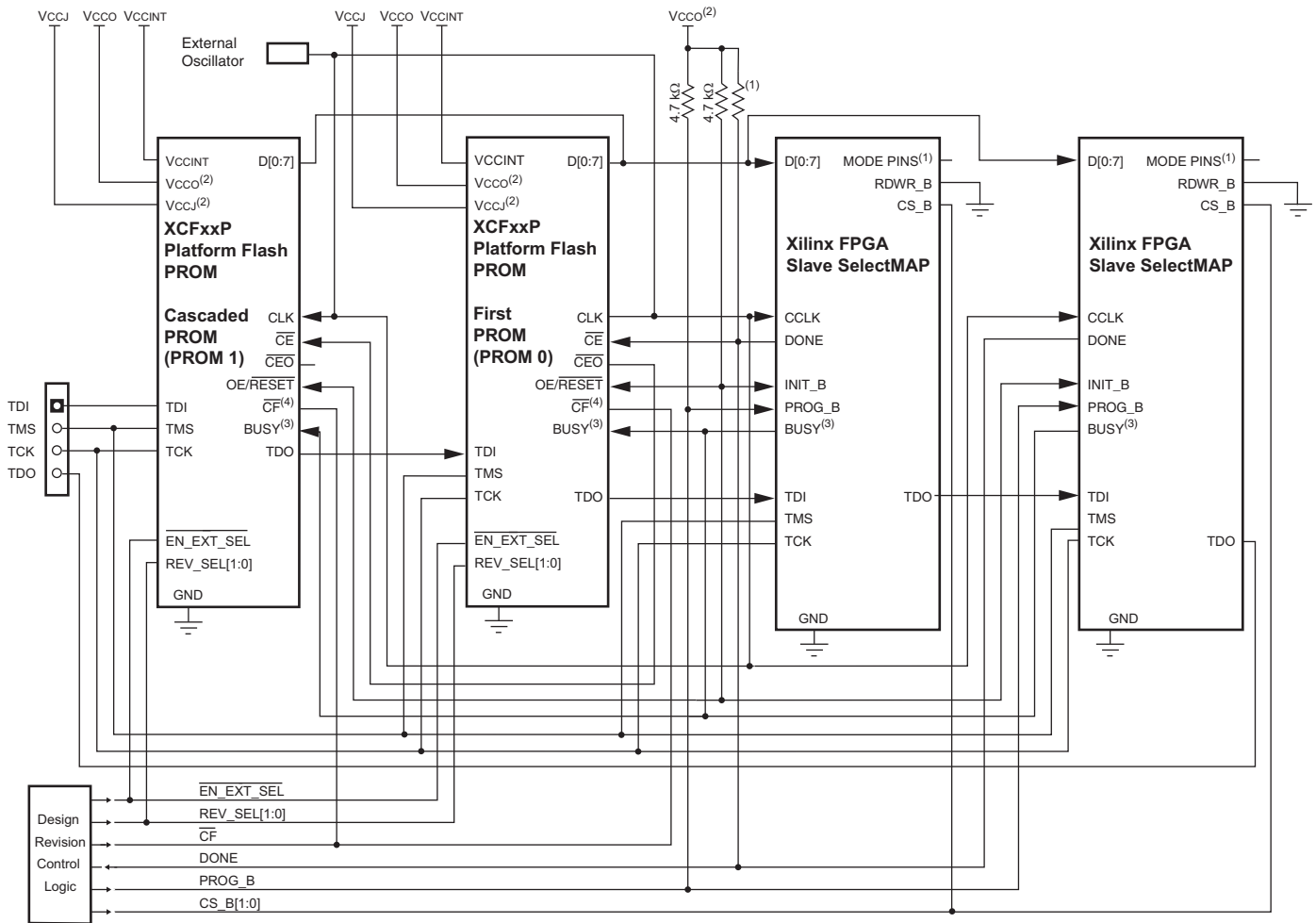
Notes

1. For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
2. For compatible voltages, refer to the appropriate data sheet.
3. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if  $\overline{CF}$  is not connected to PROG\_B, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor.

ds123\_17\_110807

Figure 12: Configuring Multiple Devices with Design Revisioning in Slave Serial Mode





Notes:

1. For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
2. For compatible voltages, refer to the appropriate data sheet.
3. The BUSY pin is only available with the XCFxxP Platform Flash PROM (only certain FPGA families require the BUSY pin connection for high-frequency SelectMAP mode configuration). For FPGAs that do not have a BUSY pin or do not use their BUSY pin during configuration, the Platform Flash PROM BUSY pin should be unconnected or grounded. For BUSY pin requirements, refer to the appropriate FPGA data sheet or FPGA family configuration user guide.
4. For the XCFxxP the CF pin is a bidirectional pin. For the XCFxxP, if CF is not connected to PROG\_B, then it must be tied to VCCO via a 4.7 kΩ pull-up resistor

ds123\_18\_110707

Figure 13: Configuring Multiple Devices with Design Revisioning in Slave SelectMAP Mode

## Reset and Power-On Reset Activation

At power up, the device requires the  $V_{CCINT}$  power supply to monotonically rise to the nominal operating voltage within the specified  $V_{CCINT}$  rise time. If the power supply cannot meet this requirement, then the device might not perform power-on reset properly. During the power-up sequence,  $\overline{OE/RESET}$  is held Low by the PROM. Once the required supplies have reached their respective POR (Power On Reset) thresholds, the  $\overline{OE/RESET}$  release is delayed ( $T_{OER}$  minimum) to allow more margin for the power supplies to stabilize before initiating configuration. The  $\overline{OE/RESET}$  pin is connected to an external 4.7 k $\Omega$  pull-up resistor and also to the target FPGA's INIT pin. For systems utilizing slow-rising power supplies, an additional power monitoring circuit can be used to delay the target configuration until the system power reaches minimum operating voltages by holding the  $\overline{OE/RESET}$  pin Low. When  $\overline{OE/RESET}$  is released, the FPGA's INIT pin is pulled High allowing the FPGA's configuration sequence to begin. If the power drops

below the power-down threshold ( $V_{CCPD}$ ), the PROM resets and  $\overline{OE/RESET}$  is again held Low until the after the POR threshold is reached.  $\overline{OE/RESET}$  polarity is not programmable. These power-up requirements are shown graphically in Figure 14.

For a fully powered Platform Flash PROM, a reset occurs whenever  $\overline{OE/RESET}$  is asserted (Low) or  $\overline{CE}$  is deasserted (High). The address counter is reset,  $\overline{CEO}$  is driven High, and the remaining outputs are placed in a high-impedance state.

### Note:

1. The XCFxxS PROM only requires  $V_{CCINT}$  to rise above its POR threshold before releasing  $\overline{OE/RESET}$ .
2. The XCFxxP PROM requires both  $V_{CCINT}$  to rise above its POR threshold and for  $V_{CCO}$  to reach the recommended operating voltage level before releasing  $\overline{OE/RESET}$ .

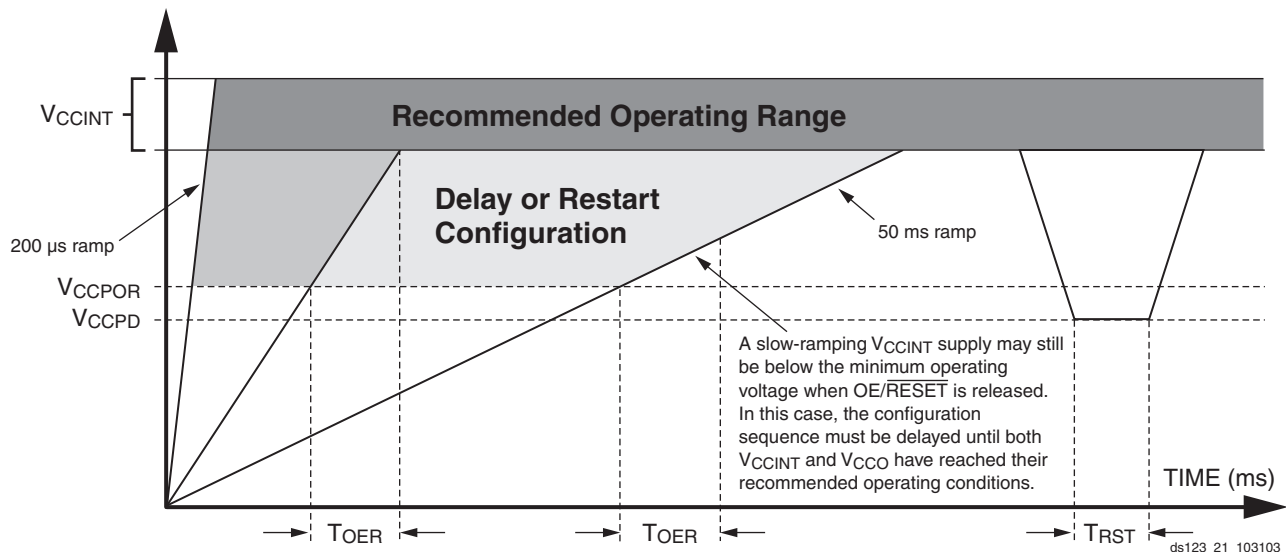


Figure 14: Platform Flash PROM Power-Up Requirements

## I/O Input Voltage Tolerance and Power Sequencing

The I/Os on each re-programmable Platform Flash PROM are fully 3.3V-tolerant. This allows 3V CMOS signals to connect directly to the inputs without damage. The core power supply ( $V_{CCINT}$ ), JTAG pin power supply ( $V_{CCJ}$ ), output power supply ( $V_{CCO}$ ), and external 3V CMOS I/O signals can be applied in any order.

Additionally, for the XCFxxS PROM only, when  $V_{CCO}$  is supplied at 2.5V or 3.3V and  $V_{CCINT}$  is supplied at 3.3V, the I/Os are 5V-tolerant. This allows 5V CMOS signals to connect directly to the inputs on a powered XCFxxS PROM without damage. Failure to power the PROM correctly while supplying a 5V input signal can result in damage to the XCFxxS device.

## Standby Mode

The PROM enters a low-power standby mode whenever  $\overline{CE}$  is deasserted (High). In standby mode, the address counter is reset,  $\overline{CEO}$  is driven High, and the remaining outputs are placed in a high-impedance state regardless of the state of the  $\overline{OE/RESET}$  input. For the device to remain in the low-power standby mode, the JTAG pins TMS, TDI, and TDO must not be pulled Low, and TCK must be stopped (High or Low).

When using the FPGA DONE signal to drive the PROM  $\overline{CE}$  pin High to reduce standby power after configuration, an external pull-up resistor should be used. Typically a 330 $\Omega$

pull-up resistor is used, but refer to the appropriate FPGA data sheet for the recommended DONE pin pull-up value. If the DONE circuit is connected to an LED to indicate FPGA configuration is complete, and is also connected to the PROM  $\overline{CE}$  pin to enable low-power standby mode, then an external buffer should be used to drive the LED circuit to ensure valid transitions on the PROM's  $\overline{CE}$  pin. If low-power standby mode is not required for the PROM, then the  $\overline{CE}$  pin should be connected to ground.

Table 11: Truth Table for XCFxxS PROM Control Inputs

| Control Inputs        |                 | Internal Address                              | Outputs |                  |         |
|-----------------------|-----------------|---|---------|------------------|---------|
| $\overline{OE/RESET}$ | $\overline{CE}$ |   | DATA    | $\overline{CEO}$ | ICC     |
| High                  | Low             | If address < TC <sup>(2)</sup> : increment    | Active  | High             | Active  |
|                       |                 | If address = TC <sup>(2)</sup> : don't change | High-Z  | Low              | Reduced |
| Low                   | Low             | Held reset                                    | High-Z  | High             | Active  |
| X <sup>(1)</sup>      | High            | Held reset                                    | High-Z  | High             | Standby |

### Notes:

1. X = don't care.
2. TC = Terminal Count = highest address value.

Table 12: Truth Table for XCFxxP PROM Control Inputs

| Control Inputs        |                 |                 |                     | Internal Address  | Outputs              |                  |        |         |
|-----------------------|-----------------|-----------------|---------------------|---|----------------------|------------------|--------|---------|
| $\overline{OE/RESET}$ | $\overline{CE}$ | $\overline{CF}$ | BUSY <sup>(5)</sup> |   | DATA                 | $\overline{CEO}$ | CLKOUT | ICC     |
| High                  | Low             | High            | Low                 | If address < TC <sup>(2)</sup> and address < EA <sup>(3)</sup> : increment    | Active               | High             | Active | Active  |
|                       |                 |                 |                     | If address < TC <sup>(2)</sup> and address = EA <sup>(3)</sup> : don't change | High-Z               | High             | High-Z | Reduced |
|                       |                 |                 |                     | Else<br>If address = TC <sup>(2)</sup> : don't change                         | High-Z               | Low              | High-Z | Reduced |
| High                  | Low             | High            | High                | Unchanged   | Active and Unchanged | High             | Active | Active  |
| High                  | Low             | ;               | X <sup>(1)</sup>    | Reset <sup>(4)</sup>  | Active               | High             | Active | Active  |
| Low                   | Low             | X               | X                   | Held reset <sup>(4)</sup>   | High-Z               | High             | High-Z | Active  |
| X                     | High            | X               | X                   | Held reset <sup>(4)</sup>   | High-Z               | High             | High-Z | Standby |

### Notes:

1. X = don't care.
2. TC = Terminal Count = highest address value.
3. For the XCFxxP with Design Revisioning enabled, EA = end address (last address in the selected design revision).
4. For the XCFxxP with Design Revisioning enabled, Reset = address reset to the beginning address of the selected bank. If Design Revisioning is not enabled, then Reset = address reset to address 0.
5. The BUSY input is only enabled when the XCFxxP is programmed for parallel data output and decompression is not enabled.

## DC Electrical Characteristics

### Absolute Maximum Ratings

| Symbol      | Description                             | XCF01S, XCF02S,<br>XCF04S | XCF08P, XCF16P,<br>XCF32P | Units |
|-------------|---|---------------------------|---------------------------|-------|
| $V_{CCINT}$ | Internal supply voltage relative to GND | -0.5 to +4.0              | -0.5 to +2.7              | V     |
| $V_{CCO}$   | I/O supply voltage relative to GND      | -0.5 to +4.0              | -0.5 to +4.0              | V     |
| $V_{CCJ}$   | JTAG I/O supply voltage relative to GND | -0.5 to +4.0              | -0.5 to +4.0              | V     |
| $V_{IN}$    | Input voltage with respect to GND       | $V_{CCO} < 2.5V$          | -0.5 to +3.6              | V     |
|             |   | $V_{CCO} \geq 2.5V$       | -0.5 to +5.5              | V     |
| $V_{TS}$    | Voltage applied to High-Z output        | $V_{CCO} < 2.5V$          | -0.5 to +3.6              | V     |
|             |   | $V_{CCO} \geq 2.5V$       | -0.5 to +5.5              | V     |
| $T_{STG}$   | Storage temperature (ambient)           | -65 to +150               | -65 to +150               | °C    |
| $T_J$       | Junction temperature                    | +125                      | +125                      | °C    |

#### Notes:

- Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins can undershoot to -2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
- For soldering guidelines, see the information on "Packaging and Thermal Characteristics" at [www.xilinx.com](http://www.xilinx.com).

### Supply Voltage Requirements for Power-On Reset and Power-Down

| Symbol      | Description  | XCF01S, XCF02S,<br>XCF04S |     | XCF08P, XCF16P,<br>XCF32P |     | Units |
|-------------|--|---------------------------|-----|---------------------------|-----|-------|
|             |  | Min                       | Max | Min                       | Max |       |
| $T_{VCC}$   | $V_{CCINT}$ rise time from 0V to nominal voltage <sup>(2)</sup>  | 0.2                       | 50  | 0.2                       | 50  | ms    |
| $V_{CCPOR}$ | POR threshold for the $V_{CCINT}$ supply   | 1                         | -   | 0.5                       | -   | V     |
| $T_{OER}$   | OE/ $\overline{RESET}$ release delay following POR <sup>(3)</sup>  | 0.5                       | 3   | 0.5                       | 30  | ms    |
| $V_{CCPD}$  | Power-down threshold for $V_{CCINT}$ supply  | -                         | 1   | -                         | 0.5 | V     |
| $T_{RST}$   | Time required to trigger a device reset when the $V_{CCINT}$ supply drops below the maximum $V_{CCPD}$ threshold | 10                        | -   | 10                        | -   | ms    |

#### Notes:

- $V_{CCINT}$ ,  $V_{CCO}$ , and  $V_{CCJ}$  supplies can be applied in any order.
- At power up, the device requires the  $V_{CCINT}$  power supply to monotonically rise to the nominal operating voltage within the specified  $T_{VCC}$  rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See [Figure 14, page 25](#).
- If the  $V_{CCINT}$  and  $V_{CCO}$  supplies do not reach their respective recommended operating conditions before the OE/ $\overline{RESET}$  pin is released, then the configuration data from the PROM is not available at the recommended threshold levels. The configuration sequence must be delayed until both  $V_{CCINT}$  and  $V_{CCO}$  have reached their recommended operating conditions.

## Recommended Operating Conditions

| Symbol             | Description                                 |                | XCF01S, XCF02S, XCF04S |     |                      | XCF08P, XCF16P, XCF32P |     |                      | Units |
|--------------------|---|----------------|------------------------|-----|----------------------|------------------------|-----|----------------------|-------|
|                    |   |                | Min                    | Typ | Max                  | Min                    | Typ | Max                  |       |
| V <sub>CCINT</sub> | Internal voltage supply                     |                | 3.0                    | 3.3 | 3.6                  | 1.65                   | 1.8 | 2.0                  | V     |
| V <sub>CCO</sub>   | Supply voltage for output drivers           | 3.3V Operation | 3.0                    | 3.3 | 3.6                  | 3.0                    | 3.3 | 3.6                  | V     |
|                    |   | 2.5V Operation | 2.3                    | 2.5 | 2.7                  | 2.3                    | 2.5 | 2.7                  | V     |
|                    |   | 1.8V Operation | 1.7                    | 1.8 | 1.9                  | 1.7                    | 1.8 | 1.9                  | V     |
|                    |   | 1.5V Operation | –                      | –   | –                    |                        | 1.5 |                      | V     |
| V <sub>CCJ</sub>   | Supply voltage for JTAG output drivers      | 3.3V Operation | 3.0                    | 3.3 | 3.6                  | 3.0                    | 3.3 | 3.6                  | V     |
|                    |   | 2.5V Operation | 2.3                    | 2.5 | 2.7                  | 2.3                    | 2.5 | 2.7                  | V     |
| V <sub>IL</sub>    | Low-level input voltage                     | 3.3V Operation | 0                      | –   | 0.8                  | 0                      | –   | 0.8                  | V     |
|                    |   | 2.5V Operation | 0                      | –   | 0.7                  | 0                      | –   | 0.7                  | V     |
|                    |   | 1.8V Operation | –                      | –   | 20% V <sub>CCO</sub> | –                      | –   | 20% V <sub>CCO</sub> | V     |
|                    |   | 1.5V Operation | –                      | –   | –                    | 0                      | –   |                      | V     |
| V <sub>IH</sub>    | High-level input voltage                    | 3.3V Operation | 2.0                    | –   | 5.5                  | 2.0                    | –   | 3.6                  | V     |
|                    |   | 2.5V Operation | 1.7                    | –   | 5.5                  | 1.7                    | –   | 3.6                  | V     |
|                    |   | 1.8V Operation | 70% V <sub>CCO</sub>   | –   | 3.6                  | 70% V <sub>CCO</sub>   | –   | 3.6                  | V     |
|                    |   | 1.5V Operation | –                      | –   | –                    | –                      | –   | 3.6                  | V     |
| T <sub>IN</sub>    | Input signal transition time <sup>(1)</sup> |                | –                      | –   | 500                  | –                      | –   | 500                  | ns    |
| V <sub>O</sub>     | Output voltage                              |                | 0                      | –   | V <sub>CCO</sub>     | 0                      | –   | V <sub>CCO</sub>     | V     |
| T <sub>A</sub>     | Operating ambient temperature               |                | –40                    | –   | 85                   | –40                    | –   | 85                   | °C    |

### Notes:

1. Input signal transition time measured between 10% V<sub>CCO</sub> and 90% V<sub>CCO</sub>.

## Quality and Reliability Characteristics

| Symbol           | Description                      | Min    | Max | Units  |
|------------------|----------------------------------|--------|-----|--------|
| T <sub>DR</sub>  | Data retention                   | 20     | –   | Years  |
| N <sub>PE</sub>  | Program/erase cycles (Endurance) | 20,000 | –   | Cycles |
| V <sub>ESD</sub> | Electrostatic discharge (ESD)    | 2,000  | –   | Volts  |

## DC Characteristics Over Operating Conditions

| Symbol                          | Description   | XCF01S, XCF02S,<br>XCF04S  |                        |     | XCF08P, XCF16P,<br>XCF32P  |                        |     | Units |
|---------------------------------|---|--|------------------------|-----|--|------------------------|-----|-------|
|                                 |   | Test Conditions  | Min                    | Max | Test Conditions  | Min                    | Max |       |
| V <sub>OH</sub>                 | High-level output voltage for 3.3V outputs                                    | I <sub>OH</sub> = -4 mA  | 2.4                    | -   | I <sub>OH</sub> = -4 mA  | 2.4                    | -   | V     |
|                                 | High-level output voltage for 2.5V outputs                                    | I <sub>OH</sub> = -500 μA  | V <sub>CCO</sub> - 0.4 | -   | I <sub>OH</sub> = -500 μA  | V <sub>CCO</sub> - 0.4 | -   | V     |
|                                 | High-level output voltage for 1.8V outputs                                    | I <sub>OH</sub> = -50 μA   | V <sub>CCO</sub> - 0.4 | -   | I <sub>OH</sub> = -50 μA   | V <sub>CCO</sub> - 0.4 | -   | V     |
|                                 | High-level output voltage for 1.5V outputs                                    | -  | -                      | -   | -  | -                      | -   | V     |
| V <sub>OL</sub>                 | Low-level output voltage for 3.3V outputs                                     | I <sub>OL</sub> = 4 mA   | -                      | 0.4 | I <sub>OL</sub> = 4 mA   | -                      | 0.4 | V     |
|                                 | Low-level output voltage for 2.5V outputs                                     | I <sub>OL</sub> = 500 μA   | -                      | 0.4 | I <sub>OL</sub> = 500 μA   | -                      | 0.4 | V     |
|                                 | Low-level output voltage for 1.8V outputs                                     | I <sub>OL</sub> = 50 μA  | -                      | 0.4 | I <sub>OL</sub> = 50 μA  | -                      | 0.4 | V     |
|                                 | Low-level output voltage for 1.5V outputs                                     | -  | -                      | -   | -  | -                      | -   | V     |
| I <sub>CCINT</sub>              | Internal voltage supply current, active mode                                  | 33 MHz   | -                      | 10  | 33 MHz   | -                      | 10  | mA    |
| I <sub>CCO</sub> <sup>(1)</sup> | Output driver supply current, active serial mode                              | 33 MHz   | -                      | 10  | 33 MHz   | -                      | 10  | mA    |
|                                 | Output driver supply current, active parallel mode                            | -  | -                      | -   | 33 MHz   | -                      | 40  | mA    |
| I <sub>CCJ</sub>                | JTAG supply current, active mode  | Note (2)   | -                      | 5   | Note (2)   | -                      | 5   | mA    |
| I <sub>CCINTS</sub>             | Internal voltage supply current, standby mode                                 | Note (3)   | -                      | 5   | Note (3)   | -                      | 1   | mA    |
| I <sub>CCOS</sub>               | Output driver supply current, standby mode                                    | Note (3)   | -                      | 1   | Note (3)   | -                      | 1   | mA    |
| I <sub>CCJS</sub>               | JTAG supply current, standby mode   | Note (3)   | -                      | 1   | Note (3)   | -                      | 1   | mA    |
| I <sub>ILJ</sub>                | JTAG pins TMS, TDI, and TDO pull-up current                                   | V <sub>CCJ</sub> = max<br>V <sub>IN</sub> = GND  | -                      | 100 | V <sub>CCJ</sub> = max<br>V <sub>IN</sub> = GND  | -                      | 100 | μA    |
| I <sub>IL</sub>                 | Input leakage current   | V <sub>CCINT</sub> = max<br>V <sub>CCO</sub> = max<br>V <sub>IN</sub> = GND or<br>V <sub>CCO</sub> | -10                    | 10  | V <sub>CCINT</sub> = max<br>V <sub>CCO</sub> = max<br>V <sub>IN</sub> = GND or<br>V <sub>CCO</sub> | -10                    | 10  | μA    |
| I <sub>IH</sub>                 | Input and output High-Z leakage current                                       | V <sub>CCINT</sub> = max<br>V <sub>CCO</sub> = max<br>V <sub>IN</sub> = GND or<br>V <sub>CCO</sub> | -10                    | 10  | V <sub>CCINT</sub> = max<br>V <sub>CCO</sub> = max<br>V <sub>IN</sub> = GND or<br>V <sub>CCO</sub> | -10                    | 10  | μA    |
| I <sub>ILP</sub>                | Source current through internal pull-ups on<br>EN_EXT_SEL, REV_SEL0, REV_SEL1 | -  | -                      | -   | V <sub>CCINT</sub> = max<br>V <sub>CCO</sub> = max<br>V <sub>IN</sub> = GND or<br>V <sub>CCO</sub> | -                      | 100 | μA    |
| I <sub>IHP</sub>                | Sink current through internal pull-down on BUSY                               | -  | -                      | -   | V <sub>CCINT</sub> = max<br>V <sub>CCO</sub> = max<br>V <sub>IN</sub> = GND or<br>V <sub>CCO</sub> | -100                   | -   | μA    |
| C <sub>IN</sub>                 | Input capacitance   | V <sub>IN</sub> = GND<br>f = 1.0 MHz   | -                      | 8   | V <sub>IN</sub> = GND<br>f = 1.0 MHz   | -                      | 8   | pF    |
| C <sub>OUT</sub>                | Output capacitance  | V <sub>IN</sub> = GND<br>f = 1.0 MHz   | -                      | 14  | V <sub>IN</sub> = GND<br>f = 1.0 MHz   | -                      | 14  | pF    |

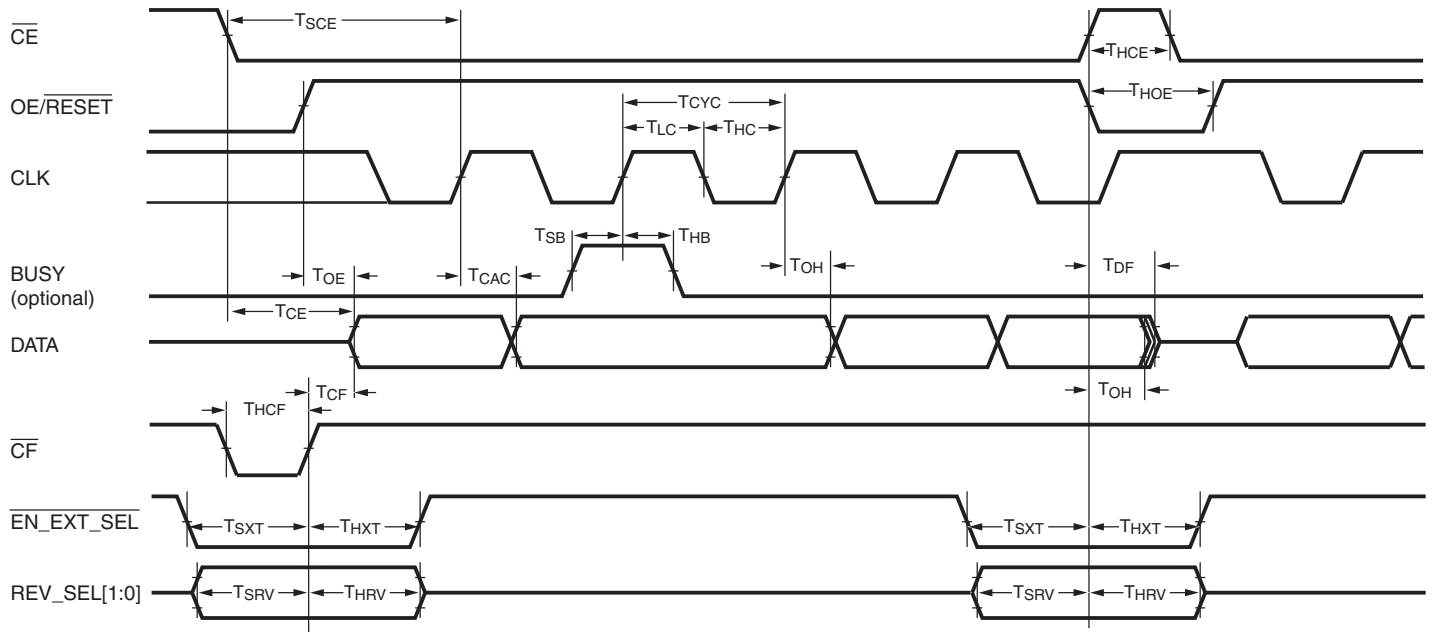
### Notes:

- Output driver supply current specification based on no load conditions.
- TDI/TMS/TCK non-static (active).
- $\overline{CE}$  High, OE Low, and TMS/TDI/TCK static.

## AC Electrical Characteristics

### AC Characteristics Over Operating Conditions

#### XCFxxS and XCFxxP PROM as Configuration Slave with CLK Input Pin as Clock Source



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| Symbol           | Description  | XCF01S, XCF02S, XCF04S |     | XCF08P, XCF16P, XCF32P |     | Units |
|------------------|--|------------------------|-----|------------------------|-----|-------|
|                  |  | Min                    | Max | Min                    | Max |       |
| T <sub>HCF</sub> | CF hold time to guarantee design revision selection is sampled when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(9)</sup>   | 300                    |     | 300                    |     | ns    |
|                  | $\overline{\text{CF}}$ hold time to guarantee design revision selection is sampled when V <sub>CCO</sub> = 1.8V <sup>(9)</sup>                             | 300                    |     | 300                    |     | ns    |
| T <sub>CF</sub>  | $\overline{\text{CF}}$ to data delay when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(8)</sup>   | –                      | –   | –                      | 25  | ns    |
|                  | $\overline{\text{CF}}$ to data delay when V <sub>CCO</sub> = 1.8V <sup>(8)</sup>   | –                      | –   | –                      | 25  | ns    |
| T <sub>OE</sub>  | OE/ $\overline{\text{RESET}}$ to data delay <sup>(6)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | –                      | 10  | –                      | 25  | ns    |
|                  | OE/ $\overline{\text{RESET}}$ to data delay <sup>(6)</sup> when V <sub>CCO</sub> = 1.8V  | –                      | 30  | –                      | 25  | ns    |
| T <sub>CE</sub>  | $\overline{\text{CE}}$ to data delay <sup>(5)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V   | –                      | 15  | –                      | 25  | ns    |
|                  | $\overline{\text{CE}}$ to data delay <sup>(5)</sup> when V <sub>CCO</sub> = 1.8V   | –                      | 30  | –                      | 25  | ns    |
| T <sub>CAC</sub> | CLK to data delay <sup>(7)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | –                      | 15  | –                      | 25  | ns    |
|                  | CLK to data delay <sup>(7)</sup> when V <sub>CCO</sub> = 1.8V  | –                      | 30  | –                      | 25  | ns    |
| T <sub>OH</sub>  | Data hold from $\overline{\text{CE}}$ , OE/ $\overline{\text{RESET}}$ , CLK, or $\overline{\text{CF}}$ when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(8)</sup> | 0                      | –   | 5                      | –   | ns    |
|                  | Data hold from $\overline{\text{CE}}$ , OE/ $\overline{\text{RESET}}$ , CLK, or $\overline{\text{CF}}$ when V <sub>CCO</sub> = 1.8V <sup>(8)</sup>         | 0                      | –   | 5                      | –   | ns    |
| T <sub>DF</sub>  | $\overline{\text{CE}}$ or OE/ $\overline{\text{RESET}}$ to data float delay <sup>(2)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V                            | –                      | 25  | –                      | 45  | ns    |
|                  | $\overline{\text{CE}}$ or OE/ $\overline{\text{RESET}}$ to data float delay <sup>(2)</sup> when V <sub>CCO</sub> = 1.8V                                    | –                      | 30  | –                      | 45  | ns    |

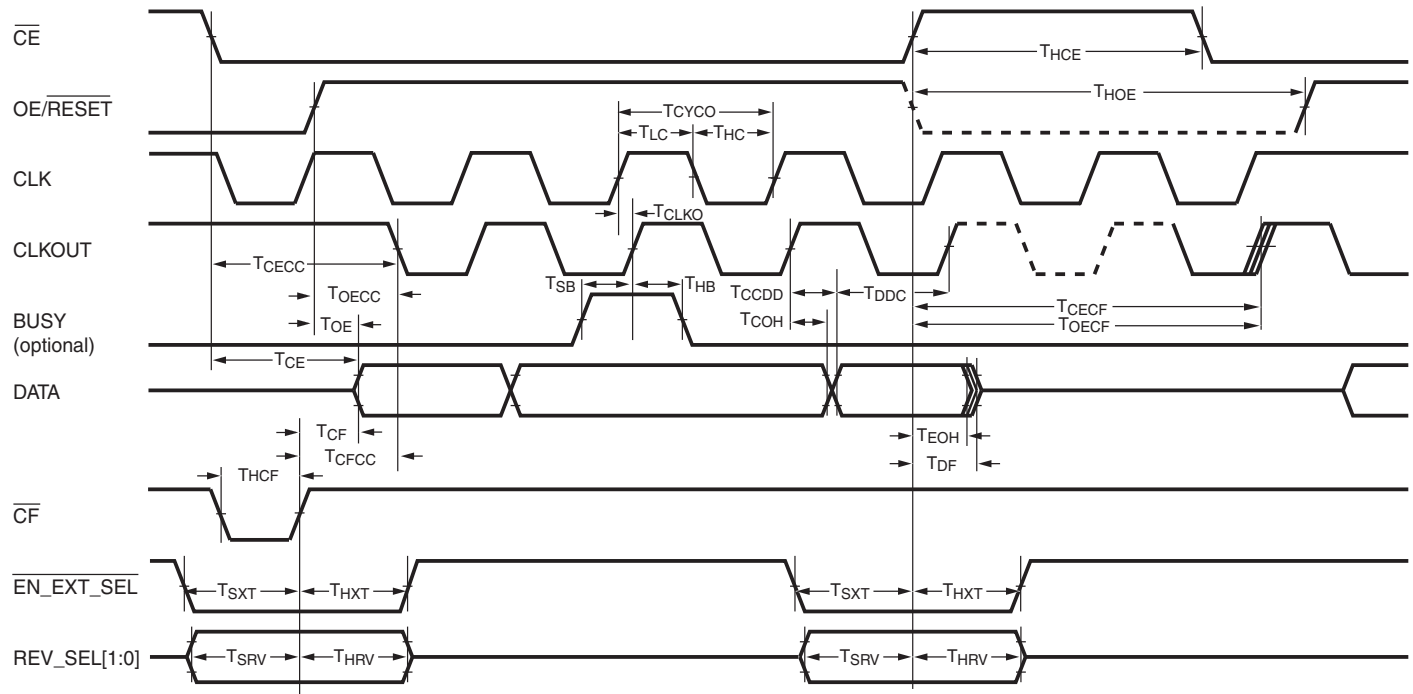


| Symbol           | Description  | XCF01S, XCF02S, XCF04S |     | XCF08P, XCF16P, XCF32P |     | Units |
|------------------|--|------------------------|-----|------------------------|-----|-------|
|                  |  | Min                    | Max | Min                    | Max |       |
| T <sub>CYC</sub> | Clock period <sup>(6)</sup> (serial mode) when V <sub>CCO</sub> = 3.3V or 2.5V   | 30                     | –   | 25                     | –   | ns    |
|                  | Clock period <sup>(6)</sup> (serial mode) when V <sub>CCO</sub> = 1.8V   | 67                     | –   | 25                     | –   | ns    |
|                  | Clock period <sup>(6)</sup> (parallel mode) when V <sub>CCO</sub> = 3.3V or 2.5V   | –                      | –   | 30                     | –   | ns    |
|                  | Clock period <sup>(6)</sup> (parallel mode) when V <sub>CCO</sub> = 1.8V   | –                      | –   | 30                     | –   | ns    |
| T <sub>LC</sub>  | CLK Low time <sup>(3)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V   | 10                     | –   | 12                     | –   | ns    |
|                  | CLK Low time <sup>(3)</sup> when V <sub>CCO</sub> = 1.8V   | 15                     | –   | 12                     | –   | ns    |
| T <sub>HC</sub>  | CLK High time <sup>(3)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | 10                     | –   | 12                     | –   | ns    |
|                  | CLK High time <sup>(3)</sup> when V <sub>CCO</sub> = 1.8V  | 15                     | –   | 12                     | –   | ns    |
| T <sub>SCE</sub> | $\overline{CE}$ setup time to CLK (guarantees proper counting) <sup>(3)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V                                       | 20                     | –   | 30                     | –   | ns    |
|                  | $\overline{CE}$ setup time to CLK (guarantees proper counting) <sup>(3)</sup> when V <sub>CCO</sub> = 1.8V   | 30                     | –   | 30                     | –   | ns    |
| T <sub>HCE</sub> | $\overline{CE}$ hold time (guarantees counters are reset) <sup>(5)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | 250                    | –   | 2000                   | –   | ns    |
|                  | $\overline{CE}$ hold time (guarantees counters are reset) <sup>(5)</sup> when V <sub>CCO</sub> = 1.8V  | 250                    | –   | 2000                   | –   | ns    |
| T <sub>HOE</sub> | OE/ $\overline{RESET}$ hold time (guarantees counters are reset) <sup>(6)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V                                     | 250                    | –   | 2000                   | –   | ns    |
|                  | OE/ $\overline{RESET}$ hold time (guarantees counters are reset) <sup>(6)</sup> when V <sub>CCO</sub> = 1.8V   | 250                    | –   | 2000                   | –   | ns    |
| T <sub>SB</sub>  | BUSY setup time to CLK when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(8)</sup>   | –                      | –   | 12                     | –   | ns    |
|                  | BUSY setup time to CLK when V <sub>CCO</sub> = 1.8V <sup>(8)</sup>   | –                      | –   | 12                     | –   | ns    |
| T <sub>HB</sub>  | BUSY hold time to CLK when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(8)</sup>  | –                      | –   | 8                      | –   | ns    |
|                  | BUSY hold time to CLK when V <sub>CCO</sub> = 1.8V <sup>(8)</sup>  | –                      | –   | 8                      | –   | ns    |
| T <sub>SXT</sub> | $\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$ , $\overline{CE}$ or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(8)</sup>  | –                      | –   | 300                    | –   | ns    |
|                  | $\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$ , $\overline{CE}$ or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 1.8V <sup>(8)</sup>          | –                      | –   | 300                    | –   | ns    |
| T <sub>HXT</sub> | $\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$ , $\overline{CE}$ or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(8)</sup> | –                      | –   | 300                    | –   | ns    |
|                  | $\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$ , $\overline{CE}$ or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 1.8V <sup>(8)</sup>         | –                      | –   | 300                    | –   | ns    |
| T <sub>SRV</sub> | REV_SEL setup time to $\overline{CF}$ , $\overline{CE}$ or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(8)</sup>                    | –                      | –   | 300                    | –   | ns    |
|                  | REV_SEL setup time to $\overline{CF}$ , $\overline{CE}$ or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 1.8V <sup>(8)</sup>                            | –                      | –   | 300                    | –   | ns    |
| T <sub>HRV</sub> | REV_SEL hold time from $\overline{CF}$ , $\overline{CE}$ or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(8)</sup>                   | –                      | –   | 300                    | –   | ns    |
|                  | REV_SEL hold time from $\overline{CF}$ , $\overline{CE}$ or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 1.8V <sup>(8)</sup>                           | –                      | –   | 300                    | –   | ns    |

**Notes:**

- AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
- Float delays are measured with 5 pF AC loads. Transition is measured at  $\pm 200$  mV from steady-state active levels.
- All AC parameters are measured with V<sub>IL</sub> = 0.0V and V<sub>IH</sub> = 3.0V.
- If T<sub>HCE</sub> High < 2  $\mu$ s, T<sub>CE</sub> = 2  $\mu$ s.
- If T<sub>HOE</sub> Low < 2  $\mu$ s, T<sub>OE</sub> = 2  $\mu$ s.
- This is the minimum possible T<sub>CYC</sub>. Actual T<sub>CYC</sub> = T<sub>CAC</sub> + FPGA Data setup time. Example: With the XCF32P in serial mode with V<sub>CCO</sub> at 3.3V, if FPGA data setup time = 15 ns, then the actual T<sub>CYC</sub> = 25 ns + 15 ns = 40 ns.
- Guaranteed by design; not tested.
- $\overline{CF}$ ,  $\overline{EN\_EXT\_SEL}$ , REV\_SEL[1:0], and BUSY are inputs for the XCFxxP PROM only.
- When JTAG CONFIG command is issued, PROM drives  $\overline{CF}$  Low for at least the T<sub>HCF</sub> minimum.

XCFxxP PROM as Configuration Master with CLK Input Pin as Clock Source



Note: Typically, 8 CLKOUT cycles are output after CE rising edge, before CLKOUT tristates, if OE/RESET remains high, and terminal count has not been reached.

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| Symbol             | Description  | XCF08P, XCF16P, XCF32P |     | Units |
|--------------------|--|------------------------|-----|-------|
|                    |  | Min                    | Max |       |
| T <sub>HCF</sub>   | $\overline{CF}$ hold time to guarantee design revision selection is sampled when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(11)</sup> | 300                    |     | 300   |
|                    | $\overline{CF}$ hold time to guarantee design revision selection is sampled when V <sub>CCO</sub> = 1.8V <sup>(11)</sup>         | 300                    |     | 300   |
| T <sub>CF</sub>    | $\overline{CF}$ to data delay when V <sub>CCO</sub> = 3.3V or 2.5V   | –                      |     | ns    |
|                    | $\overline{CF}$ to data delay when V <sub>CCO</sub> = 1.8V   | –                      |     | ns    |
| T <sub>OE</sub>    | OE/RESET to data delay <sup>(6)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V   | –                      | 25  | ns    |
|                    | OE/RESET to data delay <sup>(6)</sup> when V <sub>CCO</sub> = 1.8V   | –                      | 25  | ns    |
| T <sub>CE</sub>    | $\overline{CE}$ to data delay <sup>(5)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | –                      | 25  | ns    |
|                    | $\overline{CE}$ to data delay <sup>(5)</sup> when V <sub>CCO</sub> = 1.8V  | –                      | 25  | ns    |
| T <sub>EOH</sub>   | Data hold from $\overline{CE}$ , OE/RESET, or $\overline{CF}$ when V <sub>CCO</sub> = 3.3V or 2.5V                               | 5                      | –   | ns    |
|                    | Data hold from $\overline{CE}$ , OE/RESET, or $\overline{CF}$ when V <sub>CCO</sub> = 1.8V                                       | 5                      | –   | ns    |
| T <sub>DF</sub>    | $\overline{CE}$ or OE/RESET to data float delay <sup>(2)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V                              | –                      | 45  | ns    |
|                    | $\overline{CE}$ or OE/RESET to data float delay <sup>(2)</sup> when V <sub>CCO</sub> = 1.8V                                      | –                      | 45  | ns    |
| T <sub>OEFCF</sub> | OE/RESET to CLKOUT float delay <sup>(2)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V   | –                      |     | ns    |
|                    | OE/RESET to CLKOUT float delay <sup>(2)</sup> when V <sub>CCO</sub> = 1.8V   | –                      |     | ns    |
| T <sub>CEFCF</sub> | $\overline{CE}$ to CLKOUT float delay <sup>(2)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | –                      |     | ns    |
|                    | $\overline{CE}$ to CLKOUT float delay <sup>(2)</sup> when V <sub>CCO</sub> = 1.8V  | –                      |     | ns    |

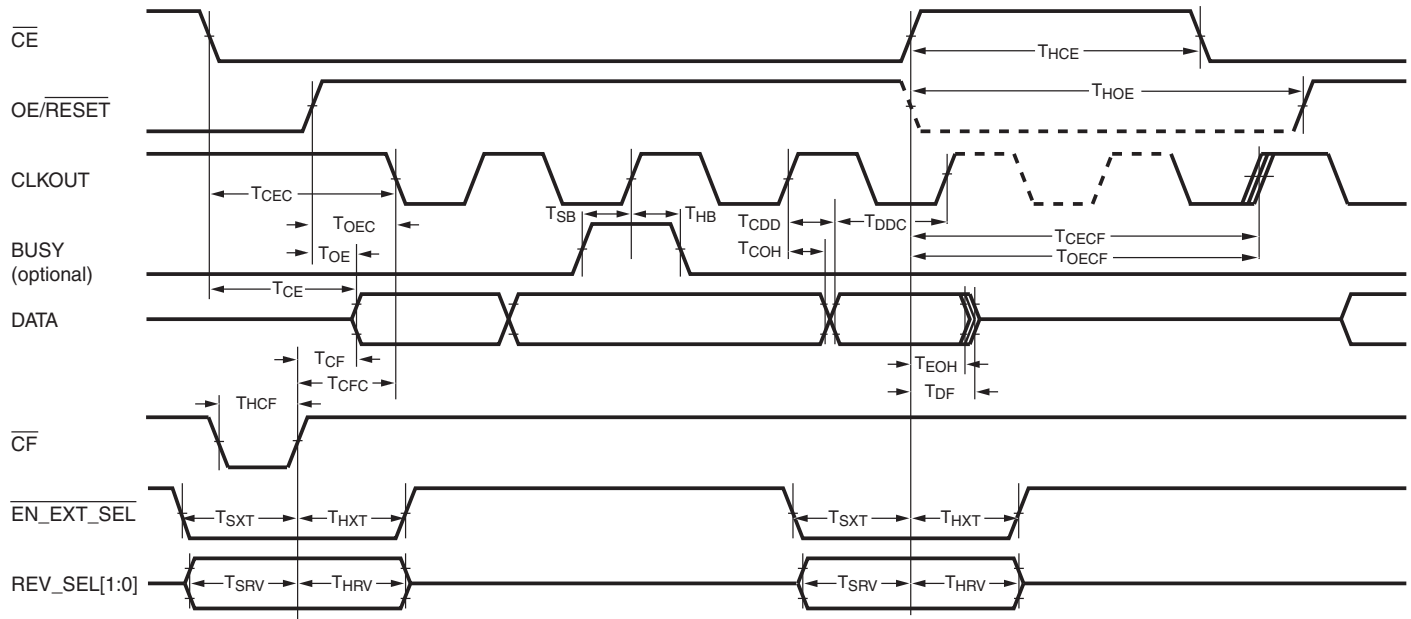
| Symbol            | Description  | XCF08P, XCF16P,<br>XCF32P |              | Units |
|-------------------|--|---------------------------|--------------|-------|
|                   |  | Min                       | Max          |       |
| T <sub>CYCO</sub> | Clock period <sup>(7)</sup> (serial mode) when V <sub>CCO</sub> = 3.3V or 2.5V   | 30                        | –            | ns    |
|                   | Clock period <sup>(7)</sup> (serial mode) when V <sub>CCO</sub> = 1.8V   | 30                        | –            | ns    |
|                   | Clock period <sup>(7)</sup> (parallel mode) when V <sub>CCO</sub> = 3.3V or 2.5V   | 35                        | –            | ns    |
|                   | Clock period <sup>(7)</sup> (parallel mode) when V <sub>CCO</sub> = 1.8V   | 35                        | –            | ns    |
| T <sub>LC</sub>   | CLK Low time <sup>(3)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V   | 12                        | –            | ns    |
|                   | CLK Low time <sup>(3)</sup> when V <sub>CCO</sub> = 1.8V   | 12                        | –            | ns    |
| T <sub>HC</sub>   | CLK High time <sup>(3)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | 12                        | –            | ns    |
|                   | CLK High time <sup>(3)</sup> when V <sub>CCO</sub> = 1.8V  | 12                        | –            | ns    |
| T <sub>HCE</sub>  | $\overline{CE}$ hold time (guarantees counters are reset) <sup>(5)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V                              | 2000                      | –            | ns    |
|                   | $\overline{CE}$ hold time (guarantees counters are reset) <sup>(5)</sup> when V <sub>CCO</sub> = 1.8V                                      | 2000                      | –            | ns    |
| T <sub>HOE</sub>  | OE/ $\overline{RESET}$ hold time (guarantees counters are reset) <sup>(6)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V                       | 2000                      | –            | ns    |
|                   | OE/ $\overline{RESET}$ hold time (guarantees counters are reset) <sup>(6)</sup> when V <sub>CCO</sub> = 1.8V                               | 2000                      | –            | ns    |
| T <sub>SB</sub>   | BUSY setup time to CLKOUT when V <sub>CCO</sub> = 3.3V or 2.5V   | 12                        | –            | ns    |
|                   | BUSY setup time to CLKOUT when V <sub>CCO</sub> = 1.8V   | 12                        | –            | ns    |
| T <sub>HB</sub>   | BUSY hold time to CLKOUT when V <sub>CCO</sub> = 3.3V or 2.5V  | 8                         | –            | ns    |
|                   | BUSY hold time to CLKOUT when V <sub>CCO</sub> = 1.8V  | 8                         | –            | ns    |
| T <sub>CLKO</sub> | CLK input to CLKOUT output delay when V <sub>CCO</sub> = 3.3V or 2.5V  | –                         | 35           | ns    |
|                   | CLK input to CLKOUT output delay when V <sub>CCO</sub> = 1.8V  | –                         | 35           | ns    |
|                   | CLK input to CLKOUT output delay when V <sub>CCO</sub> = 3.3V or 2.5V with decompression <sup>(12)</sup>                                   | –                         | 35           | ns    |
|                   | CLK input to CLKOUT output delay when V <sub>CCO</sub> = 1.8V with decompression <sup>(12)</sup>   | –                         | 35           | ns    |
| T <sub>CECC</sub> | $\overline{CE}$ to CLKOUT delay <sup>(8)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | 0                         | 2 CLK cycles | –     |
|                   | $\overline{CE}$ to CLKOUT delay <sup>(8)</sup> when V <sub>CCO</sub> = 1.8V  | 0                         | 2 CLK cycles | –     |
| T <sub>OECC</sub> | OE/ $\overline{RESET}$ to CLKOUT delay <sup>(8)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V   | 0                         | 2 CLK cycles | –     |
|                   | OE/ $\overline{RESET}$ to CLKOUT delay <sup>(8)</sup> when V <sub>CCO</sub> = 1.8V   | 0                         | 2 CLK cycles | –     |
| T <sub>CFCC</sub> | $\overline{CF}$ to CLKOUT delay <sup>(8)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | 0                         | –            | –     |
|                   | $\overline{CF}$ to CLKOUT delay <sup>(8)</sup> when V <sub>CCO</sub> = 1.8V  | 0                         | –            | –     |
| T <sub>CCDD</sub> | CLKOUT to data delay when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(9)</sup>   | –                         | 30           | ns    |
|                   | CLKOUT to data delay when V <sub>CCO</sub> = 1.8V <sup>(9)</sup>   | –                         | 30           | ns    |
| T <sub>DDC</sub>  | Data setup time to CLKOUT when V <sub>CCO</sub> = 3.3V or 2.5V with decompression <sup>(9)(12)</sup>                                       | 5                         | –            | ns    |
|                   | Data setup time to CLKOUT when V <sub>CCO</sub> = 1.8V with decompression <sup>(9)(12)</sup>   | 5                         | –            | ns    |
| T <sub>COH</sub>  | Data hold from CLKOUT when V <sub>CCO</sub> = 3.3V or 2.5V   | 3                         | –            | ns    |
|                   | Data hold from CLKOUT when V <sub>CCO</sub> = 1.8V   | 3                         | –            | ns    |
|                   | Data hold from CLKOUT when V <sub>CCO</sub> = 3.3V or 2.5V with decompression <sup>(12)</sup>  | 3                         | –            | ns    |
|                   | Data hold from CLKOUT when V <sub>CCO</sub> = 1.8V with decompression <sup>(12)</sup>  | 3                         | –            | ns    |
| T <sub>SXT</sub>  | $\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$ , $\overline{CE}$ , or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 3.3V or 2.5V | 300                       | –            | ns    |
|                   | $\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$ , $\overline{CE}$ , or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 1.8V         | 300                       | –            | ns    |

| Symbol           | Description   | XCF08P, XCF16P, XCF32P |     | Units |
|------------------|---|------------------------|-----|-------|
|                  |   | Min                    | Max |       |
| T <sub>HXT</sub> | $\overline{\text{EN\_EXT\_SEL}}$ hold time from $\overline{\text{CF}}$ , $\overline{\text{CE}}$ , or $\text{OE}/\overline{\text{RESET}}$ when $V_{\text{CCO}} = 3.3\text{V}$ or $2.5\text{V}$ | 300                    | –   | ns    |
|                  | $\overline{\text{EN\_EXT\_SEL}}$ hold time from $\overline{\text{CF}}$ , $\overline{\text{CE}}$ , or $\text{OE}/\overline{\text{RESET}}$ when $V_{\text{CCO}} = 1.8\text{V}$                  | 300                    | –   | ns    |
| T <sub>SRV</sub> | REV_SEL setup time to $\overline{\text{CF}}$ , $\overline{\text{CE}}$ , or $\text{OE}/\overline{\text{RESET}}$ when $V_{\text{CCO}} = 3.3\text{V}$ or $2.5\text{V}$                           | 300                    | –   | ns    |
|                  | REV_SEL setup time to $\overline{\text{CF}}$ , $\overline{\text{CE}}$ , or $\text{OE}/\overline{\text{RESET}}$ when $V_{\text{CCO}} = 1.8\text{V}$  | 300                    | –   | ns    |
| T <sub>HRV</sub> | REV_SEL hold time from $\overline{\text{CF}}$ , $\overline{\text{CE}}$ , or $\text{OE}/\overline{\text{RESET}}$ when $V_{\text{CCO}} = 3.3\text{V}$ or $2.5\text{V}$                          | 300                    | –   | ns    |
|                  | REV_SEL hold time from $\overline{\text{CF}}$ , $\overline{\text{CE}}$ , or $\text{OE}/\overline{\text{RESET}}$ when $V_{\text{CCO}} = 1.8\text{V}$   | 300                    | –   | ns    |

**Notes:**

- AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
- Float delays are measured with 5 pF AC loads. Transition is measured at  $\pm 200$  mV from steady-state active levels.
- Guaranteed by design, not tested.
- All AC parameters are measured with  $V_{\text{IL}} = 0.0\text{V}$  and  $V_{\text{IH}} = 3.0\text{V}$ .
- If  $T_{\text{HCE High}} < 2 \mu\text{s}$ ,  $T_{\text{CE}} = 2 \mu\text{s}$ .
- If  $T_{\text{HOE Low}} < 2 \mu\text{s}$ ,  $T_{\text{OE}} = 2 \mu\text{s}$ .
- This is the minimum possible  $T_{\text{CYCO}}$ . Actual  $T_{\text{CYCO}} = T_{\text{CCDD}} + \text{FPGA Data setup time}$ . *Example:* With the XCF32P in serial mode with  $V_{\text{CCO}}$  at 3.3V, if FPGA Data setup time = 15 ns, then the actual  $T_{\text{CYCO}} = 25 \text{ ns} + 15 \text{ ns} = 40 \text{ ns}$ .
- The delay before the enabled CLKOUT signal begins clocking data out of the device is dependent on the clocking configuration. The delay before CLKOUT is enabled increases if decompression is enabled.
- Slower CLK frequency option might be required to meet the FPGA data sheet setup time.
- When decompression is enabled, the CLKOUT signal becomes a controlled clock output. When decompressed data is available, CLKOUT toggles at  $\frac{1}{2}$  the source clock frequency (either  $\frac{1}{2}$  the selected internal clock frequency or  $\frac{1}{2}$  the external CLK input frequency). When decompressed data is not available, the CLKOUT pin is parked High. If CLKOUT is used, then it must be pulled High externally using a 4.7 k $\Omega$  pull-up to  $V_{\text{CCO}}$ .
- When JTAG CONFIG command is issued, PROM drives  $\overline{\text{CF}}$  Low for at least the  $T_{\text{HCF}}$  minimum.

XCFxxP PROM as Configuration Master with Internal Oscillator as Clock Source



**Note:** Typically, 8 CLKOUT cycles are output after CE rising edge, before CLKOUT tristates, if OE/RESET remains high, and terminal count has not been reached.

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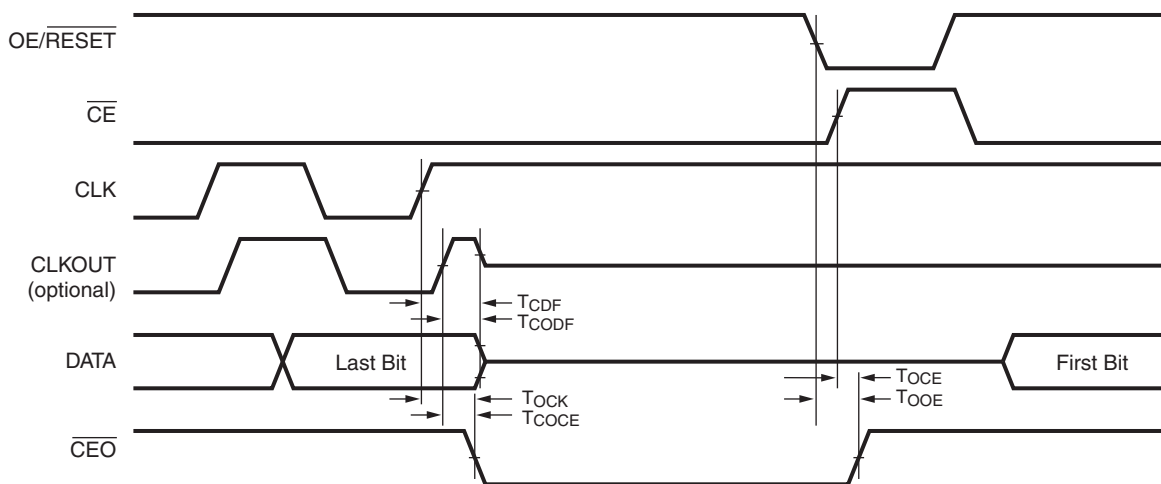
| Symbol             | Description  | XCF08P, XCF16P, XCF32P |     | Units |
|--------------------|--|------------------------|-----|-------|
|                    |  | Min                    | Max |       |
| T <sub>HCF</sub>   | $\overline{CF}$ hold time to guarantee design revision selection is sampled when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(12)</sup> | 300                    |     | 300   |
|                    | $\overline{CF}$ hold time to guarantee design revision selection is sampled when V <sub>CCO</sub> = 1.8V <sup>(12)</sup>         | 300                    |     | 300   |
| T <sub>CF</sub>    | $\overline{CF}$ to data delay when V <sub>CCO</sub> = 3.3V or 2.5V   | –                      |     | ns    |
|                    | $\overline{CF}$ to data delay when V <sub>CCO</sub> = 1.8V   | –                      |     | ns    |
| T <sub>OE</sub>    | OE/RESET to data delay <sup>(6)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V   | –                      | 25  | ns    |
|                    | OE/RESET to data delay <sup>(6)</sup> when V <sub>CCO</sub> = 1.8V   | –                      | 25  | ns    |
| T <sub>CE</sub>    | $\overline{CE}$ to data delay <sup>(5)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | –                      | 25  | ns    |
|                    | $\overline{CE}$ to data delay <sup>(5)</sup> when V <sub>CCO</sub> = 1.8V  | –                      | 25  | ns    |
| T <sub>EOH</sub>   | Data hold from $\overline{CE}$ , OE/RESET, or $\overline{CF}$ when V <sub>CCO</sub> = 3.3V or 2.5V                               | 5                      | –   | ns    |
|                    | Data hold from $\overline{CE}$ , OE/RESET, or $\overline{CF}$ when V <sub>CCO</sub> = 1.8V                                       | 5                      | –   | ns    |
| T <sub>DF</sub>    | $\overline{CE}$ or OE/RESET to data float delay <sup>(2)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V                              | –                      | 45  | ns    |
|                    | $\overline{CE}$ or OE/RESET to data float delay <sup>(2)</sup> when V <sub>CCO</sub> = 1.8V                                      | –                      | 45  | ns    |
| T <sub>OEFCF</sub> | OE/RESET to CLKOUT float delay <sup>(2)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V   | –                      |     | ns    |
|                    | OE/RESET to CLKOUT float delay <sup>(2)</sup> when V <sub>CCO</sub> = 1.8V   | –                      |     | ns    |
| T <sub>CEFCF</sub> | $\overline{CE}$ to CLKOUT float delay <sup>(2)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | –                      |     | ns    |
|                    | $\overline{CE}$ to CLKOUT float delay <sup>(2)</sup> when V <sub>CCO</sub> = 1.8V  | –                      |     | ns    |
| T <sub>HCE</sub>   | $\overline{CE}$ hold time (guarantees counters are reset) <sup>(5)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V                    | 2000                   | –   | ns    |
|                    | $\overline{CE}$ hold time (guarantees counters are reset) <sup>(5)</sup> when V <sub>CCO</sub> = 1.8V                            | 2000                   | –   | ns    |
| T <sub>HOE</sub>   | OE/RESET hold time (guarantees counters are reset) <sup>(6)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V                           | 2000                   | –   | ns    |
|                    | OE/RESET hold time (guarantees counters are reset) <sup>(6)</sup> when V <sub>CCO</sub> = 1.8V                                   | 2000                   | –   | ns    |

| Symbol           | Description   | XCF08P, XCF16P,<br>XCF32P |      | Units |
|------------------|---|---------------------------|------|-------|
|                  |   | Min                       | Max  |       |
| T <sub>SB</sub>  | BUSY setup time to CLKOUT when V <sub>CCO</sub> = 3.3V or 2.5V  | 12                        | –    | ns    |
|                  | BUSY setup time to CLKOUT when V <sub>CCO</sub> = 1.8V  | 12                        | –    | ns    |
| T <sub>HB</sub>  | BUSY hold time to CLKOUT when V <sub>CCO</sub> = 3.3V or 2.5V   | 8                         | –    | ns    |
|                  | BUSY hold time to CLKOUT when V <sub>CCO</sub> = 1.8V   | 8                         | –    | ns    |
| T <sub>CEC</sub> | $\overline{CE}$ to CLKOUT delay <sup>(7)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V   | 0                         | 1    | μs    |
|                  | $\overline{CE}$ to CLKOUT delay <sup>(7)</sup> when V <sub>CCO</sub> = 1.8V   | 0                         | 1    | μs    |
| T <sub>OEC</sub> | OE/ $\overline{RESET}$ to CLKOUT delay <sup>(7)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V  | 0                         | 1    | μs    |
|                  | OE/ $\overline{RESET}$ to CLKOUT delay <sup>(7)</sup> when V <sub>CCO</sub> = 1.8V  | 0                         | 1    | μs    |
| T <sub>CFC</sub> | $\overline{CF}$ to CLKOUT delay <sup>(7)</sup> when V <sub>CCO</sub> = 3.3V or 2.5V   | 0                         |      | –     |
|                  | $\overline{CF}$ to CLKOUT delay <sup>(7)</sup> when V <sub>CCO</sub> = 1.8V   | 0                         |      | –     |
| T <sub>CDD</sub> | CLKOUT to data delay when V <sub>CCO</sub> = 3.3V or 2.5V <sup>(8)</sup>  | –                         | 30   | ns    |
|                  | CLKOUT to data delay when V <sub>CCO</sub> = 1.8V <sup>(8)</sup>  | –                         | 30   | ns    |
| T <sub>DDC</sub> | Data setup time to CLKOUT when V <sub>CCO</sub> = 3.3V or 2.5V with decompression <sup>(8)(11)</sup>  | 5                         |      | ns    |
|                  | Data setup time to CLKOUT when V <sub>CCO</sub> = 1.8V with decompression <sup>(8)(11)</sup>  | 5                         |      | ns    |
| T <sub>COH</sub> | Data hold from CLKOUT when V <sub>CCO</sub> = 3.3V or 2.5V  | 3                         | –    | ns    |
|                  | Data hold from CLKOUT when V <sub>CCO</sub> = 1.8V  | 3                         | –    | ns    |
|                  | Data hold from CLKOUT when V <sub>CCO</sub> = 3.3V or 2.5V with decompression <sup>(11)</sup>   | 3                         | –    | ns    |
|                  | Data hold from CLKOUT when V <sub>CCO</sub> = 1.8V with decompression <sup>(11)</sup>   | 3                         | –    | ns    |
| T <sub>SXT</sub> | $\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$ , $\overline{CE}$ , or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 3.3V or 2.5V  | 300                       | –    | ns    |
|                  | $\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$ , $\overline{CE}$ , or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 1.8V          | 300                       | –    | ns    |
| T <sub>HXT</sub> | $\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$ , $\overline{CE}$ , or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 3.3V or 2.5V | 300                       | –    | ns    |
|                  | $\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$ , $\overline{CE}$ , or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 1.8V         | 300                       | –    | ns    |
| T <sub>SRV</sub> | REV_SEL setup time to $\overline{CF}$ , $\overline{CE}$ , or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 3.3V or 2.5V                    | 300                       | –    | ns    |
|                  | REV_SEL setup time to $\overline{CF}$ , $\overline{CE}$ , or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 1.8V                            | 300                       | –    | ns    |
| T <sub>HRV</sub> | REV_SEL hold time from $\overline{CF}$ , $\overline{CE}$ , or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 3.3V or 2.5V                   | 300                       | –    | ns    |
|                  | REV_SEL hold time from $\overline{CF}$ , $\overline{CE}$ , or OE/ $\overline{RESET}$ when V <sub>CCO</sub> = 1.8V                           | 300                       | –    | ns    |
| F <sub>F</sub>   | CLKOUT default (fast) frequency <sup>(9)</sup>  | 25                        | 50   | MHz   |
|                  | CLKOUT default (fast) frequency with decompression <sup>(11)</sup>  | 12.5                      | 25   | MHz   |
| F <sub>S</sub>   | CLKOUT alternate (slower) frequency <sup>(10)</sup>   | 12.5                      | 25   | MHz   |
|                  | CLKOUT alternate (slower) frequency with decompression <sup>(11)</sup>  | 6                         | 12.5 | MHz   |

**Notes:**

- AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
- Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady-state active levels.
- Guaranteed by design, not tested.
- All AC parameters are measured with V<sub>IL</sub> = 0.0V and V<sub>IH</sub> = 3.0V.
- If T<sub>HCE</sub> High < 2 μs, T<sub>CE</sub> = 2 μs.
- If T<sub>HOE</sub> Low < 2 μs, T<sub>OE</sub> = 2 μs.
- The delay before the enabled CLKOUT signal begins clocking data out of the device is dependent on the clocking configuration. The delay before CLKOUT is enabled increases if decompression is enabled.
- Slower CLK frequency option might be required to meet the FPGA data sheet setup time.
- Typical CLKOUT default (fast) period = 25 ns (40 MHz).
- Typical CLKOUT alternate (slower) period = 50 ns (20 MHz).
- When decompression is enabled, the CLKOUT signal becomes a controlled clock output. When decompressed data is available, CLKOUT toggles at ½ the source clock frequency (either ½ the selected internal clock frequency or ½ the external CLK input frequency). When decompressed data is not available, the CLKOUT pin is parked High. If CLKOUT is used, then it must be pulled High externally using a 4.7 kΩ pull-up to V<sub>CCO</sub>.
- When JTAG CONFIG command is issued, PROM drives  $\overline{CF}$  Low for at least the T<sub>HCF</sub> minimum.

## AC Characteristics Over Operating Conditions When Cascading



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| Symbol            | Description   | XCF01S, XCF02S, XCF04S |     | XCF08P, XCF16P, XCF32P |     | Units |
|-------------------|---|------------------------|-----|------------------------|-----|-------|
|                   |   | Min                    | Max | Min                    | Max |       |
| T <sub>CDF</sub>  | CLK to output float delay <sup>(2,3)</sup> when V <sub>CCO</sub> = 2.5V or 3.3V | –                      | 25  | –                      | 20  | ns    |
|                   | CLK to output float delay <sup>(2,3)</sup> when V <sub>CCO</sub> = 1.8V         | –                      | 35  | –                      | 20  | ns    |
| T <sub>OCK</sub>  | CLK to CEO delay <sup>(3,5)</sup> when V <sub>CCO</sub> = 2.5V or 3.3V          | –                      | 20  | –                      | 20  | ns    |
|                   | CLK to CEO delay <sup>(3,5)</sup> when V <sub>CCO</sub> = 1.8V                  | –                      | 35  | –                      | 20  | ns    |
| T <sub>OCE</sub>  | CE to CEO delay <sup>(3,6)</sup> when V <sub>CCO</sub> = 2.5V or 3.3V           | –                      | 20  | –                      | 80  | ns    |
|                   | CE to CEO delay <sup>(3,6)</sup> when V <sub>CCO</sub> = 1.8V                   | –                      | 35  | –                      | 80  | ns    |
| T <sub>OOE</sub>  | OE/RESET to CEO delay <sup>(3)</sup> when V <sub>CCO</sub> = 2.5V or 3.3V       | –                      | 20  | –                      | 80  | ns    |
|                   | OE/RESET to CEO delay <sup>(3)</sup> when V <sub>CCO</sub> = 1.8V               | –                      | 35  | –                      | 80  | ns    |
| T <sub>COCE</sub> | CLKOUT to CEO delay when V <sub>CCO</sub> = 2.5V or 3.3V                        | –                      | –   | –                      | 20  | ns    |
|                   | CLKOUT to CEO delay when V <sub>CCO</sub> = 1.8V                                | –                      | –   | –                      | 20  | ns    |
| T <sub>CODF</sub> | CLKOUT to output float delay when V <sub>CCO</sub> = 2.5V or 3.3V               | –                      | –   | –                      | 25  | ns    |
|                   | CLKOUT to output float delay when V <sub>CCO</sub> = 1.8V                       | –                      | –   | –                      | 25  | ns    |

### Notes:

- AC test load = 50 pF for XCF01S/XCF02S/XCF04S; 30 pF for XCF08P/XCF16P/XCF32P.
- Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
- Guaranteed by design, not tested.
- All AC parameters are measured with V<sub>IL</sub> = 0.0V and V<sub>IH</sub> = 3.0V.
- For cascaded PROMs, if the FPGA's dual-purpose configuration data pins are set to persist as configuration pins, the minimum period is increased based on the CLK to CEO and CE to data propagation delays:
  - T<sub>CYC</sub> minimum = T<sub>OCK</sub> + T<sub>CE</sub> + FPGA Data setup time
  - T<sub>CAC</sub> maximum = T<sub>OCK</sub> + T<sub>CE</sub>
- For cascaded PROMs, if the FPGA's dual-purpose configuration data pins become general I/O pins after configuration; to allow for the disable to propagate to the cascaded PROMs and to avoid contention on the data lines following configuration, the minimum period is increased based on the CE to CEO and CE to data propagation delays:
  - T<sub>CYC</sub> minimum = T<sub>OCE</sub> + T<sub>CE</sub>
  - T<sub>CAC</sub> maximum = T<sub>OCK</sub> + T<sub>CE</sub>



## Pinouts and Pin Descriptions

The XCFxxS Platform Flash PROM is available in the VO20 and VOG20 packages. The XCFxxP Platform Flash PROM is available in the VO48, VOG48, FS48, and FSG48 packages. For package drawings, specifications, and additional information, see *Device Package User Guide*, or the [Xilinx Package Specifications](#).

### Note:

1. VO20/VOG20 denotes a 20-pin (TSSOP) Plastic Thin Shrink Small Outline Package.
2. VO48/VOG48 denotes a 48-pin (TSOP) Plastic Thin Small Outline Package.
3. FS48/FSG48 denotes a 48-pin (TFBGA) Plastic Thin Fine Pitch Ball Grid Array (0.8 mm pitch).

## XCFxxS Pinouts and Pin Descriptions

### XCFxxS VO20/VOG20 Pin Names and Descriptions

Table 13 provides a list of the pin names and descriptions for the XCFxxS 20-pin VO20/VOG20 package.

Table 13: XCFxxS Pin Names and Descriptions

| Pin Name              | Boundary Scan Order | Boundary-Scan Function | Pin Description   | 20-pin TSSOP (VO20/VOG20) |
|-----------------------|---------------------|------------------------|---|---------------------------|
| D0                    | 4                   | Data Out               | D0 is the DATA output pin to provide data for configuring an FPGA in serial mode. The D0 output is set to a high-impedance state during ISPEN (when not clamped).   | 1                         |
|                       | 3                   | Output Enable          |   |                           |
| CLK                   | 0                   | Data In                | Configuration Clock Input. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected, $\overline{CE}$ is Low, and $OE/\overline{RESET}$ is High.   | 3                         |
| $OE/\overline{RESET}$ | 20                  | Data In                | Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA output is in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable.   | 8                         |
|                       | 19                  | Data Out               |   |                           |
|                       | 18                  | Output Enable          |   |                           |
| $\overline{CE}$       | 15                  | Data In                | Chip Enable Input. When $\overline{CE}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA pins are put in a high-impedance state.  | 10                        |
| $\overline{CF}$       | 22                  | Data Out               | Configuration Pulse (Open-Drain Output). Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.  | 7                         |
|                       | 21                  | Output Enable          |   |                           |
| $\overline{CEO}$      | 12                  | Data Out               | Chip Enable Output. Chip Enable Output ( $\overline{CEO}$ ) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and $OE/\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. $\overline{CEO}$ returns to High when $OE/\overline{RESET}$ goes Low or $\overline{CE}$ goes High. | 13                        |
|                       | 11                  | Output Enable          |   |                           |
| TMS                   | –                   | Mode Select            | JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50 K $\Omega$ resistive pull-up to $V_{CCJ}$ to provide a logic 1 to the device if the pin is not driven.   | 5                         |
| TCK                   | –                   | Clock                  | JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.   | 6                         |
| TDI                   | –                   | Data In                | JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50 K $\Omega$ resistive pull-up to $V_{CCJ}$ to provide a logic 1 to the device if the pin is not driven.  | 4                         |

Table 13: XCFxxS Pin Names and Descriptions (Cont'd)

| Pin Name | Boundary Scan Order | Boundary-Scan Function | Pin Description  | 20-pin TSSOP (VO20/VOG20) |
|----------|---------------------|------------------------|--|---------------------------|
| TDO      | –                   | Data Out               | JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50 KΩ resistive pull-up to V <sub>CCJ</sub> to provide a logic 1 to the system if the pin is not driven. | 17                        |
| VCCINT   | –                   | –                      | +3.3V Supply. Positive 3.3V supply voltage for internal logic.   | 18                        |
| VCCO     | –                   | –                      | +3.3V, 2.5V, or 1.8V I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the output voltage drivers and input buffers.  | 19                        |
| VCCJ     | –                   | –                      | +3.3V or 2.5V JTAG I/O Supply. Positive 3.3V or 2.5V supply voltage connected to the TDO output voltage driver and TCK, TMS, and TDI input buffers.  | 20                        |
| GND      | –                   | –                      | Ground   | 11                        |
| DNC      | –                   | –                      | Do not connect. (These pins must be left unconnected.)   | 2, 9, 12, 14, 15, 16      |

**XCFxxS VO20/VOG20 Pinout Diagram**

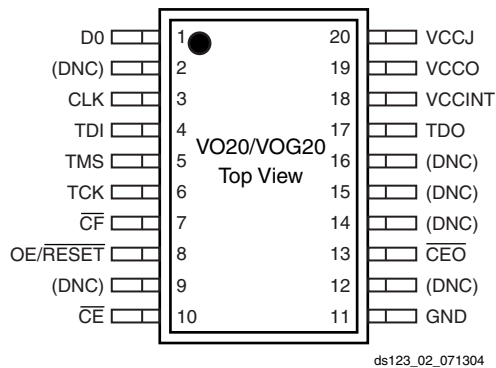


Figure 19: VO20/VOG20 Pinout Diagram (Top View) with Pin Names

## XCFxxP Pinouts and Pin Descriptions

### XCFxxP VO48/VOG48 and FS48/FSG48 Pin Names and Descriptions

Table 14 provides a list of the pin names and descriptions for the XCFxxP 48-pin VO48/VOG48 and 48-pin FS48/FSG48 packages.

Table 14: XCFxxP Pin Names and Descriptions (VO48/VOG48 and FS48/FSG48)

| Pin Name              | Boundary-Scan Order | Boundary-Scan Function | Pin Description   | 48-pin TSOP (VO48/VOG48) | 48-pin TFBGA (FS48/FSG48) |
|-----------------------|---------------------|------------------------|---|--------------------------|---------------------------|
| D0                    | 28                  | Data Out               | D0 is the DATA output pin to provide data for configuring an FPGA in serial mode.<br>D0-D7 are the DATA output pins to provide parallel data for configuring a Xilinx FPGA in SelectMap (parallel) mode. The D0 output is set to a high-impedance state during ISPEN (when not clamped).<br>The D1-D7 outputs are set to a high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. The D1-D7 pins can be left unconnected when the PROM is used in serial mode.  | 28                       | H6                        |
|                       | 27                  | Output Enable          |   |                          |                           |
| D1                    | 26                  | Data Out               |   | 29                       | H5                        |
|                       | 25                  | Output Enable          |   |                          |                           |
| D2                    | 24                  | Data Out               |   | 32                       | E5                        |
|                       | 23                  | Output Enable          |   |                          |                           |
| D3                    | 22                  | Data Out               |   | 33                       | D5                        |
|                       | 21                  | Output Enable          |   |                          |                           |
| D4                    | 20                  | Data Out               |   | 43                       | C5                        |
|                       | 19                  | Output Enable          |   |                          |                           |
| D5                    | 18                  | Data Out               |   | 44                       | B5                        |
|                       | 17                  | Output Enable          |   |                          |                           |
| D6                    | 16                  | Data Out               |   | 47                       | A5                        |
|                       | 15                  | Output Enable          |   |                          |                           |
| D7                    | 14                  | Data Out               | 48  | A6                       |                           |
|                       | 13                  | Output Enable          |   |                          |                           |
| CLK                   | 01                  | Data In                | Configuration Clock Input. An internal programmable control bit selects between the internal oscillator and the CLK input pin as the clock source to control the configuration sequence. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected, $\overline{CE}$ is Low, $OE/\overline{RESET}$ is High, $BUSY$ is Low (parallel mode only), and $\overline{CF}$ is High.  | 12                       | B3                        |
| $OE/\overline{RESET}$ | 04                  | Data In                | Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable.   | 11                       | A3                        |
|                       | 03                  | Data Out               |   |                          |                           |
|                       | 02                  | Output Enable          |   |                          |                           |
| $\overline{CE}$       | 00                  | Data In                | Chip Enable Input. When $\overline{CE}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high-impedance state.   | 13                       | B4                        |
| $\overline{CF}$       | 11                  | Data In                | Configuration Pulse (Open-Drain I/O). As an output, this pin allows the JTAG CONFIG instruction to initiate FPGA configuration without powering down the FPGA. This is an open-drain signal that is pulsed Low by the JTAG CONFIG command. As an input, on the rising edge of $\overline{CF}$ , the current design revision selection is sampled and the internal address counter is reset to the start address for the selected revision. If unused, the $\overline{CF}$ pin must be pulled High using an external 4.7 K $\Omega$ pull-up to $V_{CC0}$ . | 6                        | D1                        |
|                       | 10                  | Data Out               |   |                          |                           |
|                       | 09                  | Output Enable          |   |                          |                           |

Table 14: XCFxxP Pin Names and Descriptions (VO48/VOG48 and FS48/FSG48) (Cont'd)

| Pin Name                         | Boundary-Scan Order | Boundary-Scan Function | Pin Description  | 48-pin TSOP (VO48/VOG48) | 48-pin TFBGA (FS48/FSG48) |
|----------------------------------|---------------------|------------------------|--|--------------------------|---------------------------|
| $\overline{\text{CEO}}$          | 06                  | Data Out               | Chip Enable Output. Chip Enable Output ( $\overline{\text{CEO}}$ ) is connected to the $\overline{\text{CE}}$ input of the next PROM in the chain. This output is Low when $\overline{\text{CE}}$ is Low and OE/RESET input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value or the PROM does not contain any blocks that correspond to the selected revision. CEO returns to High when OE/RESET goes Low or $\overline{\text{CE}}$ goes High.  | 10                       | D2                        |
|                                  | 05                  | Output Enable          |  |                          |                           |
| $\overline{\text{EN\_EXT\_SEL}}$ | 31                  | Data In                | Enable External Selection Input. When this pin is Low, design revision selection is controlled by the Revision Select pins. When this pin is High, design revision selection is controlled by the internal programmable Revision Select control bits. $\overline{\text{EN\_EXT\_SEL}}$ has an internal 50 K $\Omega$ resistive pull-up to V <sub>CC0</sub> to provide a logic 1 to the device if the pin is not driven.  | 25                       | H4                        |
| REV_SEL0                         | 30                  | Data In                | Revision Select[1:0] Inputs. When the $\overline{\text{EN\_EXT\_SEL}}$ is Low, the Revision Select pins are used to select the design revision to be enabled, overriding the internal programmable Revision Select control bits. The Revision Select[1:0] inputs have an internal 50 K $\Omega$ resistive pull-up to V <sub>CC0</sub> to provide a logic 1 to the device if the pins are not driven.   | 26                       | G3                        |
| REV_SEL1                         | 29                  | Data In                |  | 27                       | G4                        |
| BUSY                             | 12                  | Data In                | Busy Input. The BUSY input is enabled when parallel mode is selected for configuration. When BUSY is High, the internal address counter stops incrementing and the current data remains on the data pins. On the first rising edge of CLK after BUSY transitions from High to Low, the data for the next address is driven on the data pins. When serial mode or decompression is enabled during device programming, the BUSY input is disabled. BUSY has an internal 50 K $\Omega$ resistive pull-down to GND to provide a logic 0 to the device if the pin is not driven.  | 5                        | C1                        |
| CLKOUT                           | 08                  | Data Out               | Configuration Clock Output. An internal Programmable control bit enables the CLKOUT signal, which is sourced from either the internal oscillator or the CLK input pin. Each rising edge of the selected clock source increments the internal address counter if data is available, $\overline{\text{CE}}$ is Low, and OE/RESET is High. Output data is available on the rising edge of CLKOUT. CLKOUT is disabled if $\overline{\text{CE}}$ is High or OE/RESET is Low. If decompression is enabled, CLKOUT is parked High when decompressed data is not ready. When CLKOUT is disabled, the CLKOUT pin is put into a high-Z state. If CLKOUT is used, then it must be pulled High externally using a 4.7 K $\Omega$ pull-up to V <sub>CC0</sub> . | 9                        | C2                        |
|                                  | 07                  | Output Enable          |  |                          |                           |
| TMS                              | –                   | Mode Select            | JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50 K $\Omega$ resistive pull-up to V <sub>CCJ</sub> to provide a logic 1 to the device if the pin is not driven.   | 21                       | E2                        |
| TCK                              | –                   | Clock                  | JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.  | 20                       | H3                        |
| TDI                              | –                   | Data In                | JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50 K $\Omega$ resistive pull-up to V <sub>CCJ</sub> to provide a logic 1 to the device if the pin is not driven.  | 19                       | G1                        |
| TDO                              | –                   | Data Out               | JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50K $\Omega$ resistive pull-up to V <sub>CCJ</sub> to provide a logic 1 to the system if the pin is not driven.  | 22                       | E6                        |

Table 14: XCFxxP Pin Names and Descriptions (VO48/VOG48 and FS48/FSG48) (Cont'd)

| Pin Name | Boundary-Scan Order | Boundary-Scan Function | Pin Description   | 48-pin TSOP (VO48/VOG48)                 | 48-pin TFBGA (FS48/FSG48)                  |
|----------|---------------------|------------------------|---|--|--|
| VCCINT   | –                   | –                      | +1.8V Supply. Positive 1.8V supply voltage for internal logic.  | 4, 15, 34                                | B1, E1, G6                                 |
| VCCO     | –                   | –                      | +3.3V, 2.5V, 1.8V, or 1.5V I/O Supply. Positive 3.3V, 2.5V, 1.8V, or 1.5V supply voltage connected to the output voltage drivers and input buffers. | 8, 30, 38, 45                            | B2, C6, D6, G5                             |
| VCCJ     | –                   | –                      | +3.3V or 2.5V JTAG I/O Supply. Positive 3.3V or 2.5V supply voltage connected to the TDO output voltage driver and TCK, TMS, and TDI input buffers. | 24                                       | H2   |
| GND      | –                   | –                      | Ground  | 2, 7, 17, 23, 31, 36, 46                 | A1, A2, B6, F1, F5, F6, H1                 |
| DNC      | –                   | –                      | Do Not Connect. (These pins must be left unconnected.)  | 1, 3, 14, 16, 18, 35, 37, 39, 40, 41, 42 | A4, C3, C4, D3, D4, E3, E4, F2, F3, F4, G2 |

XCFxxP VO48/VOG48 Pinout Diagram

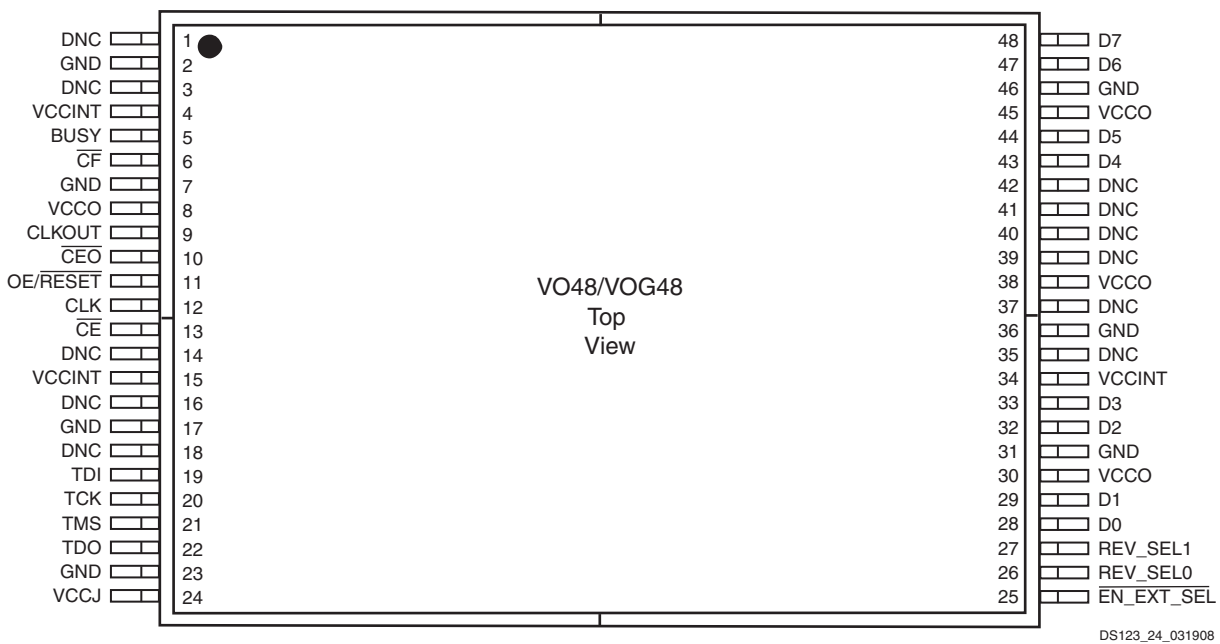
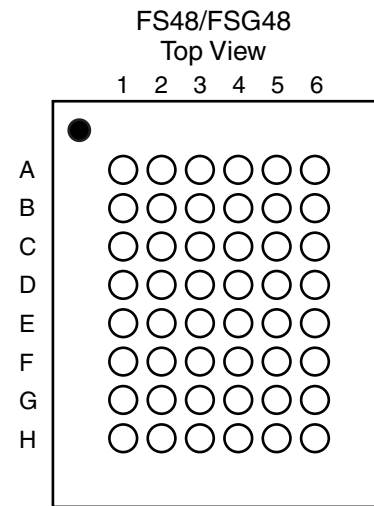


Figure 20: VO48/VOG48 Pinout Diagram (Top View) with Pin Names

**XCFxxP FS48/FSG48 Pin Names**

Table 15: XCFxxP Pin Names (FS48/FSG48)

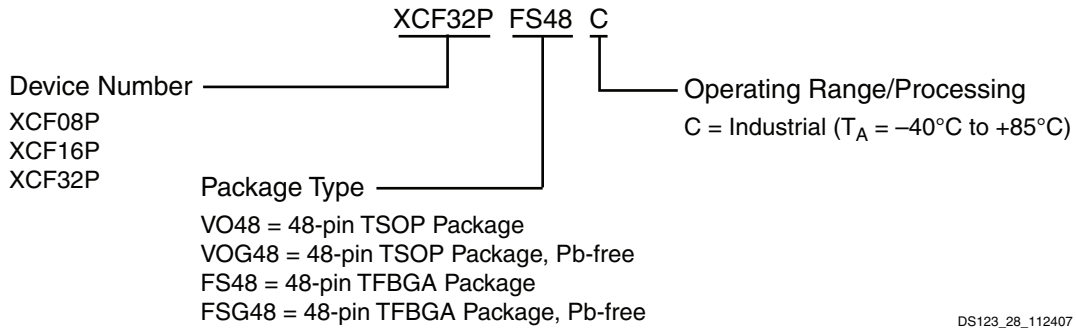
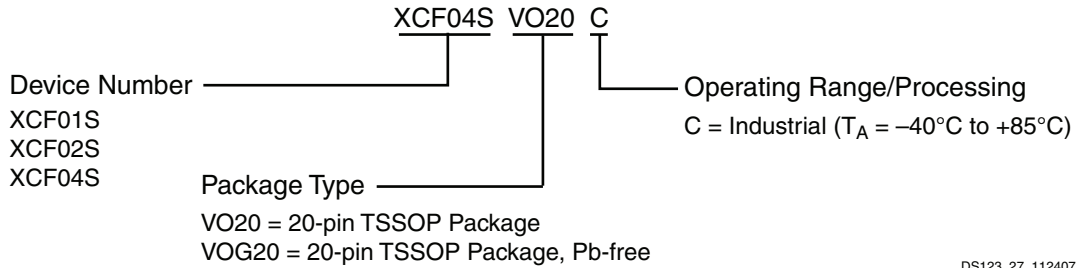
| Pin Number | Pin Name                      | Pin Number | Pin Name                         |
|------------|-------------------------------|------------|----------------------------------|
| A1         | GND                           | E1         | VCCINT                           |
| A2         | GND                           | E2         | TMS                              |
| A3         | OE/ $\overline{\text{RESET}}$ | E3         | DNC                              |
| A4         | DNC                           | E4         | DNC                              |
| A5         | D6                            | E5         | D2                               |
| A6         | D7                            | E6         | TDO                              |
| B1         | VCCINT                        | F1         | GND                              |
| B2         | VCCO                          | F2         | DNC                              |
| B3         | CLK                           | F3         | DNC                              |
| B4         | $\overline{\text{CE}}$        | F4         | DNC                              |
| B5         | D5                            | F5         | GND                              |
| B6         | GND                           | F6         | GND                              |
| C1         | BUSY                          | G1         | TDI                              |
| C2         | CLKOUT                        | G2         | DNC                              |
| C3         | DNC                           | G3         | REV_SEL0                         |
| C4         | DNC                           | G4         | REV_SEL1                         |
| C5         | D4                            | G5         | VCCO                             |
| C6         | VCCO                          | G6         | VCCINT                           |
| D1         | $\overline{\text{CF}}$        | H1         | GND                              |
| D2         | $\overline{\text{CEO}}$       | H2         | VCCJ                             |
| D3         | DNC                           | H3         | TCK                              |
| D4         | DNC                           | H4         | $\overline{\text{EN\_EXT\_SEL}}$ |
| D5         | D3                            | H5         | D1                               |
| D6         | VCCO                          | H6         | D0                               |

**XCFxxP FS48/FSG48 Pinout Diagram**


ds121\_01\_071604

Figure 21: FS48/FSG48 Pinout Diagram (Top View)

## Ordering Information



## Valid Ordering Combinations

|              |              |             |               |               |               |
|--------------|--------------|-------------|---------------|---------------|---------------|
| XCF01SVO20 C | XCF08PVO48 C | XCF08PF48 C | XCF01SVOG20 C | XCF08PVOG48 C | XCF08PFSG48 C |
| XCF02SVO20 C | XCF16PVO48 C | XCF16PF48 C | XCF02SVOG20 C | XCF16PVOG48 C | XCF16PFSG48 C |
| XCF04SVO20 C | XCF32PVO48 C | XCF32PF48 C | XCF04SVOG20 C | XCF32PVOG48 C | XCF32PFSG48 C |

## Marking Information

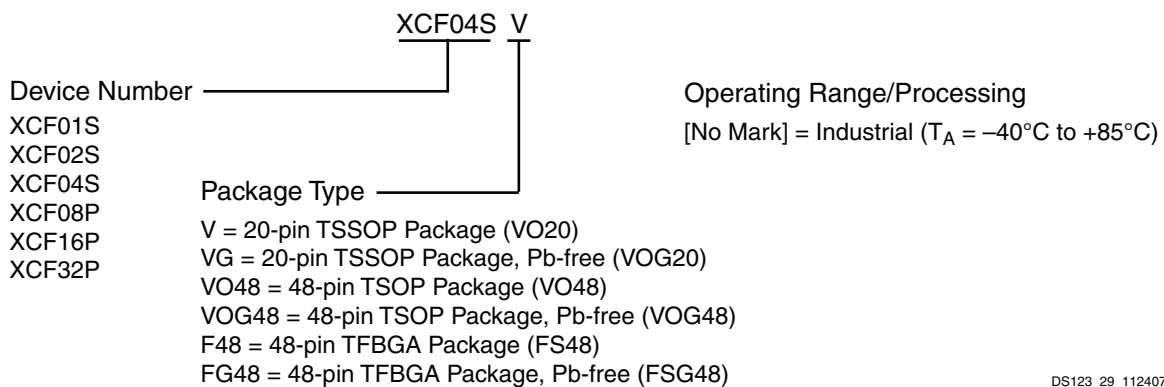




Figure 22 through Figure 24 illustrate the part markings for each available package.

**Note:** Package types can differ from the samples shown.

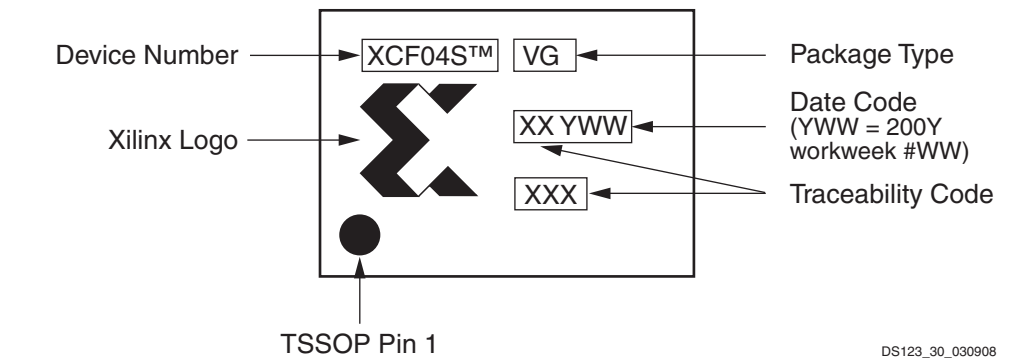


Figure 22: 20-Pin TSSOP Marking

DS123\_30\_030908

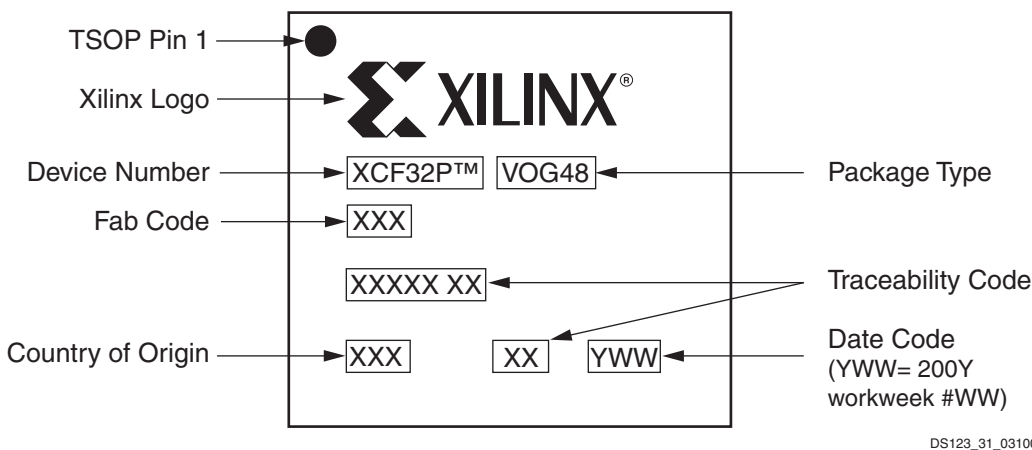


Figure 23: 48-Pin TSOP Marking

DS123\_31\_031008

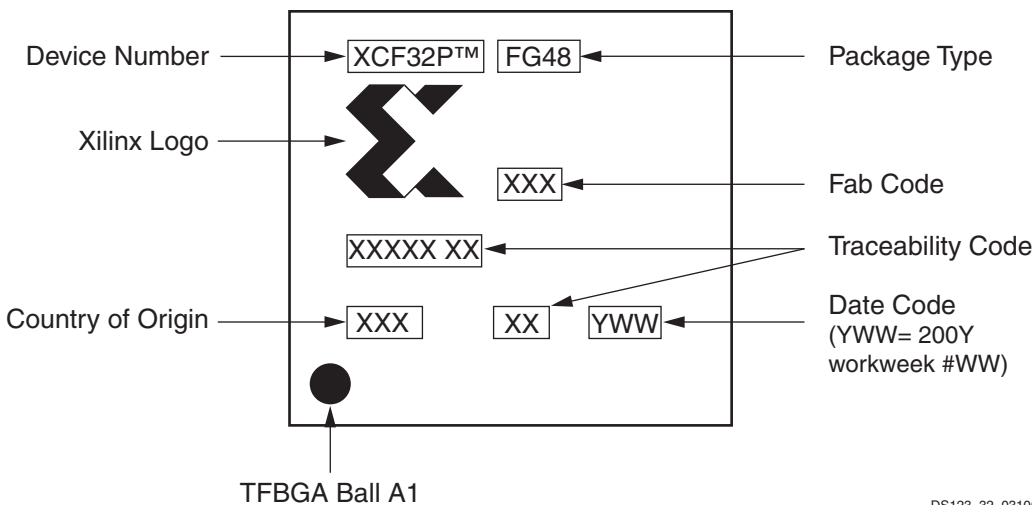


Figure 24: 48-Pin TFBGA Marking

DS123\_32\_031008

## Revision History

The following table shows the revision history for this document.

| Date     | Version | Revision  |
|----------|---------|---|
| 04/29/03 | 1.0     | Xilinx Initial Release.   |
| 06/03/03 | 1.1     | Made edits to all pages.  |
| 11/05/03 | 2.0     | Major revision.   |
| 11/18/03 | 2.1     | Pinout corrections as follows: <ul style="list-style-type: none"> <li>• <a href="#">Table 14</a>:                             <ul style="list-style-type: none"> <li>◆ For VO48 package, removed 38 from VCCINT and added it to VCCO.</li> <li>◆ For FS48 package, removed pin D6 from VCCINT and added it to VCCO.</li> </ul> </li> <li>• <a href="#">Table 15</a> (FS48 package):                             <ul style="list-style-type: none"> <li>◆ For pin D6, changed name from VCCINT to VCCO.</li> <li>◆ For pin A4, changed name from GND to DNC.</li> </ul> </li> <li>• <a href="#">Figure 16</a> (VO48 package): For pin 38, changed name from VCCINT to VCCO.</li> </ul>   |
| 12/15/03 | 2.2     | <ul style="list-style-type: none"> <li>• Added specification (4.7k<math>\Omega</math>) for recommended pull-up resistor on OE/<math>\overline{\text{RESET}}</math> pin to section "<a href="#">Reset and Power-On Reset Activation</a>," <a href="#">page 25</a>.</li> <li>• Added paragraph to section "<a href="#">Standby Mode</a>," <a href="#">page 26</a>, concerning use of a pull-up resistor and/or buffer on the DONE pin.</li> </ul>   |
| 05/07/04 | 2.3     | <ul style="list-style-type: none"> <li>• Section "<a href="#">Features</a>," <a href="#">page 1</a>: Added package styles and 33 MHz configuration speed limit to itemized features.</li> <li>• Section "<a href="#">Description</a>," <a href="#">page 1</a> and following: Added state conditions for <math>\overline{\text{CF}}</math> and BUSY to the descriptive text.</li> <li>• <a href="#">Table 2</a>, <a href="#">page 3</a>: Updated Virtex-II configuration bitstream sizes.</li> <li>• Section "<a href="#">Design Revisioning</a>," <a href="#">page 10</a>: Rewritten.</li> <li>• Section "<a href="#">PROM to FPGA Configuration Mode and Connections Summary</a>," <a href="#">page 13</a> and following, five instances: Added instruction to tie <math>\overline{\text{CF}}</math> High if it is not tied to the FPGA's PROG_B (PROGRAM) input.</li> <li>• <a href="#">Figure 6</a>, <a href="#">page 16</a>, through <a href="#">Figure 13</a>, <a href="#">page 23</a>: Added footnote indicating the directionality of the <math>\overline{\text{CF}}</math> pin in each configuration.</li> <li>• Section "<a href="#">I/O Input Voltage Tolerance and Power Sequencing</a>," <a href="#">page 25</a>: Rewritten.</li> <li>• <a href="#">Table 12</a>, <a href="#">page 25</a>: Added <math>\overline{\text{CF}}</math> column to truth table, and added an additional row to document the Low state of <math>\overline{\text{CF}}</math>.</li> <li>• Section "<a href="#">Absolute Maximum Ratings</a>," <a href="#">page 27</a>: Revised <math>V_{\text{IN}}</math> and <math>V_{\text{TS}}</math> for 'P' devices.</li> <li>• Section "<a href="#">Supply Voltage Requirements for Power-On Reset and Power-Down</a>," <a href="#">page 27</a>:                             <ul style="list-style-type: none"> <li>◆ Revised footnote callout number on <math>T_{\text{OER}}</math> from Footnote (4) to Footnote (3).</li> <li>◆ Added Footnote (2) callout to <math>T_{\text{VCC}}</math>.</li> </ul> </li> <li>• Section "<a href="#">Recommended Operating Conditions</a>," <a href="#">page 28</a>:                             <ul style="list-style-type: none"> <li>◆ Added Typical (Typ) parameter columns and parameters for <math>V_{\text{CCINT}}</math> and <math>V_{\text{CCO}}/V_{\text{CCJ}}</math>.</li> <li>◆ Added 1.5V operation parameter row to <math>V_{\text{IL}}</math> and <math>V_{\text{IH}}</math>, 'P' devices.</li> <li>◆ Revised <math>V_{\text{IH}}</math> Min, 2.5V operation, from 2.0V to 1.7V.</li> <li>◆ Added parameter row <math>T_{\text{IN}}</math> and Max parameters</li> </ul> </li> <li>• (Continued on next page)</li> <li>• Section "<a href="#">DC Characteristics Over Operating Conditions</a>," <a href="#">page 29</a>:                             <ul style="list-style-type: none"> <li>◆ Added parameter row and parameters for parallel configuration mode, 'P' devices, to <math>I_{\text{CCO}}</math>.</li> <li>◆ Added Footnote (1) and Footnote (2) with callouts in the Test Conditions column for <math>I_{\text{CCJ}}</math>, <math>I_{\text{CCINTS}}</math>, <math>I_{\text{CCOS}}</math>, and <math>I_{\text{CCJS}}</math>, to define active and standby mode requirements.</li> </ul> </li> <li>• Section "<a href="#">AC Characteristics Over Operating Conditions</a>," <a href="#">page 30</a>:                             <ul style="list-style-type: none"> <li>◆ Corrected description for second <math>T_{\text{CAC}}</math> parameter line to show parameters for 1.8V <math>V_{\text{CCO}}</math>.</li> <li>◆ Revised Footnote (7) to indicate <math>V_{\text{CCO}} = 3.3\text{V}</math>.</li> <li>◆ Applied Footnote (7) to second <math>T_{\text{CYC}}</math> parameter line.</li> </ul> </li> <li>• Section "<a href="#">AC Characteristics Over Operating Conditions When Cascading</a>," <a href="#">page 37</a>: Revised Footnote (5) <math>T_{\text{CYC}}</math> Min and <math>T_{\text{CAC}}</math> Min formulas.</li> <li>• <a href="#">Table 14</a>, <a href="#">page 39</a>:                             <ul style="list-style-type: none"> <li>◆ Added additional state conditions to CLK description.</li> <li>◆ Added function of resetting the internal address counter to <math>\overline{\text{CF}}</math> description.</li> </ul> </li> </ul> |

|          |     |  |
|----------|-----|--|
| 07/20/04 | 2.4 | <ul style="list-style-type: none"> <li>Added Pb-free package options VOG20, FSG48, and VOG48.</li> <li><a href="#">Figure 6, page 16</a>, and <a href="#">Figure 7, page 17</a>: Corrected connection name for FPGA DOUT (OPTIONAL Daisy-chained Slave FPGAs with different configurations) from DOUT to DIN.</li> <li>Section "<a href="#">Absolute Maximum Ratings</a>," <a href="#">page 27</a>: Removed parameter <math>T_{SOL}</math> from table. (<math>T_{SOL}</math> information can be found in <i>Package User Guide</i>.)</li> <li><a href="#">Table 2, page 3</a>: Removed reference to XC2VP125 FPGA.</li> </ul>  |
| 10/18/04 | 2.5 | <ul style="list-style-type: none"> <li><a href="#">Table 1, page 1</a>: Broke out <math>V_{CCO}</math> / <math>V_{CCJ}</math> into two separate columns.</li> <li><a href="#">Table 9, page 9</a>: Added clarification of ID code die revision bits.</li> <li><a href="#">Table 10, page 10</a>: Deleted <math>T_{CKMIN2}</math> (bypass mode) and renamed <math>T_{CKMIN1}</math> to <math>T_{CKMIN}</math>.</li> <li>Table "<a href="#">Recommended Operating Conditions</a>," <a href="#">page 28</a>: Separated <math>V_{CCO}</math> and <math>V_{CCJ}</math> parameters.</li> <li>Table "<a href="#">DC Characteristics Over Operating Conditions</a>," <a href="#">page 29</a>: <ul style="list-style-type: none"> <li>Added most parameter values for XCF08P, XCF16P, XCF32P devices.</li> <li>Added Footnote (1) to <math>I_{CCO}</math> specifying no-load conditions.</li> </ul> </li> <li>Table "<a href="#">AC Characteristics Over Operating Conditions</a>," <a href="#">page 30</a>: <ul style="list-style-type: none"> <li>Added most parameter values for XCF08P, XCF16P, XCF32P devices.</li> <li>Expanded Footnote (1) to include XCF08P, XCF16P, XCF32P devices.</li> <li>Added Footnote (8) through (11) relating to CLKOUT conditions for various parameters.</li> <li>Added rows to <math>T_{CYC}</math> specifying parameters for parallel mode.</li> <li>Added rows specifying parameters with decompression for <math>T_{CLKO}</math>, <math>T_{COH}</math>, <math>T_{FF}</math>, <math>T_{SF}</math></li> <li>Added <math>T_{DDC}</math> (setup time with decompression).</li> </ul> </li> <li>Table "<a href="#">AC Characteristics Over Operating Conditions When Cascading</a>," <a href="#">page 37</a>: <ul style="list-style-type: none"> <li>Added most parameter values for XCF08P, XCF16P, XCF32P devices.</li> <li>Separated Footnote (5) into Footnotes (5) and (6) to specify different derivations of <math>T_{CYC}</math>, depending on whether dual-purpose configuration pins persist as configuration pins, or become general I/O pins after configuration.</li> </ul> </li> </ul> |
| 03/14/05 | 2.6 | <ul style="list-style-type: none"> <li>Added Virtex-4 LX/FX/SX configuration data to <a href="#">Table 2</a>.</li> <li>Corrected Virtex-II configuration data in <a href="#">Table 2</a>.</li> <li>Corrected Virtex-II Pro configuration data in <a href="#">Table 2</a>.</li> <li>Added Spartan-3L configuration data to <a href="#">Table 2</a>.</li> <li>Added Spartan-3E configuration data to <a href="#">Table 2</a>.</li> <li>Paragraph added to <i>FPGA Master SelectMAP (Parallel) Mode (1)</i>, <a href="#">Page 14</a>.</li> <li>Changes to DC Characteristics <ul style="list-style-type: none"> <li><math>T_{OER}</math> changed, <a href="#">Page 29</a>.</li> <li><math>I_{OL}</math> changed for <math>V_{OL}</math>, <a href="#">Page 29</a>.</li> <li><math>V_{CCO}</math> added to test conditions for <math>I_{IL}</math>, <math>I_{ILP}</math>, <math>I_{IHP}</math> and <math>I_H</math>, <a href="#">Page 29</a>. Values modified for <math>I_{ILP}</math> and <math>I_{IHP}</math>.</li> </ul> </li> <li>Changes to AC Characteristics <ul style="list-style-type: none"> <li><math>T_{LC}</math> and <math>T_{HC}</math> modified for 1.8V, <a href="#">Page 33</a>.</li> <li>New rows added for <math>T_{CEC}</math> and <math>T_{OEC}</math>, <a href="#">Page 32</a>.</li> </ul> </li> <li>Minor changes to grammar and punctuation.</li> <li>Added explanation of "Preliminary" to DC and AC Electrical Characteristics.</li> </ul>   |
| 07/11/05 | 2.7 | <ul style="list-style-type: none"> <li>Move from "Preliminary" to "Product Specification"</li> <li>Corrections to Virtex-4 configuration bitstream values</li> <li>Minor changes to <a href="#">Figure 7, page 17</a>, <a href="#">Figure 12, page 22</a>, <a href="#">Figure 13, page 23</a>, and <a href="#">Figure 16, page 31</a></li> <li>Change to "<a href="#">Internal Oscillator</a>," <a href="#">page 10</a> description</li> <li>Change to "<a href="#">CLKOUT</a>," <a href="#">page 10</a> description</li> </ul>  |
| 12/29/05 | 2.8 | <ul style="list-style-type: none"> <li>Update to the first paragraph of "<a href="#">IEEE 1149.1 Boundary-Scan (JTAG)</a>," <a href="#">page 7</a>.</li> <li>Added JTAG cautionary note to <a href="#">Page 7</a>.</li> <li>Corrected logic values for Erase/Program (ER/PROG) Status field, IR[4], listed under "<a href="#">XCFxxP Instruction Register (16 bits wide)</a>," <a href="#">page 7</a>.</li> <li>Sections "<a href="#">XCFxxS and XCFxxP PROM as Configuration Slave with CLK Input Pin as Clock Source</a>," <a href="#">page 30</a>, "<a href="#">XCFxxP PROM as Configuration Master with CLK Input Pin as Clock Source</a>," <a href="#">page 32</a> and "<a href="#">XCFxxP PROM as Configuration Master with Internal Oscillator as Clock Source</a>," <a href="#">page 35</a> added to "<a href="#">AC Characteristics Over Operating Conditions</a>," <a href="#">page 30</a>.</li> </ul>   |

|                      |        |   |
|----------------------|--------|---|
| 12/29/05<br>(Cont'd) | 2.8    | <ul style="list-style-type: none"> <li>Notes for <a href="#">Figure 6, page 16</a>, <a href="#">Figure 7, page 17</a>, <a href="#">Figure 8, page 18</a>, <a href="#">Figure 9, page 19</a>, <a href="#">Figure 10, page 20</a>, <a href="#">Figure 11, page 21</a>, <a href="#">Figure 12, page 22</a>, and <a href="#">Figure 13, page 23</a> updated to specify the need for a pull-up resistor if CF is not connected to PROGB.</li> <li>Enhanced description under section "CLKOUT," <a href="#">page 10</a>.</li> <li>Enhanced description on design revision sampling under section "Design Revisioning," <a href="#">page 10</a>.</li> <li>Figure 4 and Figure 5 renamed to <a href="#">Table 7, page 8</a> and <a href="#">Table 8, page 8</a> respectively. All tables, figures, and table and figure references renumber this point forward.</li> <li>Value for "ICCINT," <a href="#">page 29</a> updated from 5mA to 1mA for XCFxxP.</li> <li>Block diagram in <a href="#">Figure 2, page 2</a> updated to show clock source muxing and route clocking to all functional blocks.</li> </ul> |
| 05/09/06             | 2.9    | <ul style="list-style-type: none"> <li>Added Virtex-5 LX support to <a href="#">Table 2, page 3</a>.</li> <li>"VIL" maximum for 2.5V operation in "Recommended Operating Conditions," <a href="#">page 28</a> updated to match LVC MOS25 standard.</li> </ul>   |
| 12/08/06             | 2.10   | <ul style="list-style-type: none"> <li>Added Virtex-5 LXT support to <a href="#">Table 2, page 3</a>.</li> <li>Defined reprogramming operation requirements in "Programming," <a href="#">page 5</a>.</li> <li>Corrected statements regarding the FPGA BUSY pin and corrected various references.</li> </ul>  |
| 02/01/07             | 2.11   | <ul style="list-style-type: none"> <li>Removed Spartan-3L support and added Spartan-3A and Virtex-5 SXT support to <a href="#">Table 2, page 3</a>.</li> <li>Corrected Spartan-3E bitstream sizes in <a href="#">Table 2, page 3</a>.</li> <li>Correct supported voltages for "VCCJ" in <a href="#">Table 13, page 38</a>, "VCCO" and "VCCJ" in <a href="#">Table 14, page 40</a>.</li> </ul>   |
| 03/30/07             | 2.11.1 | Added Spartan-3A DSP support to <a href="#">Table 2, page 3</a> .   |
| 01/28/08             | 2.12   | <ul style="list-style-type: none"> <li>Added support for XC5VLX155, XC5VLX20T, and XC5VLX155T.</li> <li>Updated JTAG TAP timing specifications in <a href="#">Table 10, page 9</a> to reflect improved performance.</li> <li>Tied FPGA CS_B and FPGA RDWR_B to GND in the FPGA SelectMAP schematics (<a href="#">Figure 9, page 20</a>, <a href="#">Figure 10, page 21</a>, <a href="#">Figure 11, page 22</a>, and <a href="#">Figure 13, page 24</a>) to ensure valid logic Low.</li> <li>Hardwired external oscillator to FPGA CCLK in the FPGA slave mode schematics (<a href="#">Figure 7, page 18</a>, <a href="#">Figure 10, page 21</a>, <a href="#">Figure 12, page 23</a>, and <a href="#">Figure 13, page 24</a>).</li> <li>Added marking templates (<a href="#">Figure 22, page 45</a>, <a href="#">Figure 23</a> and <a href="#">Figure 24</a>), and corrected marks for 48-pin TFBGA packages in "Marking Information," <a href="#">page 44</a>.</li> <li>Other edits and updates made.</li> <li>Updated document template.</li> <li>Updated URLs.</li> </ul>                             |
| 03/31/08             | 2.13   | <ul style="list-style-type: none"> <li>Added Virtex-5 FX FPGA support to <a href="#">Table 2, page 3</a>.</li> <li>Corrected markings for all packaging (<a href="#">Figure 22, page 45</a>, <a href="#">Figure 23</a>, and <a href="#">Figure 24</a>).</li> <li>Added note regarding variances in packaging and marking to <a href="#">Page 45</a>.</li> </ul>   |
| 04/03/08             | 2.13.1 | <ul style="list-style-type: none"> <li>Corrected typo.</li> <li>Updated trademark notations.</li> </ul>   |
| 05/14/08             | 2.14   | Added support for XC5VSX240T and Platform Flash XL to <a href="#">Table 2, page 3</a> .   |
| 07/07/08             | 2.15   | Updated "Write Protection," <a href="#">page 6</a> .  |

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