



### FEATURES

- RF frequency range of 700 MHz to 2800 MHz
- LO frequency range of 450MHz to 2760MHz
- IF frequency range of 40 MHz to 450 MHz
- Power conversion gain of 7dB
- SSB noise figure of 11 dB
- Input IP3 of 24dBm over the full RF bandwidth
- Input P1dB of 11 dBm over the full RF bandwidth
- Typical LO drive of 0 dBm
- Single-ended, 50Ω RF Port
- Single-ended or Balanced LO Input Port
- Single-supply operation: 3.6 to 5.0V
- Serial port interface control on all functions
- Exposed paddle 6 x 6 mm, 40 Lead LFCSP

### APPLICATIONS

- Multi-band/ multi-standard cellular base station diversity receivers
- Wideband radio link diversity downconverters
- Multi-mode cellular extenders and picocells

### GENERAL DESCRIPTION

The ADL5812 uses revolutionary new broadband square wave limiting LO amplifiers to achieve an unprecedented RF bandwidth of 700 to 2800MHz. Unlike conventional narrowband sine wave LO amplifier solutions, this permits the LO to be applied either above or below the RF input over an extremely wide bandwidth. Since energy storage elements are not utilized, the DC current consumption also decreases with decreasing LO frequency.

The ADL5812 utilizes highly linear doubly balanced passive mixer cores along with integrated RF and LO balancing circuits to allow for single-ended operation. The ADL5812 incorporates programmable RF baluns allowing for optimal performance over a 700 to 2800 MHz RF input frequency. The balanced passive mixer arrangement provides outstanding LO to RF and LO to IF leakages, excellent RF to IF isolation, and excellent intermodulation performance over the full RF bandwidth.

### REV. PrA

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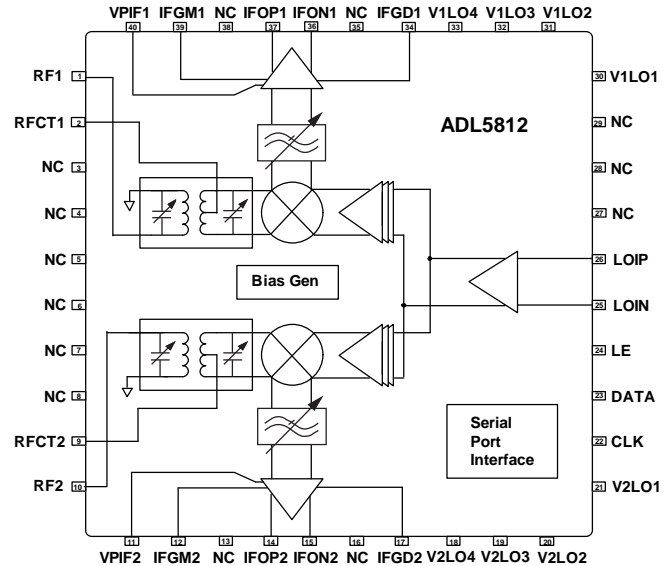


Figure 1. Functional Block Diagram

The balanced mixer cores also provide extremely high input linearity allowing the device to be used in demanding wideband applications where in-band blocking signals may otherwise result in the degradation of dynamic range. Blocker Noise Figure performance is comparable to narrowband passive mixer designs. High linearity IF buffer amplifiers follow the passive mixer cores, yielding typical power conversion gains of 7dB, and can be utilized with a wide range of output impedances. For low voltage applications, the ADL5812 is capable of operation at voltages down to 3.6V with substantially reduced current. Two logic pins are provided to individually power down (<100uA) the 2 channels as desired.

All features of the ADL5812 are controlled via a 3-wire serial port interface resulting in optimum performance and minimum external components.

The ADL5812 is fabricated using a BiCMOS high performance IC process. The device will be available in a 6mm x 6mm 40-lead LFCSP package and operates over a -40°C to +85°C temperature range. An evaluation board is also available.

## ADL5812—Specifications

Table 1.  $V_S = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $f_{RF} = 1900\text{ MHz}$ ,  $f_{LO} = 1697\text{ MHz}$ , LO power = 0 dBm,  $Z_o = 50\Omega$ , unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20dB broadband via serial port		10		dB
Input Impedance			50		$\Omega$
RF Frequency Range		700		2800	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, $f = 200\text{ MHz}$		200		$\Omega$
IF Frequency Range		40		450	MHz
DC Bias Voltage <sup>1</sup>	Externally generated		$V_S$		V
LO INTERFACE					
LO Power		-5	0	+10	dBm
Return Loss			14		dB
Input Impedance			50		$\Omega$
LO Frequency Range	Low or High Side LO	450		2760	MHz
DYNAMIC PERFORMANCE					
Power Conversion Gain	Including 4:1 IF port transformer and PCB loss		7.6		dB
Voltage Conversion Gain	$Z_{SOURCE} = 50\Omega$ , Differential $Z_{LOAD} = 200\Omega$ Differential		13.3		dB
SSB Noise Figure			11		dB
SSB Noise Figure Under-Blocking	5dBm Blocker present +/-10MHz from wanted RF input, LO source filtered		22		dB
Input Third Order Intercept	$f_{RF1} = 1900\text{ MHz}$ , $f_{RF2} = 1901\text{ MHz}$ , $f_{LO} = 1697\text{ MHz}$ , each RF tone at -10 dBm		25.5		dBm
Input Second Order Intercept	$f_{RF1} = 1900\text{ MHz}$ , $f_{RF2} = 1950\text{ MHz}$ , $f_{LO} = 1697\text{ MHz}$ , each RF tone at -10 dBm		57		dBm
Input 1 dB Compression Point			11		dBm
LO to IF Output Leakage	Unfiltered IF Output		-36		dBm
LO to RF Input Leakage			-45		dBm
RF to IF Output Isolation			30		dB
IF/2 Spurious	-10 dBm Input Power		-66		dBc
IF/3 Spurious	-10dBm Input Power		-69		dBc
POWER INTERFACE					
Supply Voltage, $V_S$		3.6	5	5.5	V
Quiescent Current	Resistor Programmable IF Current		380		mA

<sup>1</sup> Supply voltage must be applied from external circuit through choke inductors

**TIMING CHARACTERISTICS**

Table 2. Serial Interface Timing,  $V_{CC} = 5\text{ V} \pm 5\%$

Parameter	Limit	Unit	Test Conditions/Comments
$t_1$	20	ns minimum	LE setup time
$t_2$	10	ns minimum	DATA to CLK setup time
$t_3$	10	ns minimum	DATA to CLK hold time
$t_4$	25	ns minimum	CLK high duration
$t_5$	25	ns minimum	CLK low duration
$t_6$	10	ns minimum	CLK to LE setup time
$t_7$	20	ns minimum	LE pulse width

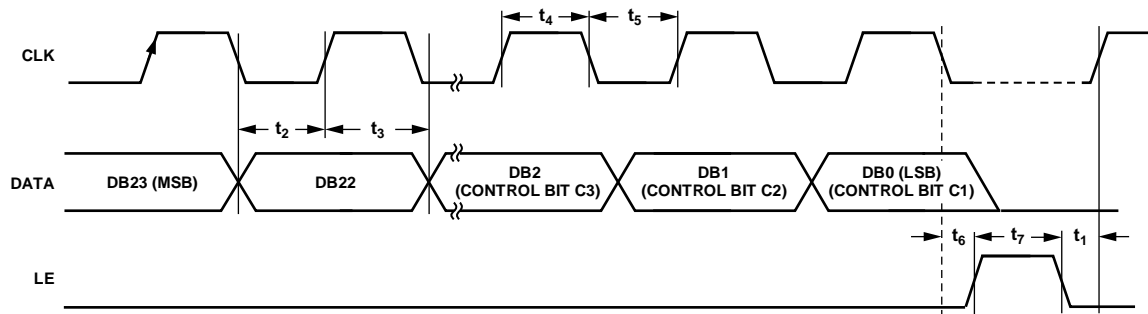


Figure 2. Timing Diagram

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## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, $V_{POS}$	5.5 V
CLK, DATA, LE	5.5 V
IF Output Bias	6.0 V
RF Input Power	20 dBm
LO Input Power	13 dBm
Internal Power Dissipation	TBD
$\theta_{JA}$ (Exposed Paddle Soldered Down)	TBD
$\theta_{JC}$ (At Exposed Paddle)	TBD
Maximum Junction Temperature	TBD
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

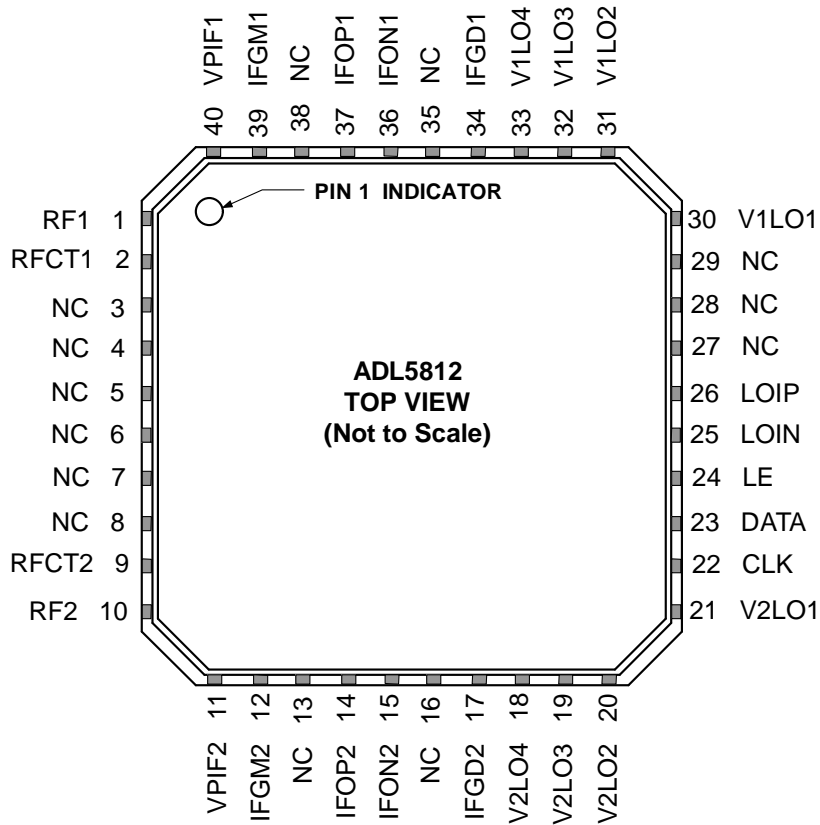
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



**NOTES**

- 1. NC = NO CONNECT.
- 2. EXPOSED PAD MUST BE CONNECTED TO GROUND.

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
3,4,5,6,7,8,13,16, 27,28,29,35,36,38	NC	No Connect. Can be grounded.
1,10	RF1,RF2	RF Input. Must be ac-coupled.
3,8	RFCT1,2	RF Balun Center Tap (AC Ground).
18,19,20,21, 30,31,32,33	V1LO1,V1LO2,V1LO3,V1LO4, V2LO1,V2LO2,V2LO3,V2LO4	Positive Supply Voltages for LO Amplifiers.
22,23,24	CLK,DATA,LE	Serial Port Interface Control.
25	LOIN	Ground Return for LO Input, must be ac coupled.
26	LOIP	LO Input. Must be ac-coupled.
17,34	IFGD1, IFGD2	Supply Return for IF Amplifier. Must be grounded.
14,15,36,37	IFOP1,IFOP2, IFON1,IFON2	Differential Open-Collector IF Outputs. Should be pulled-up to VCC via external inductors.
12,39	IFGM1, FIGM2	IF amplifier bias control.
11,40	VFIP1, VFIP2	Supply Voltage for IF amplifier.
Paddle	EPAD	Exposed pad must be connected to ground.

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , as measured using typical circuit schematic with low-side LO unless otherwise noted.

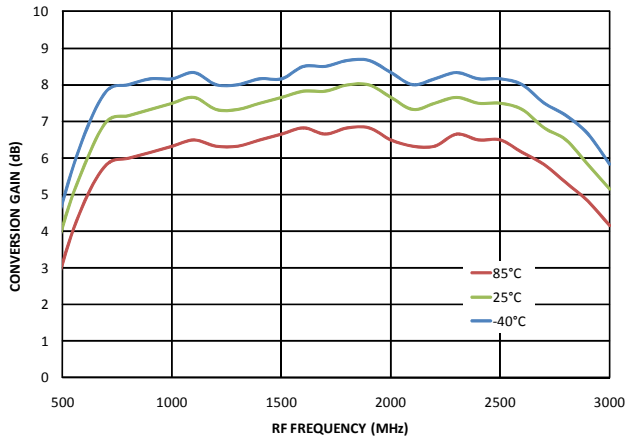


Figure 4. Conversion Gain versus RF Frequency

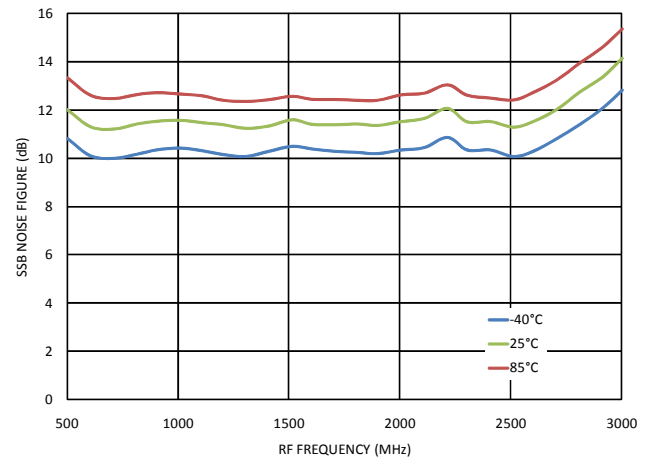


Figure 7. Single-Sideband NF versus RF Frequency

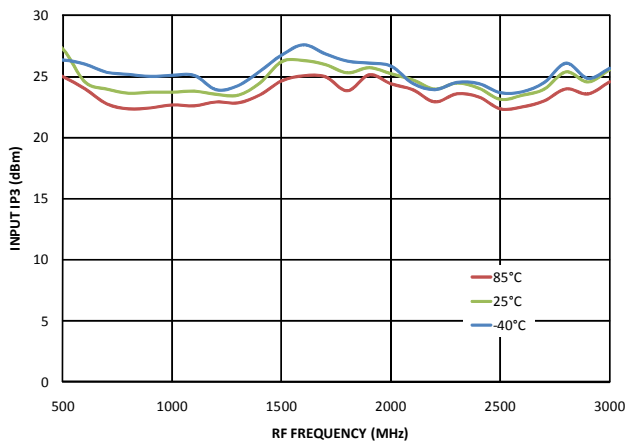


Figure 5. IIP3 versus RF Frequency

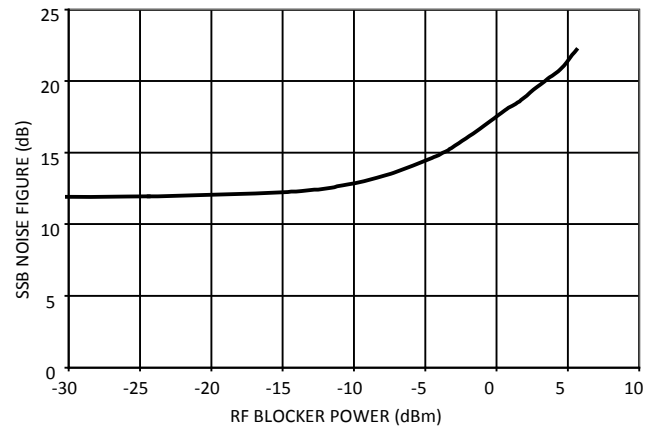


Figure 8. Single-Sideband NF versus Blocker Level

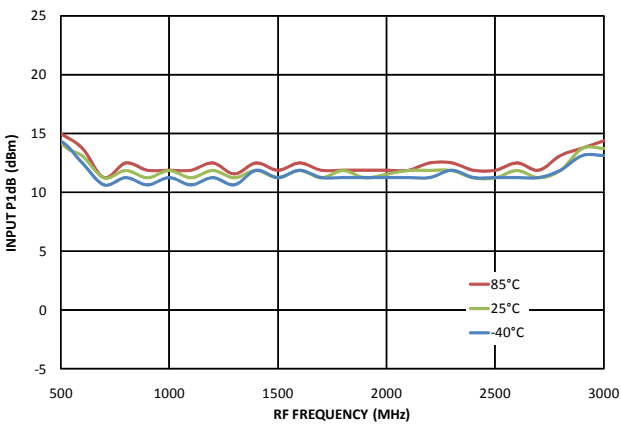


Figure 6. IP1dB versus RF Frequency

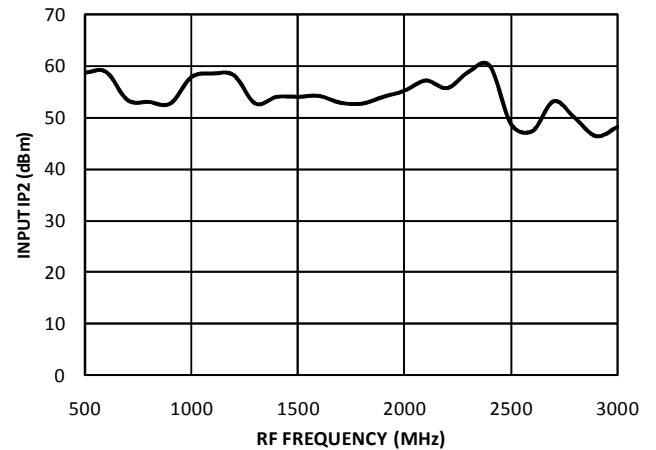


Figure 9. IIP2 versus RF Frequency

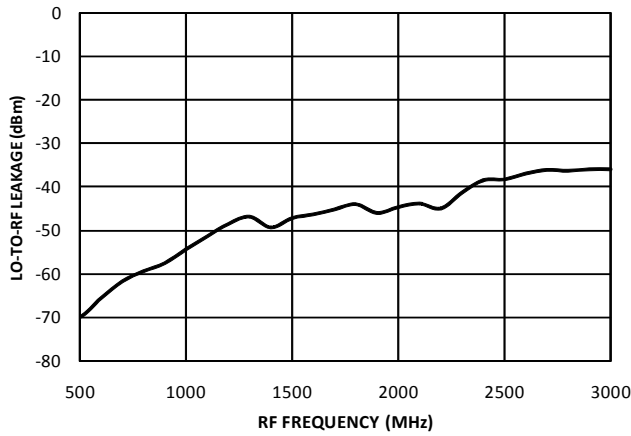


Figure 10. LO to RF Leakage versus RF Frequency

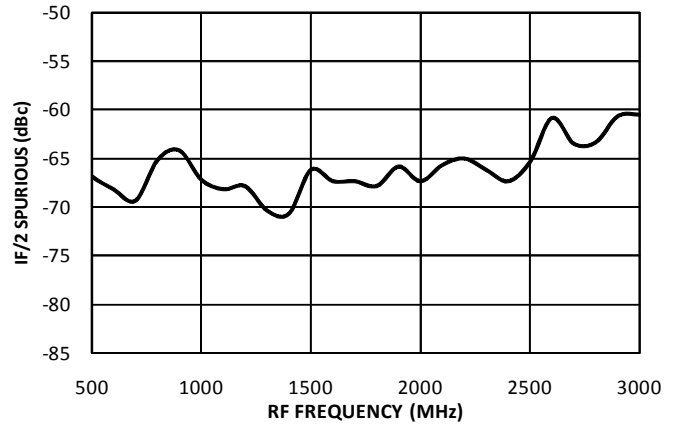


Figure 13. IF/2 Spurious versus RF Frequency

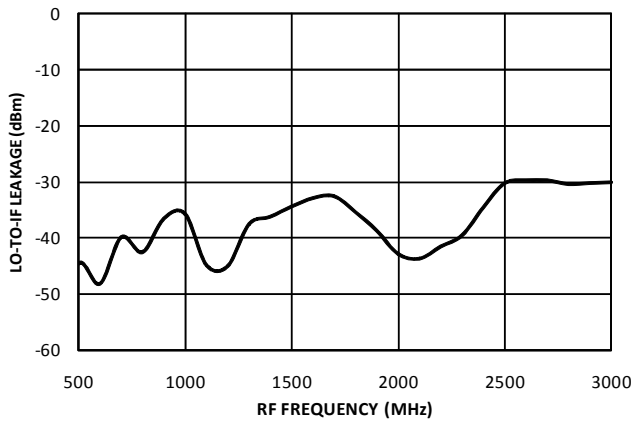


Figure 11. LO to IF Leakage versus RF Frequency

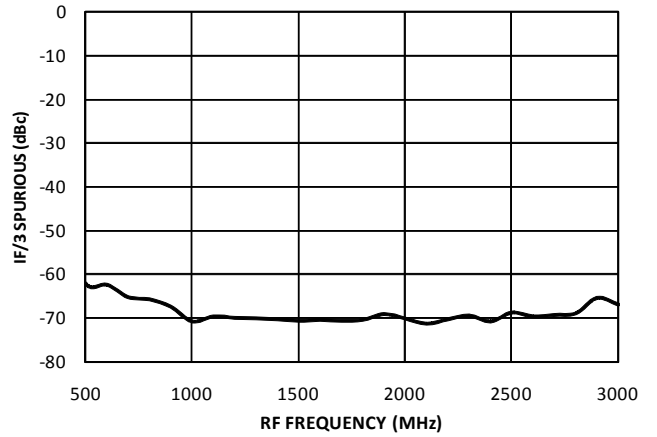


Figure 14. IF/3 Spurious versus RF Frequency

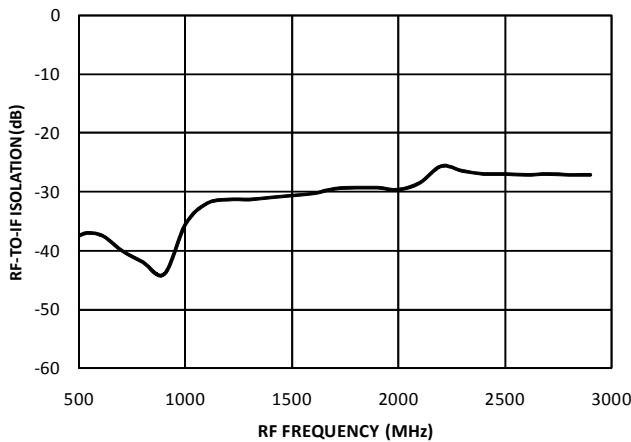


Figure 12. RF to IF Isolation versus RF Frequency

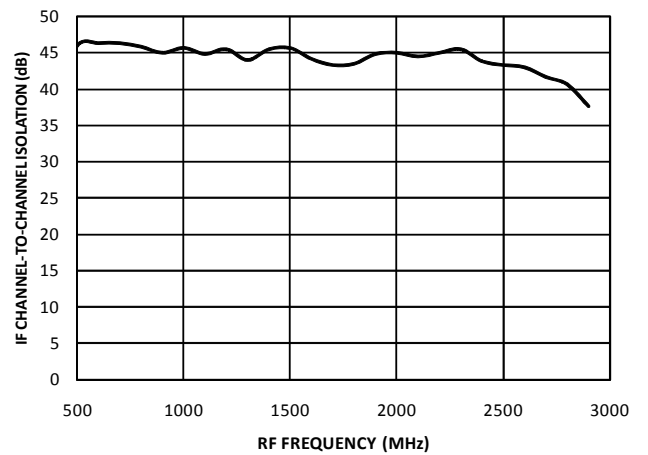


Figure 15. Channel-to-Channel Isolation versus RF Frequency

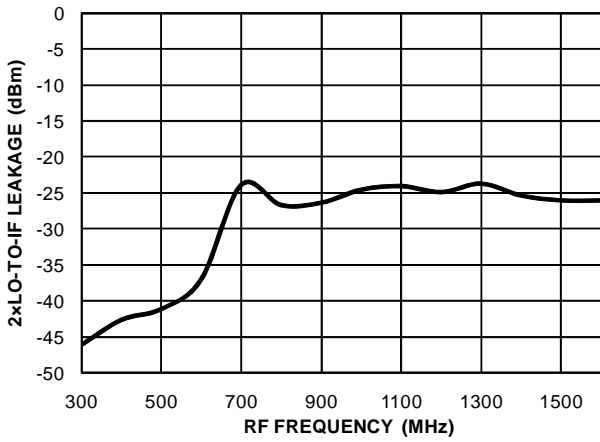


Figure 16. 2xLO to IF Leakage versus RF Frequency

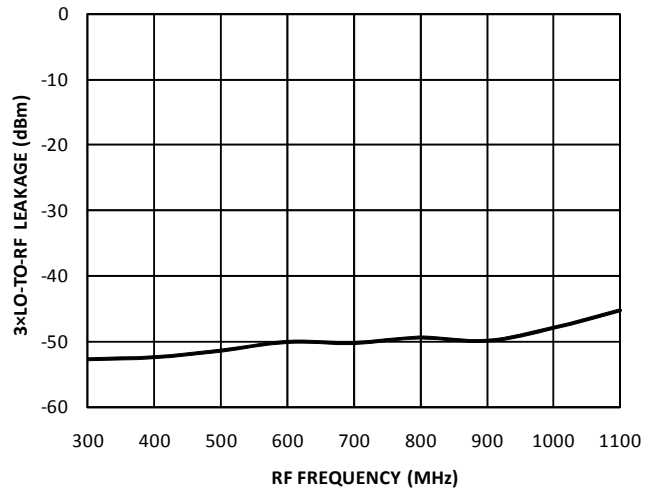


Figure 19. 3xLO to RF Leakage versus RF Frequency

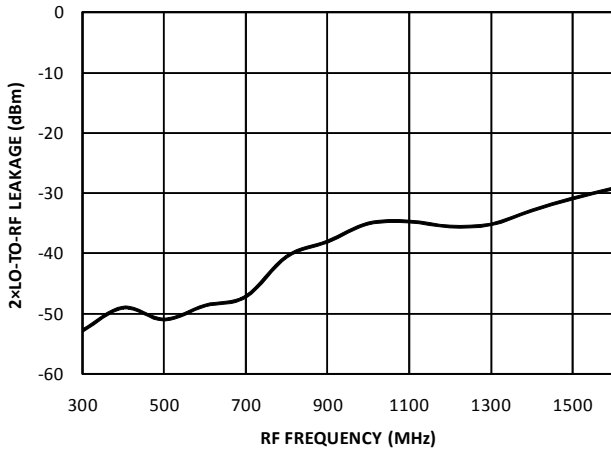


Figure 17. 2xLO to RF Leakage versus RF Frequency

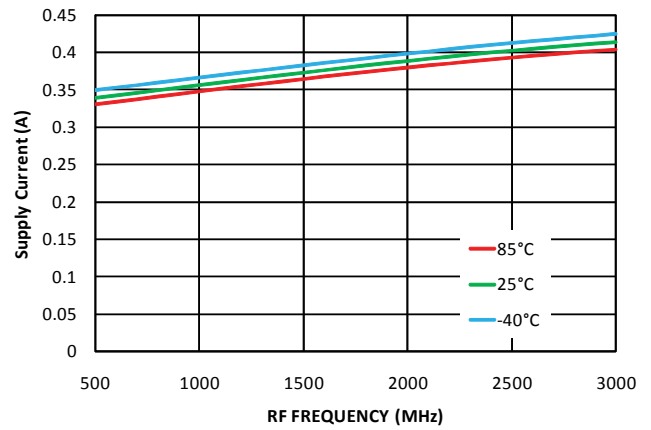


Figure 20. Supply Current versus RF Frequency

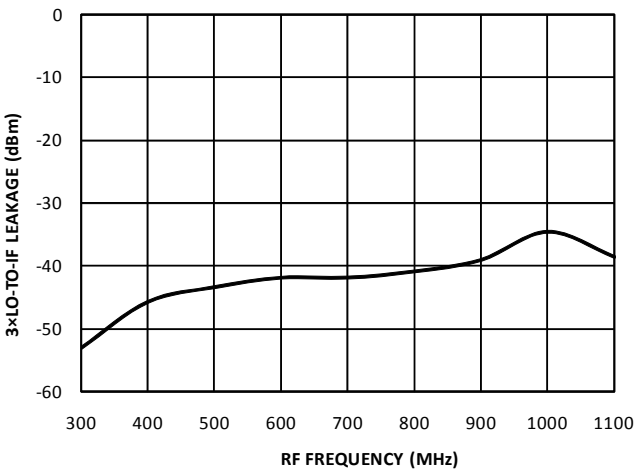


Figure 18. 3xLO to IF Leakage versus RF Frequency

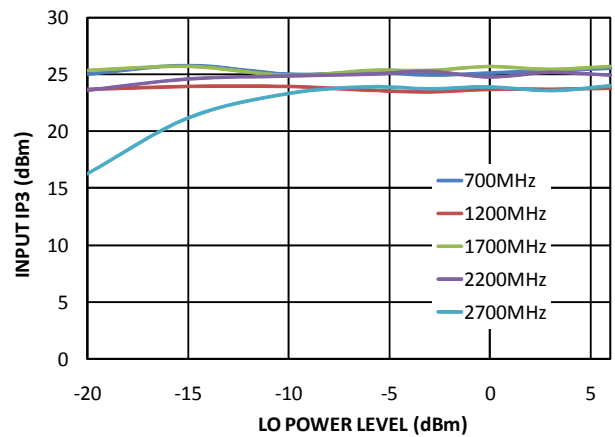


Figure 21. Input IP3 versus LO Power Level



### SPUR TABLES

All spur tables are  $(N \times f_{RF}) - (M \times f_{LO})$  and were measured using the standard evaluation board. Mixer spurious products are measured in dBc from the IF output power level. Data was measured only for frequencies less than 6 GHz. Typical noise floor of the measurement system = -100 dBm. N.M. indicates that the spurs were below the noise floor of the measurement system.

### 5 V PERFORMANCE

$V_S = 5\text{ V}$ ,  $I_S = 350\text{ mA}$ ,  $T_A = 25^\circ\text{C}$ ,  $f_{RF} = 1910\text{ MHz}$ ,  $f_{LO} = 1700\text{ MHz}$ , RF power = -10 dBm, LO power = 0 dBm, optimum settings, and  $Z_O = 50\ \Omega$ , unless otherwise noted.

		M														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
N	0		-17.4	-12.2	-46.6	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	1	-24.7	8.8	-40.1	-46.9	-69.8	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	2	-62.2	-61.6	-69.1	-61.1	-71.9	-88.7	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	3	-101.7	-77.7	-89.4	-68.9	-87.3	-100.3	-101.4	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	4	N.M.	-101.7	-101.2	-103.2	-95.9	-107.4	-103.1	-101.2	-102.2	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.
	5	N.M.	N.M.	N.M.	-101.5	-102.9	-103.3	-104.1	-102.4	-102.4	-100.5	N.M.	N.M.	N.M.	N.M.	N.M.
	6	N.M.	N.M.	N.M.	N.M.	-99.9	-103.5	-104.7	-107.3	-103.8	-97.4	-99.5	N.M.	N.M.	N.M.	N.M.
	7	N.M.	N.M.	N.M.	N.M.	N.M.	-100.5	-100.2	-103.2	-105.2	-101.9	-101.2	-99.0	N.M.	N.M.	N.M.
	8	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	-101.0	-101.2	-105.0	-108.2	-104.6	-100.4	-98.7	N.M.	N.M.
	9	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	-100.7	-100.8	-104.4	-105.3	-105.6	-101.6	-101.1	N.M.
	10	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	-99.3	-99.6	-105.2	-105.3	-103.9	-102.8	-100.3
	11	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	-99.4	-101.7	-102.5	-105.2	-105.3	-104.0
	12	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	-101.1	-102.0	-105.9	-105.9	-106.5
	13	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	-100.5	-102.2	-103.2
	14	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	-98.8	-102.9
	15	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	N.M.	-99.3

## REGISTER STRUCTURE

Figure 22 illustrates the register map of ADL5812. The ADL5812 uses only register 5. As such the Control Bits should be set to 5 in all cases. The Main ENB and Div ENB bits, DB7 and DB6 respectively, when set to 0 will enable the part. By setting one of these bits to 1 that channel will be powered down. Either channel can be powered down independently of the other. The CAP DAC RFB IN and Out bits are used to tune the RF Balun. In most cases they will be tuned together with the higher settings, 15, tuning for low frequencies and lower settings, 0, tuning for high frequencies. There are times where it becomes advantageous to tune the input and output of the RF

balun separately and that ability is provided for here. The LPF bits control the Low Pass Filter settings at the IF output. The ability to tune the low pass filter allows some tradeoff between Gain, Noise Figure and Input IP3 with higher settings, 7, providing higher Input IP3 at the cost of some Gain and Noise Figure while lower settings, 0, provide higher Gain and lower NF at the cost of lower Input IP3. The VGS bits control the VGS settings of the mixer core and will allow further tuning of the device.

Figure 23 illustrates the optimum settings characterized for each frequency band.

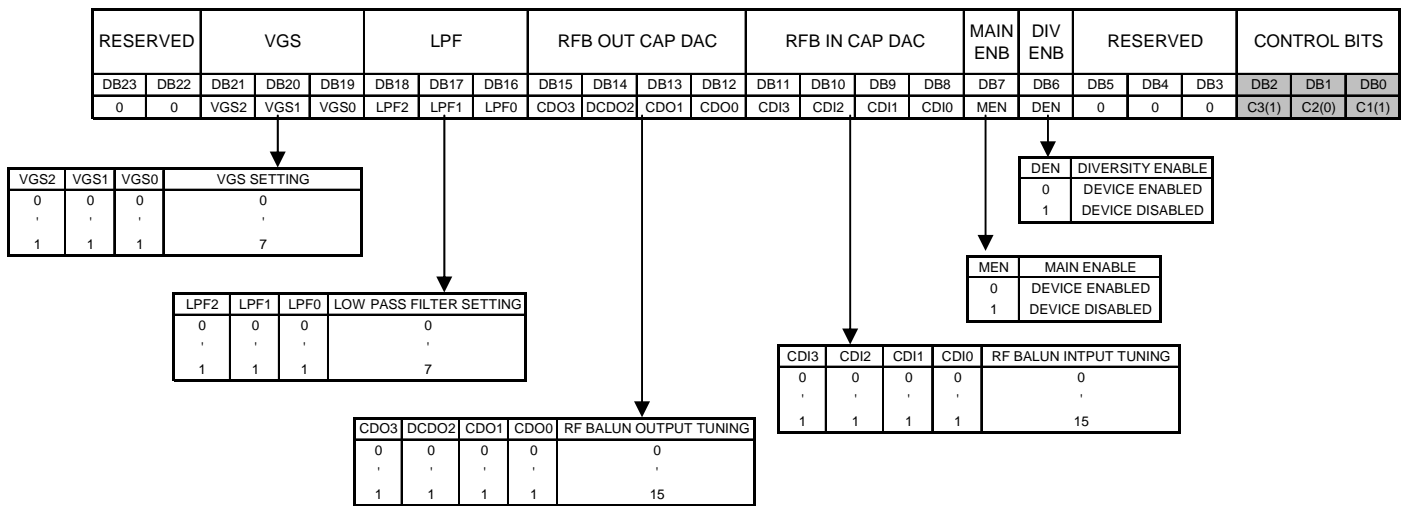


Figure 22. ADL5812 Register Maps

RF (MHz)	LO (MHz)	VGS			LPF			RFB OUT CAP DAC				RFB IN CAP DAC			
		DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8
		VGS2	VGS1	VGS0	LPF2	LPF1	LPF0	CDO3	DCDO2	CDO1	CDO0	CDI3	CDI2	CDI1	CDI0
300	97	0	0	0	0	1	0	1	1	1	1	1	1	1	1
400	197	0	0	0	0	1	0	1	1	1	1	1	1	1	1
500	297	0	0	0	0	1	0	1	1	1	1	1	1	1	1
600	397	0	0	0	0	1	0	1	1	0	0	1	1	0	0
700	497	0	0	0	0	1	0	1	1	0	0	1	1	0	0
800	597	0	0	0	0	1	0	1	0	0	0	1	0	0	0
900	697	0	0	0	0	1	0	1	0	0	0	1	0	0	0
1000	797	0	0	0	0	1	0	1	0	0	0	1	0	0	0
1100	897	0	0	0	0	1	0	1	0	0	0	1	0	0	0
1200	997	0	0	0	1	0	0	1	0	0	0	1	0	0	0
1300	1097	0	0	0	1	0	0	0	1	1	0	0	1	1	0
1400	1197	0	0	0	1	0	0	0	1	1	0	0	1	1	0
1500	1297	0	0	0	1	0	0	0	1	1	0	0	1	1	0
1600	1397	0	0	0	1	0	0	0	1	1	0	0	1	1	0
1700	1497	0	0	0	1	0	0	0	1	1	0	0	1	1	0
1800	1597	0	0	0	1	0	0	0	1	1	0	0	1	1	0
1900	1697	0	0	0	1	0	0	0	1	1	0	0	1	1	0
2000	1797	0	0	0	1	0	0	0	1	1	0	0	1	1	0
2100	1897	0	0	0	1	0	0	0	1	1	0	0	1	1	0
2200	1997	0	0	0	1	0	0	0	1	1	0	0	1	1	0
2300	2097	0	0	0	1	0	0	0	0	1	0	0	1	0	0
2400	2197	0	0	0	1	0	0	0	0	0	0	0	1	0	0
2500	2297	0	0	0	0	1	0	0	0	0	0	0	1	0	0
2600	2397	0	0	0	0	1	0	0	0	0	0	0	1	0	0
2700	2497	0	0	0	0	1	0	0	0	0	0	0	1	0	0
2800	2597	0	0	0	0	1	0	0	0	0	0	0	1	0	0
2900	2697	0	0	0	0	1	0	0	0	0	0	0	1	0	0
3000	2797	0	0	0	0	1	0	0	0	0	0	0	1	0	0

Figure 23. ADL5812 Optimum Settings

### EVALUATION BOARD

An evaluation board is available for the ADL5812. The standard evaluation board schematic is presented in Figure 24. The evaluation board is fabricated on a multilayer Rogers board. Table 4 details the various configuration options of the evaluation board.

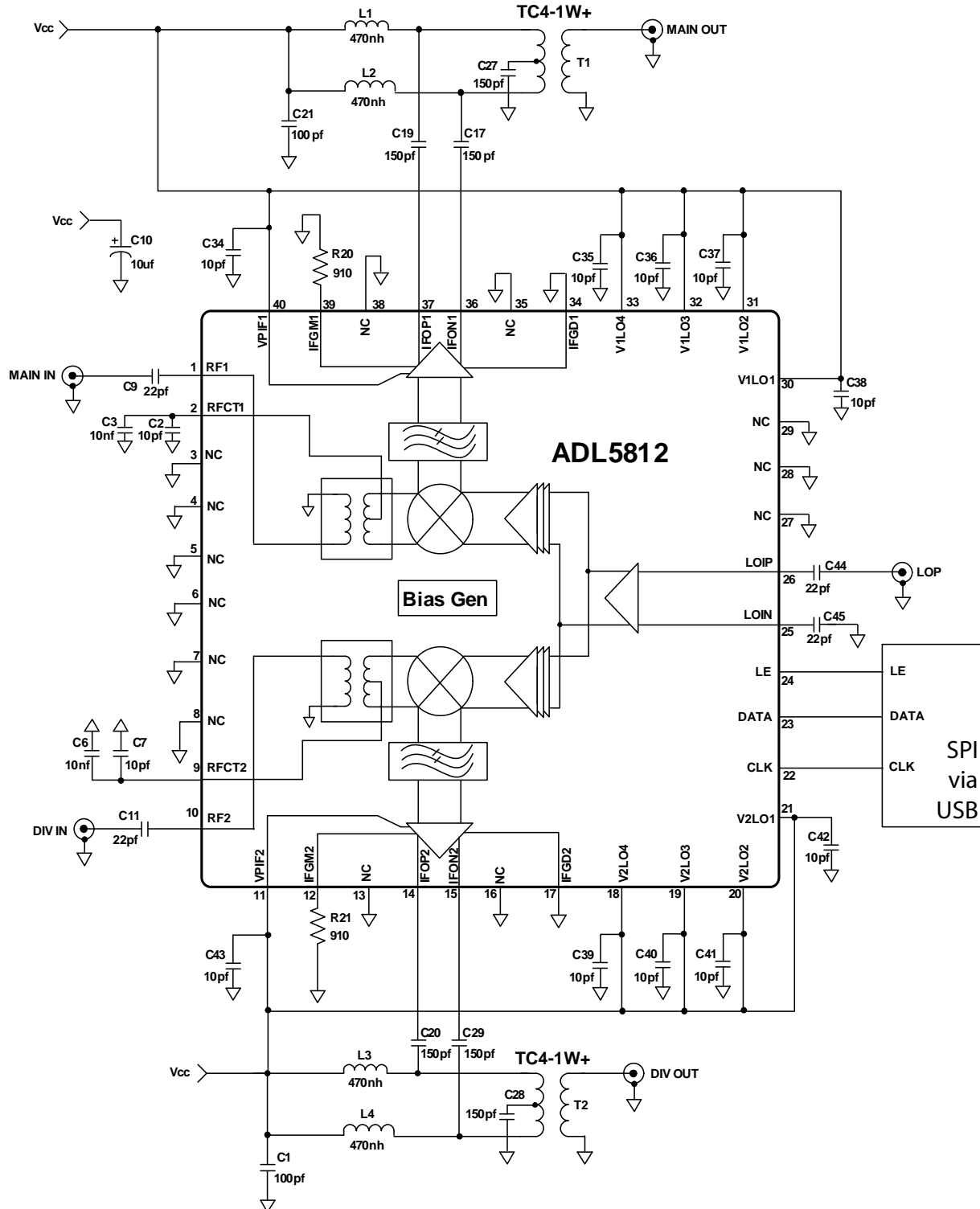


Figure 24. Evaluation Board Schematic.

Table 4. Eval Board Configuration

Components	Function	Default Conditions
C1, C10, C21, C34-C43	Power Supply Decoupling. Nominal supply decoupling consists a 10 $\mu$ F capacitor to ground in parallel with 10pF capacitors to ground positioned as close to the device as possible.	C10 = 10 $\mu$ F (size 0603) C34-C43 = 10 pF (size 0402) C1, C8,C12,C21 = 100 pF (size 0402)
C2,C3,C6,C7,C9, C11	RF Input Interface. The input channels are ac-coupled through C9, C11. C2,C3,C6,C7 provide bypassing for the center taps of the RF input baluns.	C9,C11 = 22 pF (size 0402) C3,C6 = 0.01 $\mu$ F (size 0402) C2, C7 = 10 pF (size 0402)
T1, T2,C27, C28, C20, C29,L1-L4	IF Output Interface. The open collector IF output interfaces are biased through pull-up choke inductors L1-L4. T1, T2 are 4:1 impedance transformer used to provide a single ended IF output interface, with C27, C28 providing center-tap bypassing.	C27, C28 = 150 pF (size 0402) T1 = TC4-1W+ (MiniCircuits) L1-L4 = 470 nH (size 1008)
C25, C26,C44, C45	LO Interface. C44 and C45 provide ac-coupling for the LO1_IN and LO2_IN local oscillator inputs.	C44, C45 = 22pF (size 0402)
R20,R21	Bias Control. R20,21 sets the bias point for the internal IF amplifiers.	R20,R21 = 910 $\Omega$ (size 0402)

