700 MHz to 2800 MHz, Balanced Mixer, LO Buffer, IF Amplifier, and RF Balun

Preliminary Technical Data

ADL5811

FEATURES

RF frequency range of 700 MHz to 2800 MHz
LO frequency range of 450 MHz to 2760 MHz
IF freqeuncy range of 40 MHz to 450 MHz
Power conversion gain of 7.5dB
SSB noise figure of 11dB
Input IP3 of 24dBm over the full RF bandwidth
Input P1dB of 12 dBm over the full RF bandwidth
Typical LO drive of 0 dBm
Single-ended, 50Ω RF port
Single-ended or balanced LO input port
Single-supply operation: 3.6 V to 5 V
Exposed paddle 5 x 5 mm, 32-lead LFCSP

APPLICATIONS

Multi-band/ multi-standard cellular base station receivers
Wideband transmit observation receivers
Wideband radio link downconverters
Multi-mode cellular extenders and picocells

GENERAL DESCRIPTION

The ADL5811 uses a revolutionary new broadband square wave limiting LO amplifier to achieve an unprecedented RF bandwidth of 700 to 2800MHz. Unlike conventional narrowband sinewave LO amplifier solutions, this permits the LO to be applied either above or below the RF input over an extremely wide bandwidth. Since energy storage elements are not utilized, the DC current consumption also decreases with decreasing LO frequency.

The ADL5811 utilizes a highly linear doubly balanced passive mixer core along with integrated RF and LO balancing circuitry to allow for single-ended operation. The ADL5811 incorporates a programmable RF balun allowing for optimal performance over a 700 to 2800 MHz RF input frequency. The balanced passive mixer arrangement provides outstanding LO to RF and LO to IF leakages, excellent RF to IF isolation, and excellent intermodulation performance over the full RF bandwidth. The

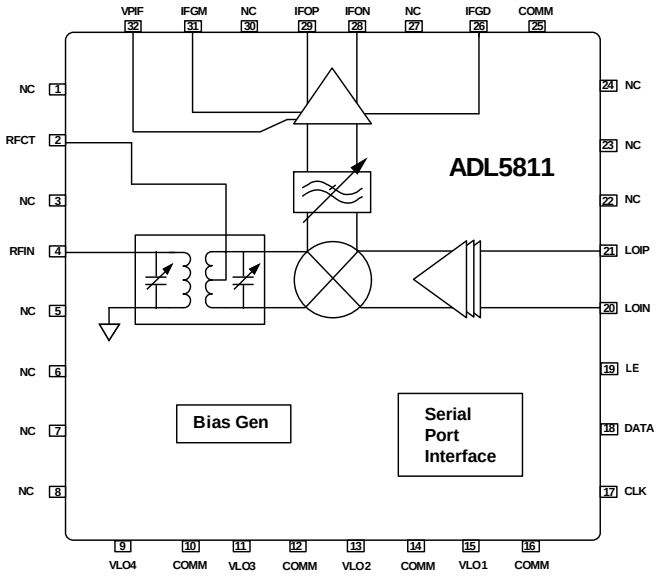

Figure 1. Functional Block Diagram

balanced mixer core also provides extremely high input linearity allowing the device to be used in demanding wideband applications where in-band blocking signals may otherwise result in the degradation of dynamic range. Blocker Noise Figure performance is comparable to narrowband passive mixer designs. A high linearity IF buffer amp follows the passive mixer core, to yield a typical power conversion gain of 7.5dB, and can be utilized with a wide range of output impedances. For low voltage applications, the ADL5811 is capable of operation at voltages down to 3.6V with substantially reduced current. A logic pin is provided to power down (<100uA) the circuit when desired.

The ADL5811 is fabricated using a BiCMOS high performance IC process. The device will be available in a 5mm x 5mm 32-lead LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

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ADL5811—Specifications

Table 1. V_S = 5 V, T_A = 25°C, f_{RF} = 1900 MHz, f_{LO} = 1697 MHz, LO power = 0 dBm, Zo = 50Ω, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20dB over a limited bandwidth		14		dB
Input Impedance			50		Ω
RF Frequency Range		700		2800	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		200		Ω
IF Frequency Range		40		450	MHz
DC Bias Voltage[1]	Externally generated		V_S		V
LO INTERFACE					
LO Power		-5	0	+10	dBm
Return Loss			14		dB
Input Impedance			50		Ω
LO Frequency Range	Low or High Side LO	450		2760	MHz
DYNAMIC PERFORMANCE					
Power Conversion Gain	Including 4:1 IF port transformer and PCB loss		7.6		dB
Voltage Conversion Gain	Z_{SOURCE} = 50Ω, Differential Z_{LOAD} = 200Ω Differential		13.9		dB
SSB Noise Figure			10.0		dB
SSB Noise Figure Under-Blocking	5dBm Blocker present +/-10MHz from wanted RF input, LO source filtered		22		dB
Input Third Order Intercept	f_{RF1} = 1900 MHz, f_{RF2} = 1901 MHz, f_{LO} = 1697 MHz, each RF tone at -10 dBm		25		dBm
Input Second Order Intercept	f_{RF1} = 1900 MHz, f_{RF2} = 1950 MHz, f_{LO} = 1697 MHz, each RF tone at -10 dBm		55		dBm
Input 1 dB Compression Point			11		dBm
LO to IF Output Leakage	Unfiltered IF Output		-40		dBm
LO to RF Input Leakage			-48		dBm
RF to IF Output Isolation			28		dB
IF/2 Spurious	-10 dBm Input Power		-65		dBc
IF/3 Spurious	-10dBm Input Power		-68		dBc
POWER INTERFACE					
Supply Voltage, Vs		3.3	5	5.5	V
Quiescent Current	Resistor Programmable IF Current		190		mA

[1] Supply voltage must be applied from external circuit through choke inductors

TIMING CHARACTERISTICS

Table 2. Serial Interface Timing, V_{CC} = 5 V ± 5%

Parameter	Limit	Unit	Test Conditions/Comments
t_1	20	ns minimum	LE setup time
t_2	10	ns minimum	DATA to CLK setup time
t_3	10	ns minimum	DATA to CLK hold time
t_4	25	ns minimum	CLK high duration
t_5	25	ns minimum	CLK low duration
t_6	10	ns minimum	CLK to LE setup time
t_7	20	ns minimum	LE pulse width

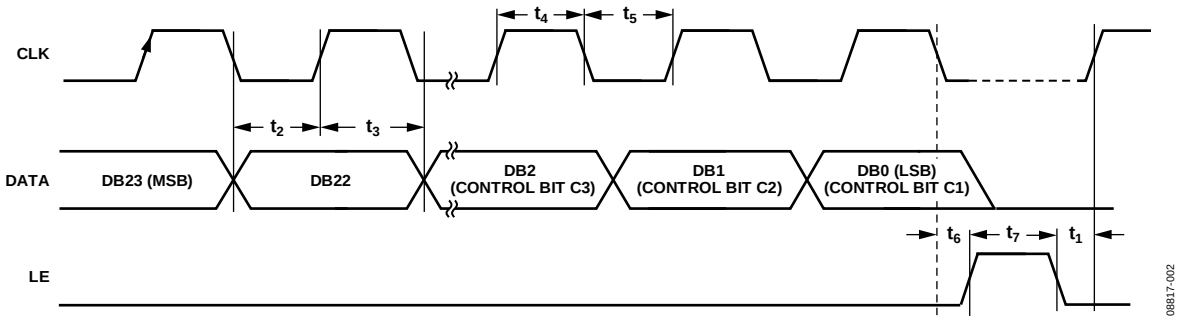

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
CLK, DATA, LE	5.5 V
IF Output Bias	6.0 V
RF Input Power	20 dBm
LO Input Power	13 dBm
Internal Power Dissipation	TBD
θ_{JA} (Exposed Paddle Soldered Down)	TBD
θ_{JC} (At Exposed Paddle)	TBD
Maximum Junction Temperature	TBD
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

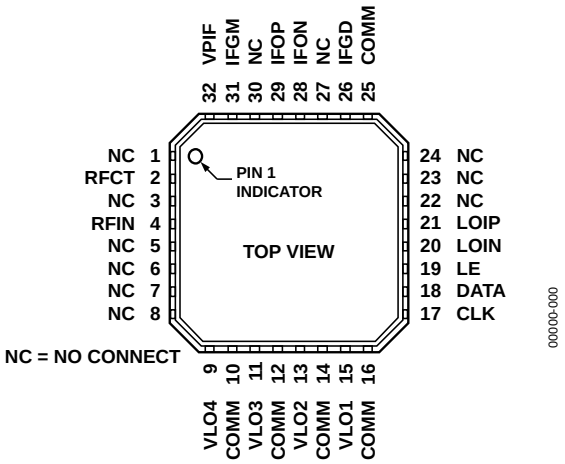

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1,3,5,6,7,8,22,23,24,27,30	NC	No Connect. Can be grounded.
2	RFCT	RF Balun Center Tap (AC Ground).
4	RFIN	RF Input. Must be grounded.
9,11,13,15	VLO4,VLO3,VLO2, VLO1	Positive Supply Voltages for LO Amplifier.
10,12,14,16	COMM	Supply Return for LO Amplifier. Must be grounded.
17,18,19	CLK,DATA,LE	Serial Port Interface Control.
20	LOIN	Ground Return for LO Input.
21	LOIP	LO Input. Must be ac-coupled.
25	COMM	Ground.
26	IFGD	Supply Return for IF Amplifier. Must be grounded.
28,29	IFOP, IFON	IF Differential Open-Collector Outputs. Should be pulled-up to VCC using external inductors.
31	IFGM	IF Amplifier Bias Control.
32	VFIP	Supply Voltage for IF Amplifier.
Paddle	EPAD	Exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, as measured using typical circuit schematic with low-side LO unless otherwise noted.

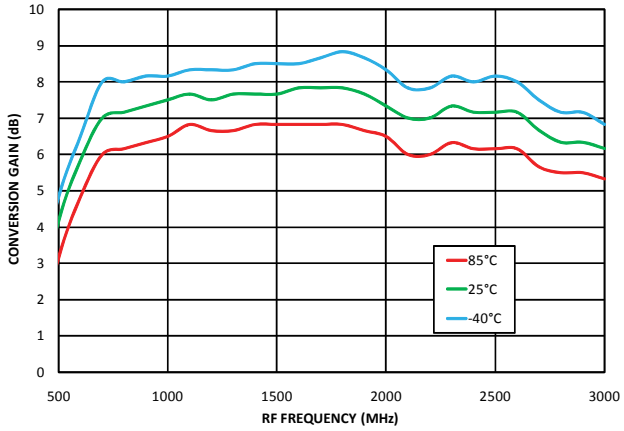

Figure 4. Conversion Gain versus RF Frequency

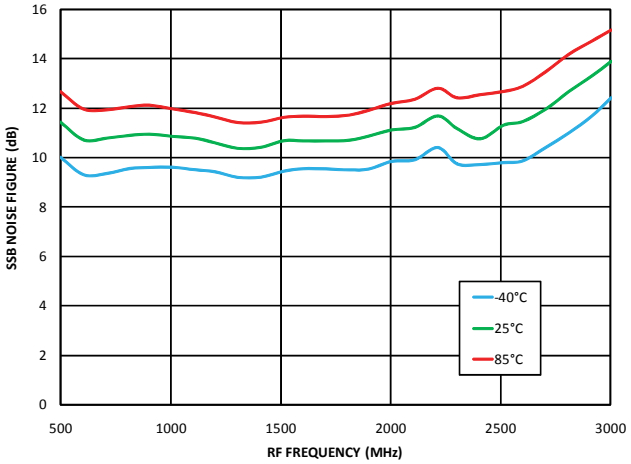

Figure 7. Single-Sideband NF versus RF Frequency

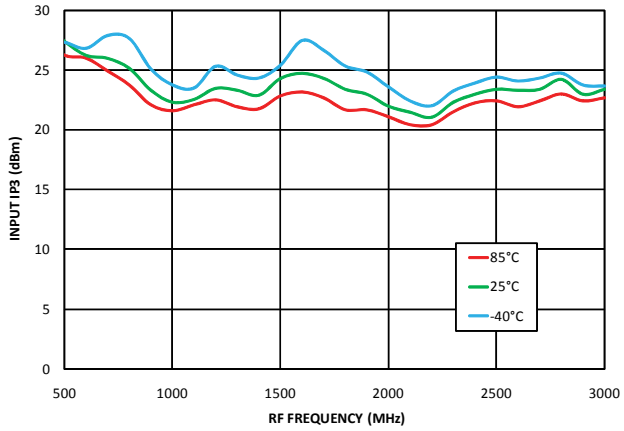

Figure 5. IIP3 versus RF Frequency

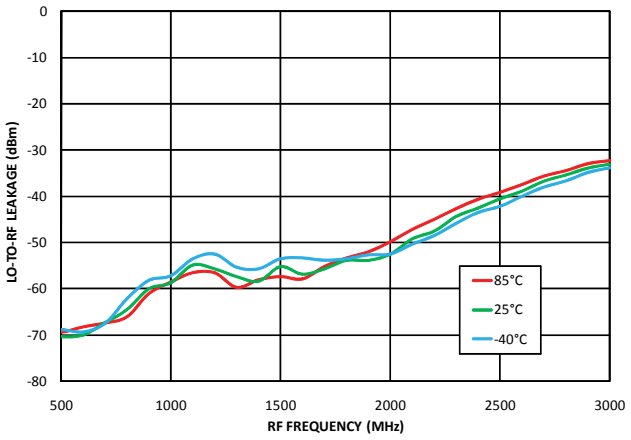

Figure 8. LO to RF Leakage versus RF Frequency

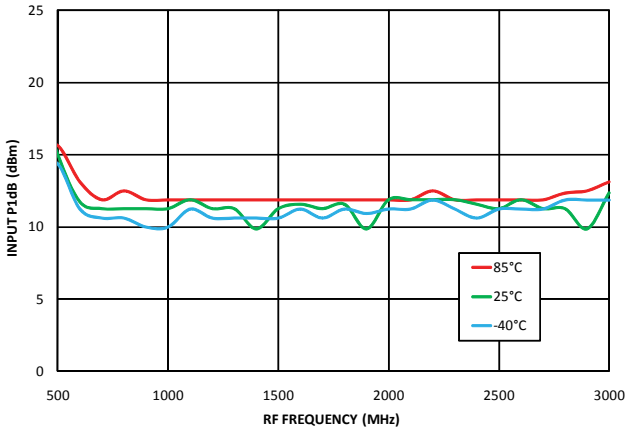

Figure 6. IP1dB versus RF Frequency

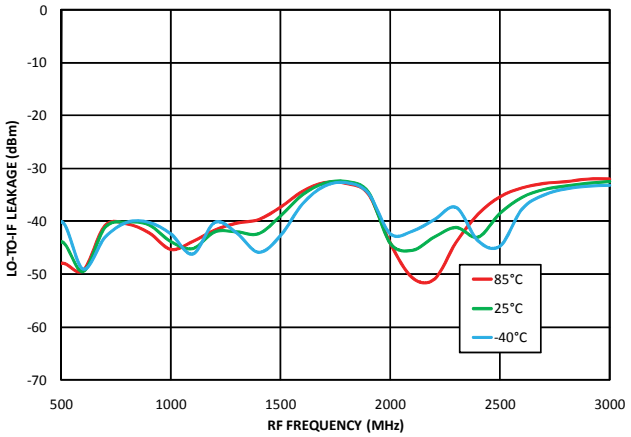

Figure 9. LO to IF Leakage versus RF Frequency

REGISTER STRUCTURE

Figure 10 illustrates the register map of ADL5811. The ADL5811 uses only register 5. As such the Control Bits should be set to 5 in all cases. The ENBL bit, DB7 respectively, when set to 0 will enable the part. By setting this bit to 1 the mixer will be powered down. The CAP DAC RFB IN and Out bits are used to tune the RF Balun. In most cases they will be tuned together with the higher settings, 15, tuning for low frequencies and lower settings, 0, tuning for high frequencies. There are times where it becomes advantageous to tune the input and output of the RF balun separately and that ability is provided for here.

The LPF bits control the Low Pass Filter settings at the IF output. The ability to tune the low pass filter allows some tradeoff between Gain, Noise Figure and Input IP3 with higher settings, 7, providing higher Input IP3 at the cost of some Gain and Noise Figure while lower settings, 0, provide higher Gain and lower NF at the cost of lower Input IP3. The VGS bits control the VGS settings of the mixer core and will allow further tuning of the device.

Figure 11 illustrates the optimum settings characterized for each frequency band.

RESERVED		VGS			LPF		RESERVED	RFB OUT CAP DAC			RESERVED	RFB IN CAP DAC			RESERVED	ENBL	RESERVED				CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	VGS2	VGS1	VGS0	LPF1	LPF0	0	CDO2	CDO1	CDO0	0	CDI2	CDI1	CDI0	0	0	0	0	0	0	C3(1)	C2(0)	C1(1)

VGS2	VGS1	VGS0	VGS SETTING
0	0	0	0
.	.	.	.
1	1	1	7

LP1	LP0	LOW PASS FILTER SETTING
0	0	0
.	.	.
1	1	3

CDO2	CDO1	CDO0	RF BALUN OUTPUT TUNING
0	0	0	0
.	.	.	.
1	1	1	7

CDI2	CDI1	CDI0	RF BALUN INPUT TUNING
0	0	0	0
.	.	.	.
1	1	1	7

ENBL	ENABLE
0	DEVICE ENABLED
1	DEVICE DISABLED

Figure10. ADL5811 Register Maps

RF (MHz)	VGS			LPF		RFB OUT CAP DAC			RFB IN CAP DAC		
	DB21	DB20	DB19	DB18	DB17	DB15	DB14	DB13	DB11	DB10	DB9
	VGS2	VGS1	VGS0	LPF1	LPF0	CDO2	CDO1	CDO0	CDI2	CDI1	CDI0
500	0	0	0	0	1	1	1	1	1	1	1
600	0	0	0	0	1	1	1	0	1	1	0
700	0	0	0	0	1	1	1	0	1	1	0
800	0	0	0	0	1	1	0	0	1	0	0
900	0	0	0	0	1	1	0	0	1	0	0
1000	0	0	0	0	1	1	0	0	1	0	0
1100	0	0	0	0	1	1	0	0	1	0	0
1200	0	0	0	1	0	1	0	0	1	0	0
1300	0	0	0	1	0	0	1	1	0	1	1
1400	0	0	0	1	0	0	1	1	0	1	1
1500	0	0	0	1	0	0	1	1	0	1	1
1600	0	0	0	1	0	0	1	1	0	1	1
1700	0	0	0	1	0	0	1	1	0	1	1
1800	0	0	0	1	0	0	1	1	0	1	1
1900	0	0	0	1	0	0	1	1	0	1	1
2000	0	0	0	1	0	0	1	1	0	1	1
2100	0	0	0	1	0	0	1	1	0	1	1
2200	0	0	0	1	0	0	1	1	0	1	1
2300	0	0	0	1	0	0	0	1	0	1	0
2400	0	0	0	1	0	0	0	0	0	1	0
2500	0	0	0	0	1	0	0	0	0	1	0
2600	0	0	0	0	1	0	0	0	0	1	0
2700	0	0	0	0	1	0	0	0	0	1	0
2800	0	0	0	0	1	0	0	0	0	1	0
2900	0	0	0	0	1	0	0	0	0	1	0
3000	0	0	0	0	1	0	0	0	0	1	0

Figure 11. ADL5811 Optimum Settings

EVALUATION BOARD

An evaluation board is available for the family of double balanced mixers, including the ADL5811. The standard evaluation board schematic is presented in Figure 12. The evaluation board is fabricated on a multilayer Rogers board. Table 4 details the various configuration options of the evaluation board.

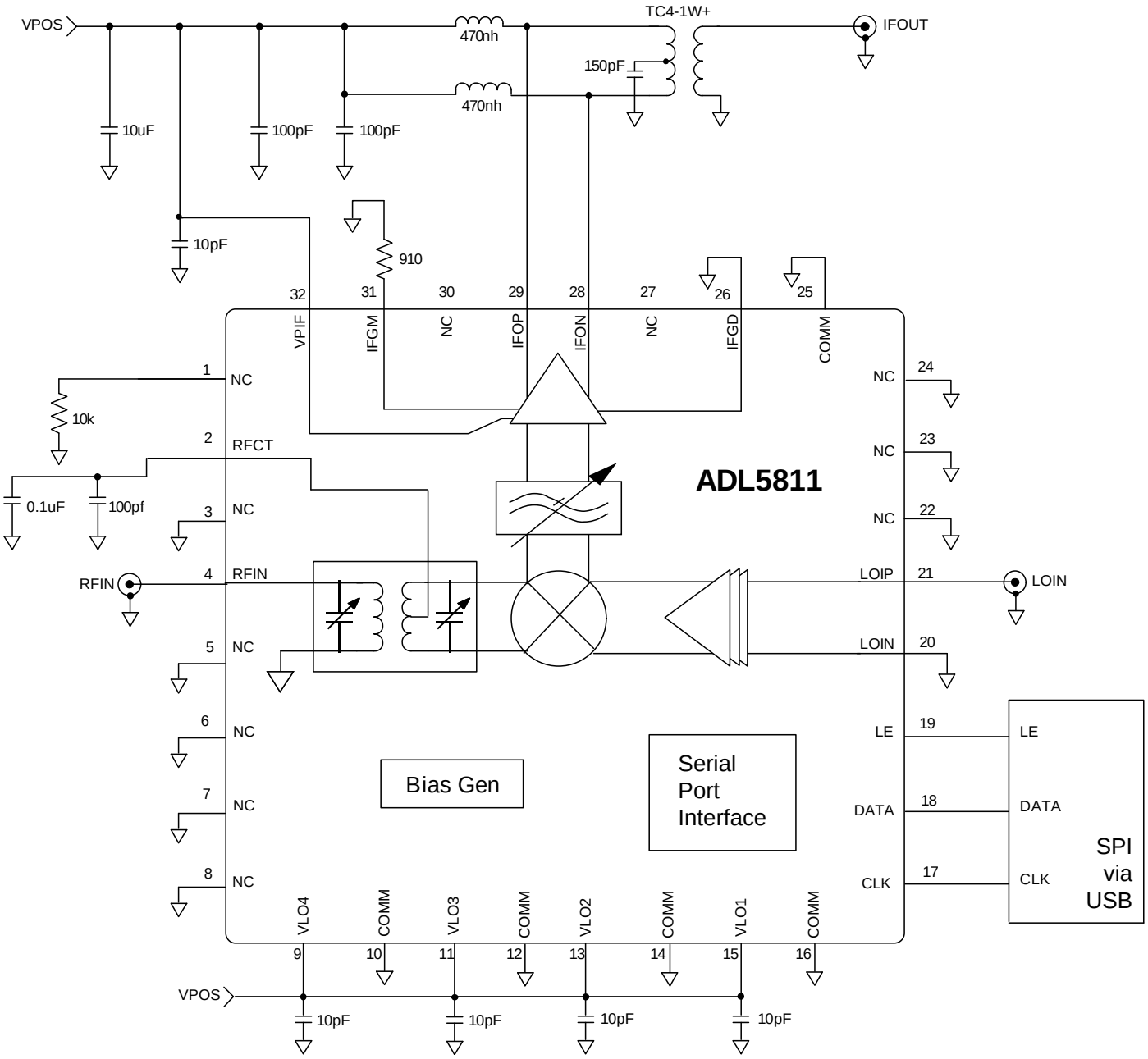

Figure 12. Evaluation Board Schematic.

OUTLINE DIMENSIONS

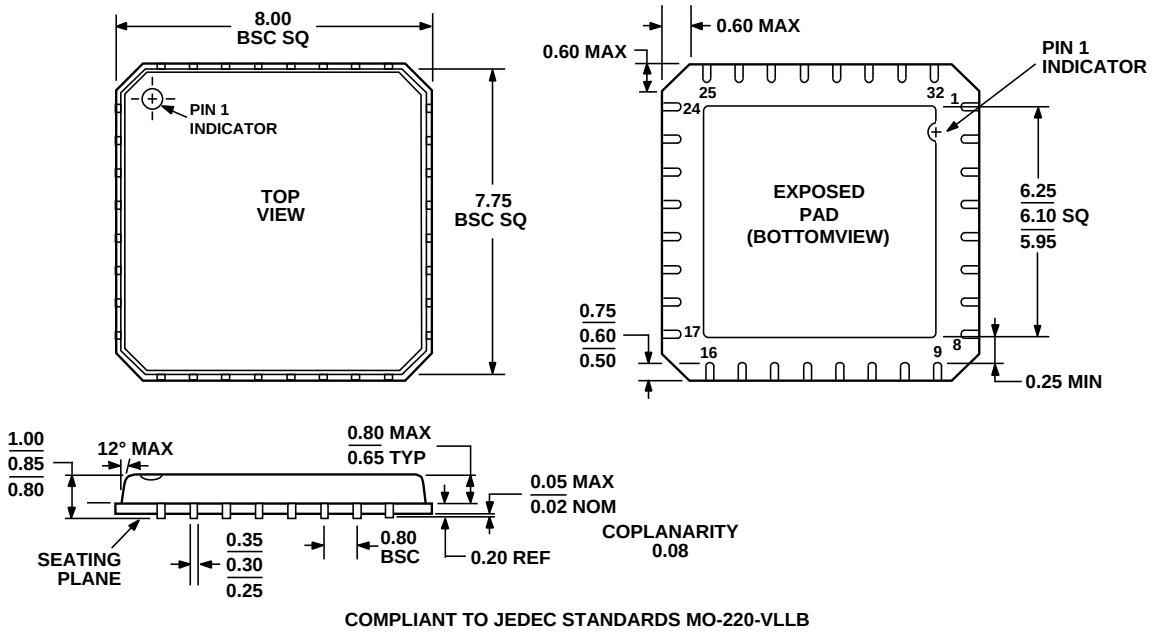

Figure 13. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad (CP-32-5))
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option	Branding	Transport Media Quantity
ADL5811XCPZ-R7[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-5	TBD	TBD, Reel
ADL5811-EVALZ		Evaluation Board			1

[1] *Z = Pb-free part.*