High-IP3
10MHz – 6GHz Active Mixer

Preliminary Technical Data

ADL5801

FEATURES

Wideband Channel Up/Down Converter
Power Conversion Gain of 1.5dB
Wideband RF, LO, and IF ports
SSB Noise Figure of 10dB
Exceptional Blocking SSB NF
Input IP3 of 27dBm
Input P_{1dB} of 12 dBm
Typical LO Drive of 0 dBm
-40dBm LO Leakage at RF
Single Supply Operation: 5 V @ 80 mA
Adjustable Bias for Low Power Operation
Exposed Paddle 4 x 4 mm, 24 Lead LFCSP Package

APPLICATIONS

Cellular Base Station Receivers
Radio Link Downconverters
Broadband Block Conversion
Instrumentation

GENERAL DESCRIPTION

The ADL5801 utilizes a high linearity doubly balanced active mixer core with integrated LO buffer amplifier to provide high dynamic range frequency conversion from 10MHz to 6GHz. The mixer benefits from a proprietary linearization architecture which provides enhanced IP3 performance when subject to high input levels. A bias adjust feature allows the input linearity, SSB Noise Figure, and DC current to be optimized using a single control pin. An optional input power detector is provided for adaptive bias control. The high input linearity allows the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in degradation in dynamic performance. Employing the adaptive bias feature allows the part to provide high IP3 performance when presented with large blocking signals. When blockers are removed the ADL5801 can automatically bias down to provide low noise figure and low power consumption.

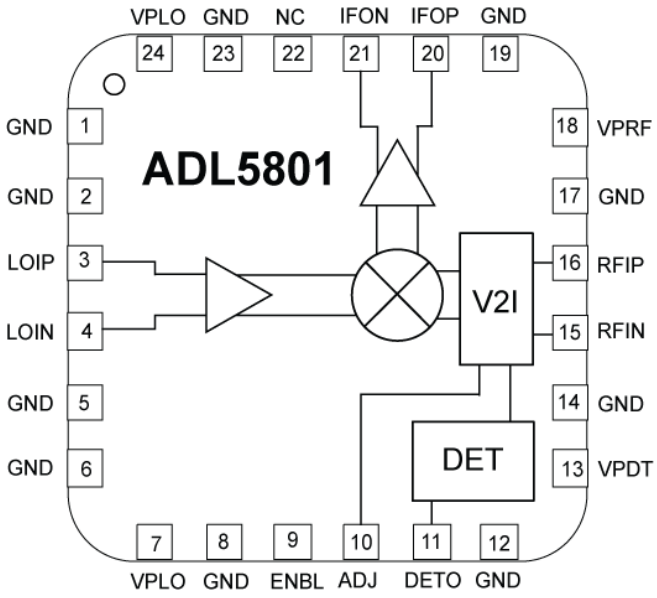

Figure 1. Functional Block Diagram

The balanced active mixer arrangement provides superb LO to RF and LO to IF leakage, typically better than -40dBm. The IF outputs are internally terminated to a 200-Ω source impedance and provide a typical voltage conversion gain of 7.5dB when loaded into a 200-Ω load. The broad frequency range of the open-collector IF outputs allows the ADL5801 to be applied as an up-converter for various transmit applications.

The ADL5801 is fabricated using a SiGe high performance IC process. The device is available in a compact 4mm x 4mm 24-lead LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

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ADL5801—Specifications

Table 1. V_S = 5 V, T_A = 25°C, f_{RF} = 900 MHz, f_{LO} = 703 MHz, LO power = 0 dBm, Zo = 50Ω, ADJ = 3.8V,unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20dB over a limited bandwidth		23		dB
Input Impedance			50		Ω
RF Frequency Range		10		6000	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		200		Ω
IF Frequency Range	Can be matched externally to 3000MHz	LF		600	MHz
without external matching					
DC Bias Voltage[1]			V_S		V
LO INTERFACE					
LO Power		-6	0	+6	dBm
Return Loss			20		dB
Input Impedance			50		Ω
LO Frequency Range		25		6000	MHz
DYNAMIC PERFORMANCE					
Power Conversion Gain	Excluding Transformer and PCB Losses		1.5		dB
Voltage Conversion Gain	Z_{SOURCE} = 50Ω, Differential Z_{LOAD} = 200Ω Differential		7.8		dB
SSB Noise Figure			12		dB
SSB Noise Figure Under-Blocking	+10dBm Blocker present +/-3MHz from wanted RF input, LO source filtered		20		dB
Input Third Order Intercept	f_{RF1} = 900 MHz, f_{RF2} = 901 MHz, f_{LO} = 703 MHz, each RF tone at -10 dBm		28		dBm
Input Second Order Intercept	f_{RF1} = 900 MHz, f_{RF2} = 950 MHz, f_{LO} = 703 MHz, each RF tone at -10 dBm		66		dBm
Input 1 dB Compression Point			12.5		dBm
LO to IF Output Leakage	Unfiltered IF Output		-31		dBm
LO to RF Input Leakage			-31		dBm
RF to IF Output Isolation	Unfiltered IF Output		-36		dB
IF/2 Spurious	-10 dBm Input Power		-65		dBc
POWER INTERFACE					
Supply Voltage		4.5	5	5.5	V
Quiescent Current	Resistor Programmable		135		mA

[1] Supply voltage should be applied from external circuit through choke inductors or IF Transformer center tap.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPRF, VPLO, VPDT	5.5 V
ENBL, ADJ, DETO	TBD
RF Input Power RFOP, RFON	TBD
Internal Power Dissipation	TBD
θ_{JA} (Exposed Paddle Soldered Down)	TBD
θ_{JC} (At Exposed Paddle)	TBD
Maximum Junction Temperature	TBD
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

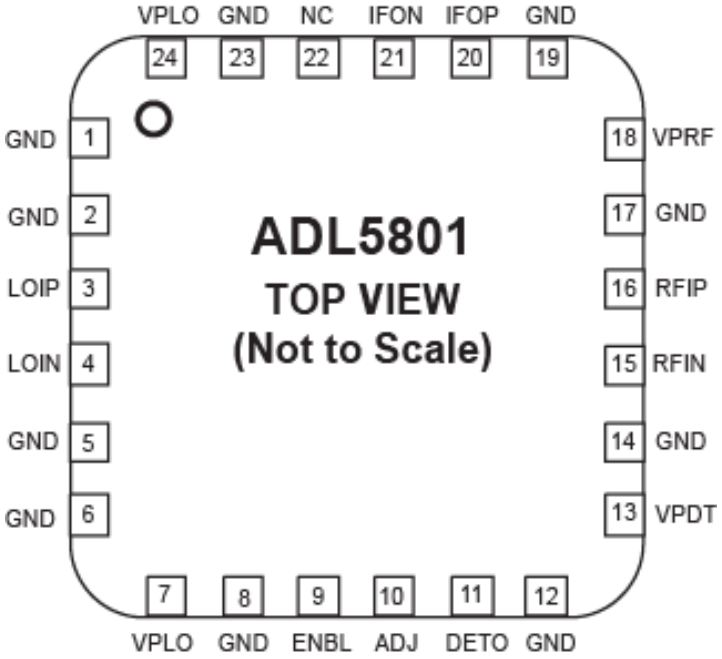

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2, 5, 6, 8,12,14, 17, 19, 23	GND	Device Common (DC Ground).
3, 4	LOIP, LOIN	Differential LO input terminals. Internally matched to 50Ω. Must be ac-coupled.
7, 24	VPLO	Positive Supply Voltage for LO system.
9	ENBL	Device Enable. Pull high to disable the device, pull low to enable.
10	ADJ	IP3 Bias Adjustment. The voltage presented to the ADJ pin sets the internal bias of the mixer core and allows for adaptive control of the IIP3 and NF characteristics of the mixer core.
11	DETO	Detector Output. DETO pin should be loaded with a capacitor to ground. The developed voltage is proportional to the RMS input level. By connecting the DETO output voltage to the ADJ input pin the part will auto bias and increase IP3 performance when presented with large signal input levels.
13	VPDT	Positive Supply Voltage for Detector.
15, 16	RFIP, RFIN	Differential RF input terminal. Internally matched to 50Ω differential input impedance. Must be ac-coupled.
18	VPRF	Positive Supply Voltage for RF Input system.
21,20	IFOP, IFON	Differential IF Output terminals. Need to apply bias through pull-up choke inductors or center tap of the IF transfomer.
22	NC	Not Connected.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, ADJ = 3.8V as measured using typical circuit schematic unless otherwise noted.

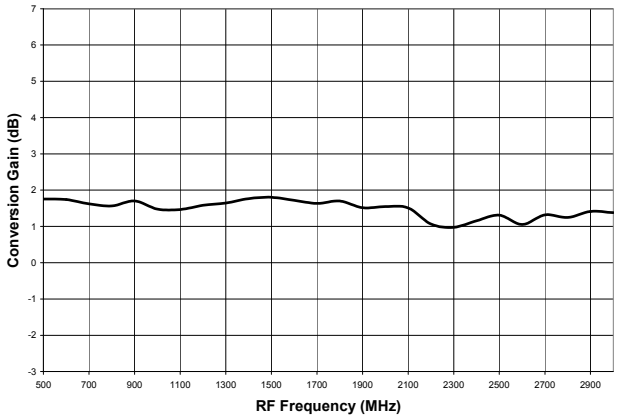

Figure 3. Conversion Gain versus RF Frequency

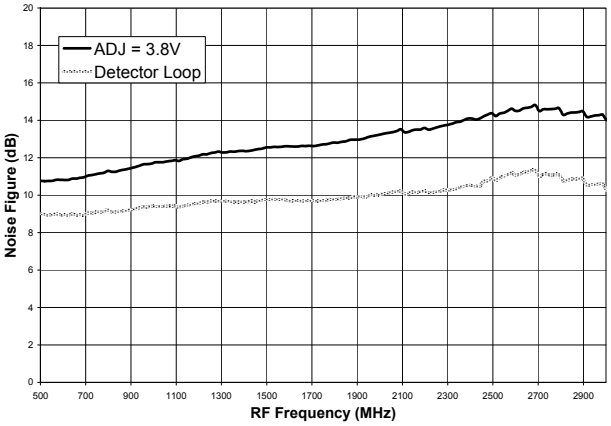

Figure 6. Single-Sideband NF versus RF Frequency

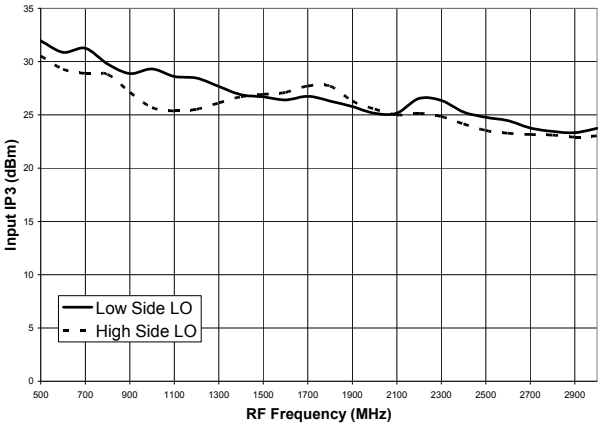

Figure 4. IIP3 versus RF Frequency

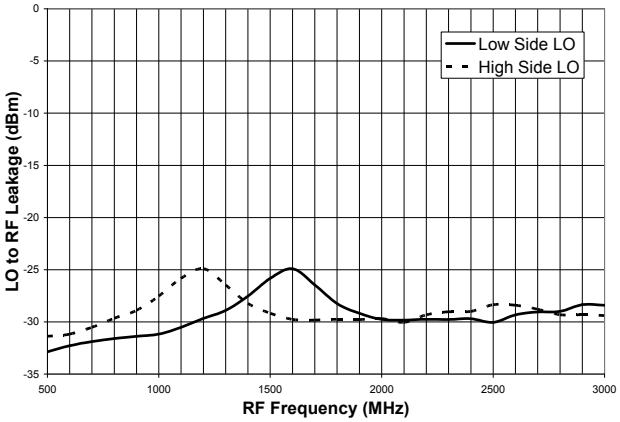

Figure 8. LO to RF Leakage versus LO Frequency

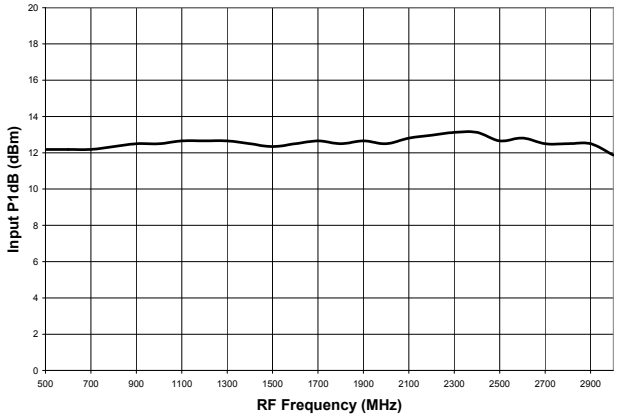

Figure 5. IP1dB versus RF Frequency

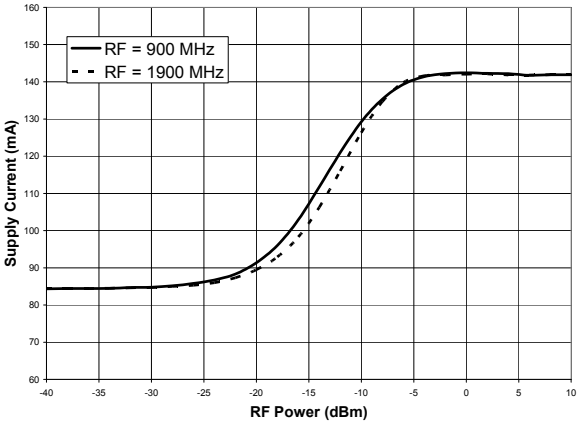

Figure 9. Supply Current versus RF Power with Detector Looped to ISET

EVALUATION BOARD SCHEMATIC

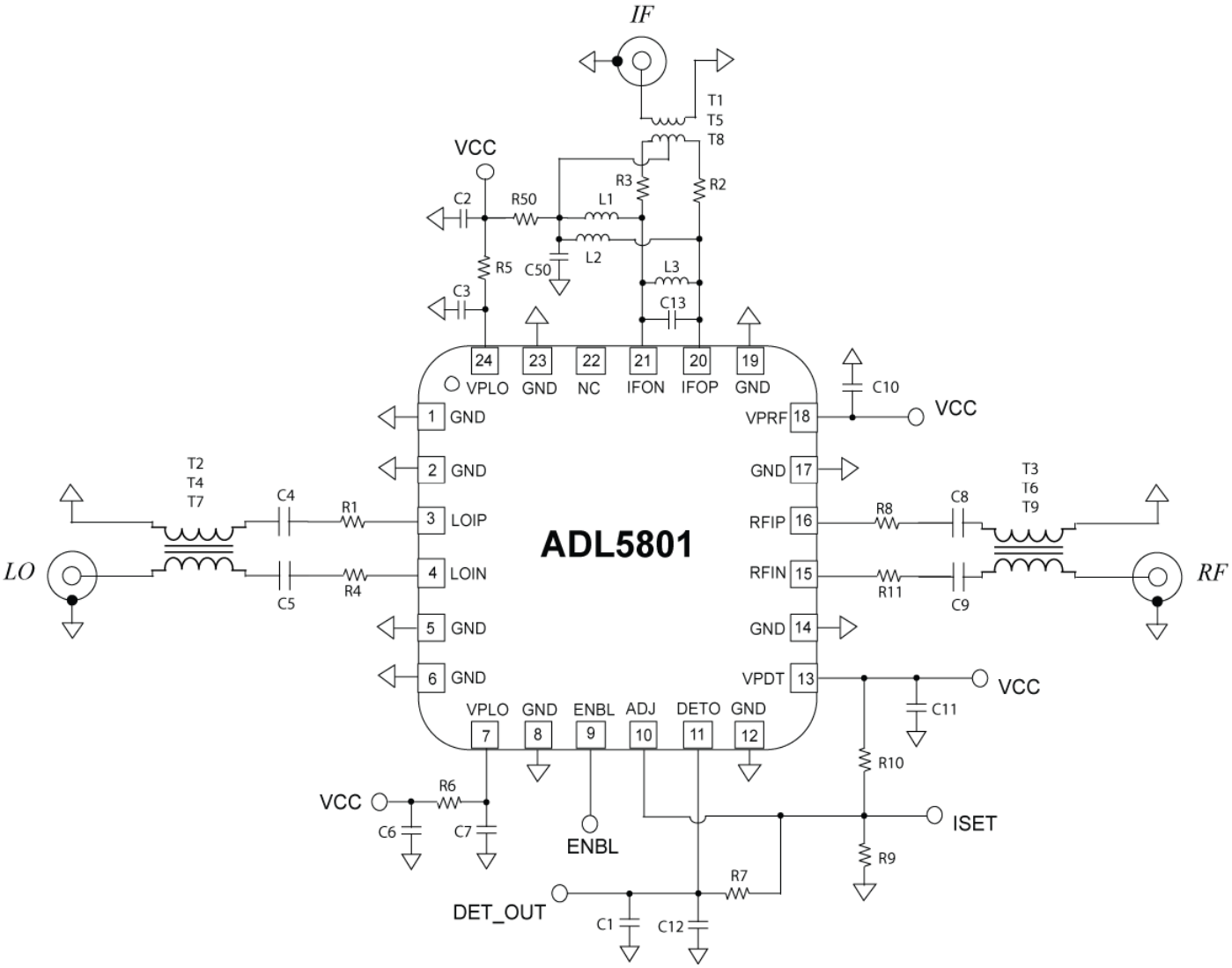

Figure 10. Evaluation Board Schematic.

Table 4. Eval Board Configuration

Components	Function	Default Conditions
C2, C3, C6, C7, C10, C11, R5, R6	Power Supply Decoupling. Nominal supply decoupling consists a 0.1 µF capacitor to ground in parallel with 100pF capacitors to ground positioned as close to the device as possible. Series resistors are provided for enhanced supply decoupling using optional ferrite chip inductors.	C2, C6, C10, C11 = 0.1 µF (size 0402) C3, C7 = 100 pF (size 0402) R5, R6 = 0Ω (size 0402)
C8, C9, T3, T6, T9, RF	RF Input Interfaces. Input channels are ac-coupled through C18 and C9. R8 and R11 provide the options when additional matching is needed. T3 is a 1:1 balun used to interface to the 50-Ω differential inputs. T6 and T9 provides the options when high frequency baluns are used and require smaller balun footprints.	C8, C9 = 100 pF (size 0402) T3 = TC1-1-13M+ (Mini-Circuits)
C13, C50, L1, L2, L3, R2, R3, R50, T1, T5, T8, IF	IF Output Interfaces. The 200-Ω open collector IF output interfaces are biased through the center tap of a 4:1 impedance transformer at T1. C50 provides local bypassing with R50 available for additional supply bypassing. L1 and L2 provide the options when pull-up choke inductors are used to bias the open-collector outputs. C13,	C13 = OPEN (size 0402) C50 = 0.1 µF (size 0402) L1, L2 = OPEN (size 1008) L3 = OPEN (size 0402)

	L3, R2 and R3 are provided for IF filtering and matching options. T5 and T8 provides the options when high frequency baluns are used and require smaller balun footprints.	R2, R3, R50 = 0 Ω (size 0402) T1 = TC4-1W+ (Mini-Circuits)
C4, C5, R1, R4, T2, T4, T7, LO	LO Interface. C4 and C5 provide ac-coupling for the local oscillator input. T2 is a 1:1 balun to allow single-ended interfacing to the differential 50-Ω local oscillator input. R1 and R4 provide the options when additional matching is needed. T4 and T7 provides the options when high frequency baluns are used and require smaller balun footprints.	C4, C5 = 100 pF (size 0402) R1, R4 = 0 Ω (size 0402) T2 = TC1-1-13M+ (Mini-Circuits)
C1, C12, R7, DET_OUT	DET_OUT Interface. C1 and C12 provide decoupling for pin DETO. R7 provide the access to pin ADJ when automatic IP3 control is needed.	C1 = 0.1 µF (size 0603) C12 = 0.01 µF (size 0603) R7 = OPEN (size 0402)
R9, R10, ISET	ADJ Bias Control. R9 and R10 form an optional resistor divider network between VCC and GND, allowing for a fixed bias setting. The default values are set up for 3.8 V at the ADJ pin.	R9, R10 = OPEN (size 0402)

OUTLINE DIMENSIONS

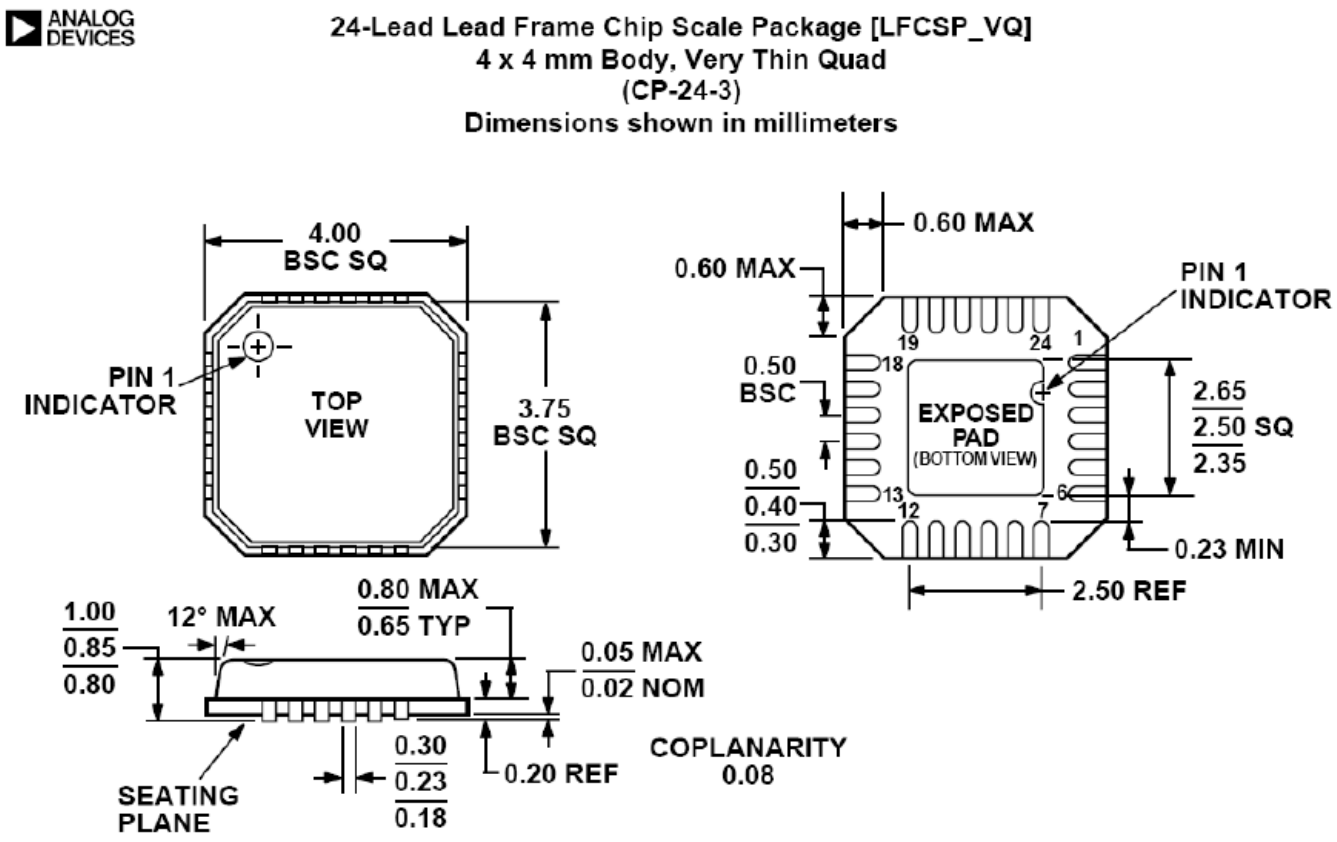

Figure 11. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4mm × 4mm Body, Very Thin Quad (CP-24-2))
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option	Branding	Transport Media Quantity
ADL5801XCPZ-R7[1]	–40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-2	TBD	TBD, Reel
ADL5801-EVALZ		Evaluation Board			1

[1] *Z = Pb-free part.*