Dual Channel High-IP3 100MHz – 6GHz Active Mixer

Preliminary Technical Data

ADL5802

FEATURES

Dual Channel Up/Down Converter
Power Conversion Gain of 1.5dB
Wideband RF, LO, and IF ports
SSB Noise Figure of 11dB
SSB NF with +10dBm blocker of 20dB
Input IP3 of 27dBm
Input P_{1dB} of 12 dBm
Typical LO Drive of 0 dBm
-40dBm LO Leakage at RF
Low Current Operation: 5 V @ 200 mA
Adjustable Bias for Low Power Operation
Exposed Paddle 4 x 4 mm, 24 Lead LFCSP Package

APPLICATIONS

Cellular Base Station Receivers
Main and Diversity Receiver Designs
Radio Link Downconverters

GENERAL DESCRIPTION

The ADL5802 utilizes high linearity doubly balanced active mixer cores with integrated LO buffer amplifiers to provide high dynamic range frequency conversion from 100MHz to 6GHz. The mixers benefit from a proprietary linearization architecture which provides enhanced IP3 performance when subject to high input levels. A bias adjust feature allows the input linearity, SSB Noise Figure, and DC current to be optimized using a single control pin. The high input linearity allows the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in degradation in dynamic performance. The balanced active mixer arrangement provides superb LO to RF and LO to IF leakage, typically better than -40dBm. The IF outputs are internally terminated to a 200-Ω source impedance and provide a typical voltage conversion gain of 7.5 dB when loaded into a 200-Ω load.

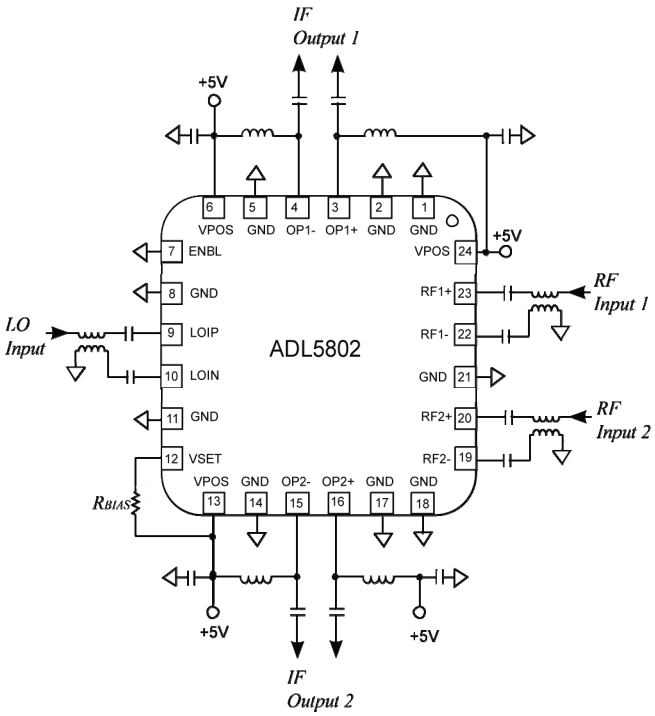

Figure 1. Functional Block Diagram

The ADL5802 is fabricated using a SiGe high performance IC process. The device is available in a compact 4mm x 4mm 24-lead LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

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ADL5802—Specifications

Table 1. V_S = 5 V, T_A = 25°C, f_{RF} = 900 MHz, f_{LO} = 703 MHz, LO power = 0 dBm, Zo = 50Ω, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20dB over a limited bandwidth		12		dB
Input Impedance			50		Ω
RF Frequency Range		100		6000	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		200		Ω
IF Frequency Range	Can be matched externally to 3000MHz	LF		600	MHz
DC Bias Voltage[1]		4.75	V_S	5.25	V
LO INTERFACE					
LO Power		-6	0	+6	dBm
Return Loss			12		dB
Input Impedance			50		Ω
LO Frequency Range		100		6000	MHz
DYNAMIC PERFORMANCE					
Power Conversion Gain	Excluding Transformer and PCB Losses		1.5		dB
Voltage Conversion Gain	Z_{SOURCE} = 50Ω, Differential Z_{LOAD} = 200Ω Differential		7.5		dB
SSB Noise Figure			11		dB
SSB Noise Figure Under-Blocking	+10dBm Blocker present +/-3MHz from wanted RF input, LO source filtered		20		dB
Input Third Order Intercept	f_{RF1} = 889 MHz, f_{RF2} = 890 MHz, f_{LO} = 690 MHz, each RF tone at -10 dBm		27		dBm
Input Second Order Intercept	f_{RF1} = 889 MHz, f_{RF2} = 890 MHz, f_{LO} = 690 MHz, each RF tone at -10 dBm		56		dBm
Input 1 dB Compression Point			12		dBm
LO to IF Output Leakage	Unfiltered IF Output		-65		dBm
LO to RF Input Leakage			-40		dBm
RF to IF Output Isolation	Unfiltered IF Output		-28		dB
RFI1 to RFI2 Channel Isolation			50		dB
IF/2 Spurious	-10 dBm Input Power		-65		dBc
POWER INTERFACE					
Supply Voltage			5		V
Quiescent Current	Resistor Programmable		200		mA
Disable Current	ENBL pin low.		160		mA

[1] Supply voltage should be applied from external circuit through choke inductors or IF Transformer center tap.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
PWDN, VSET	TBD
RF Input Power, RF1+, RF1-, RF2+, RF2-	TBD
Internal Power Dissipation	TBD
θ_{JA} (Exposed Paddle Soldered Down)	TBD
θ_{JC} (At Exposed Paddle)	TBD
Maximum Junction Temperature	TBD
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

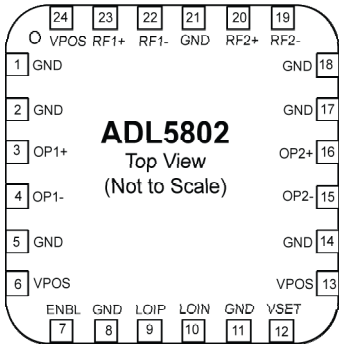

Figure 2. Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Function
1,2,5,8,14, 17,18, 21	GND	Device Common (DC Ground).
3,4	OP1+, OP1-	Channel 1Mixer differential output terminals. Need to apply bias through pull-up choke inductors or center tap of the IF transfomer.
6, 13, 24	VPOS	Positive Supply Voltage. 5.0V Nominal
7	ENBL	Device Enable. Pull low to enable the device, pull high to disable.
9, 10	LOIP, LOIN	Differential LO input terminals. Internally matched to 50Ω. Must be ac-coupled.
12	VSET	High IP3 bias control. For high IP3 performance apply ~4V. Improved NF performance and lower supply current can be set by applying ~2V – 3V to the VSET pin. A resistor can be connected to the supply to raise the voltage while a resistor to GND will lower the voltage.
15, 16	OP2+, OP2-	Channel 2 Mixer differential output terminals. Need to apply bias through pull-up choke inductors or center tap of the IF transfomer.
19. 20	RF2+, RF2-	Differential RF input terminals for channel 2. Internally matched to 50Ω. Must be ac-coupled.
22, 23	RF1+, RF1-	Differential RF input terminals for channel 1. Internally matched to 50Ω. Must be ac-coupled.

TYPICAL PERFORMANCE CHARACTERISTICS–PRELIMINARY DATA

V_S = 5 V, T_A = 25°C, as measured using typical circuit schematic with low-side LO unless otherwise noted

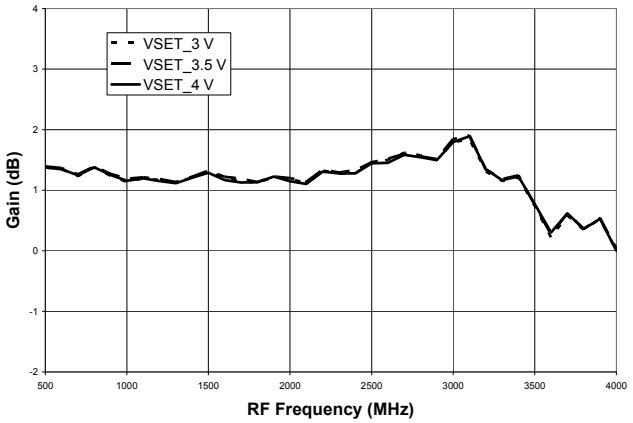

Figure 3. Conversion Gain versus RF Frequency

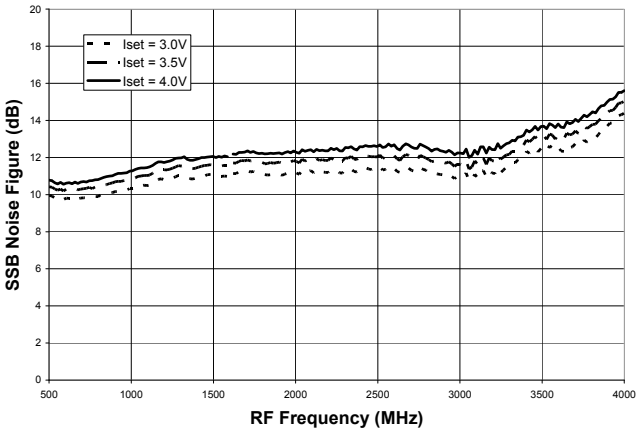

Figure 6. Single-Sideband NF versus RF Frequency

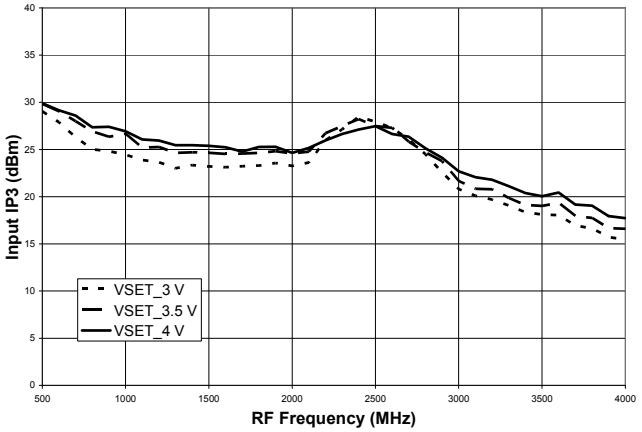

Figure 4. IIP3 versus RF Frequency

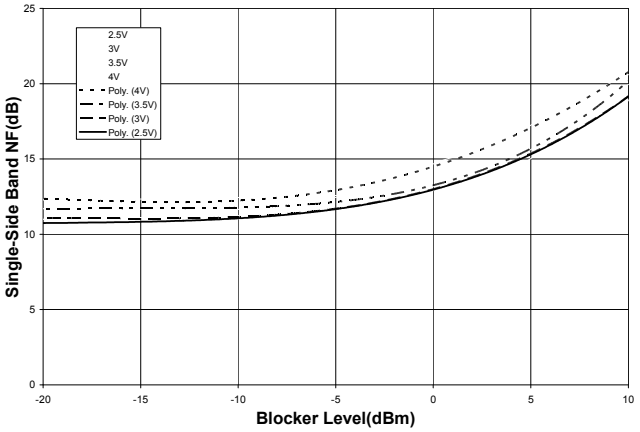

Figure 7. Single-Sideband NF versus Blocker Level at 1950MHz

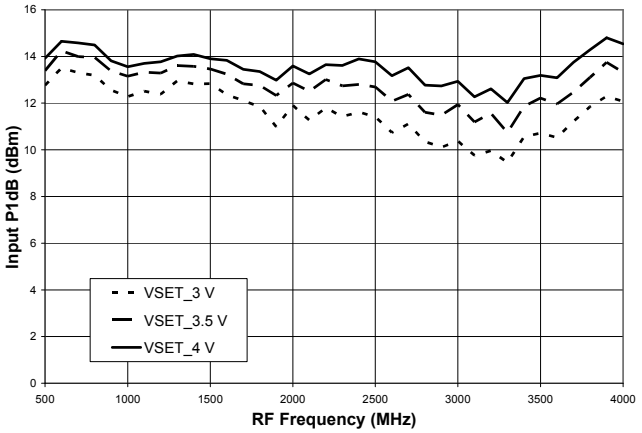

Figure 5. IP1dB versus RF Frequency

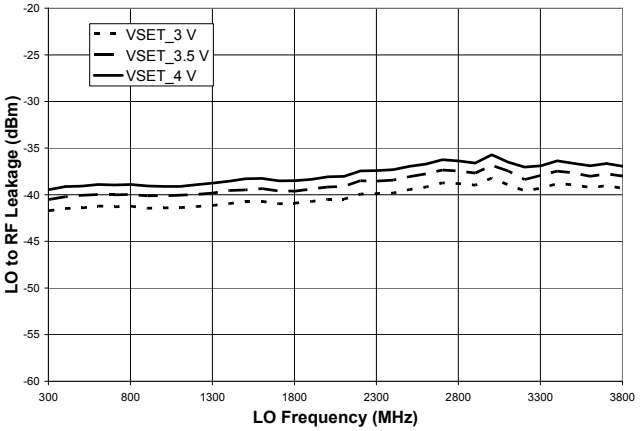

Figure 8. LO to RF Leakage versus LO Frequency

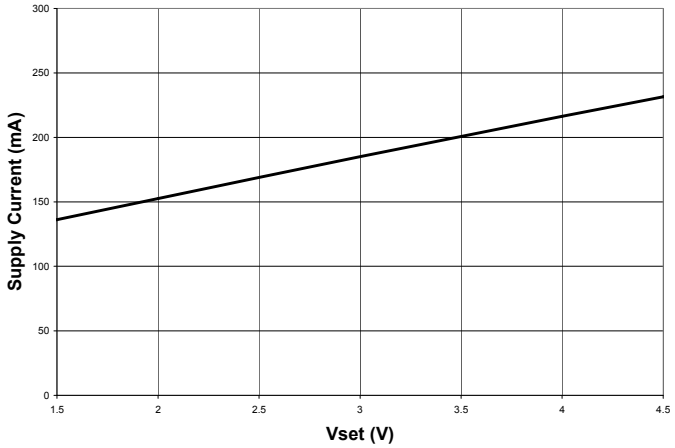

Figure 9. Supply Current vs. Vset

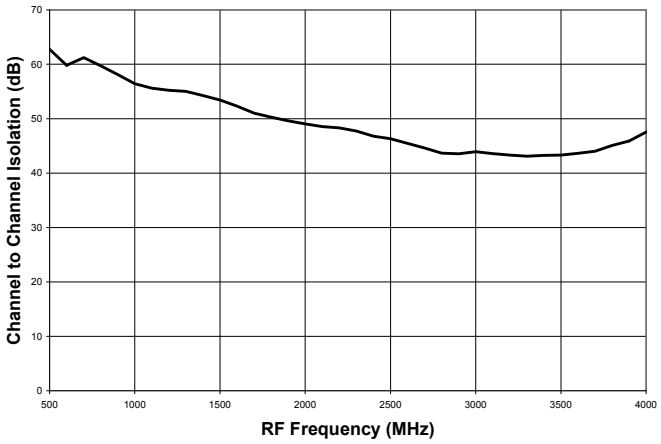

Figure 10. Channel to Channel Isolation vs. RF Frequency

EVALUATION BOARD SCHEMATIC

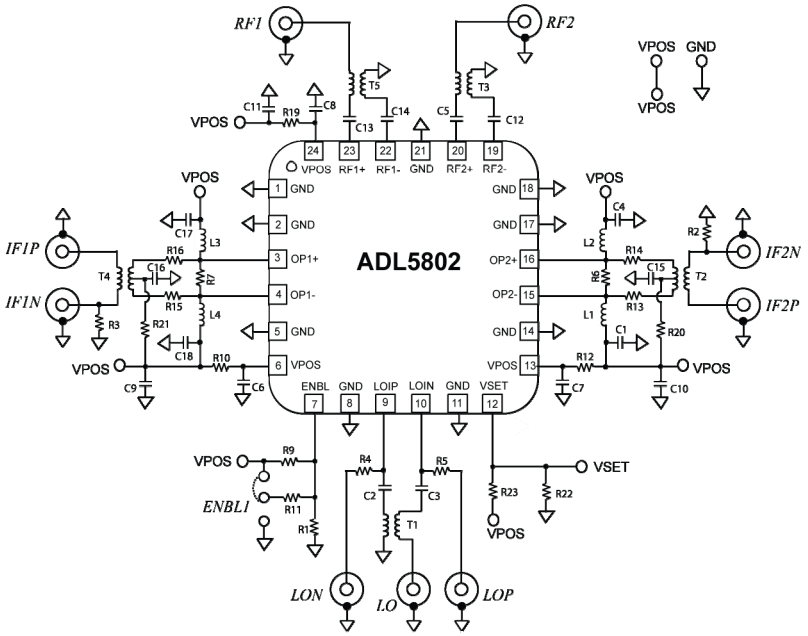

Figure 11. Evaluation Board Schematic.

Table 3. Eval Board Configuration

Components	Function	Default Conditions
C1, C4, C6, C7, C8, C9, C10, C11, C17, C18, R10, R12, R19, R20, R21	Power Supply Decoupling. Nominal supply decoupling consists a 0.01 µF capacitor to ground in parallel with 10pF capacitors to ground positioned as close to the device as possible. Series resistors are provided for enhanced supply decoupling using optional ferrite chip inductors.	C6, C7, C8 = 10pF (size 0402) C9, C10, C11 = 0.01 µF (size 0402) C1, C4, C17, C18 = open (size 0402) R10, R12, R19, R20, R21 = 0Ω (size 0402)
C5, C12, C13, C14, T3, T5, RF1, RF2	RF Channel 1 and Channel 2 Input Interfaces. Input channels are ac-coupled through C5, C12, C13 and C14. T3 and T4 are 1:1 baluns used to interface to the 50-Ω differential inputs.	C5, C12, C13, C14 = 1nF (size 0402) T3, T5 = ETC1-1-13 (M/A-Com)
C15, C16, L1, L2, L3, L4, R2, R3, R6, R7, R13, R14, R15, R16, R20, R21, T2, T4, IF1, IF2	IF Channel 1 and Channel 2 Output Interfaces. The 200-Ω open collector IF output interfaces are biased through the center taps of 4:1 impedance transformers at T2 and T4. C15 and C16 provide local bypassing with R20 and R21 available for additional supply bypassing. L1, L2, L3, and L4 provide the options when pull-up choke inductors are used to bias the open-collector outputs. R6, R7, R13, R14, R15, and R16 are provided for IF filtering and matching options.	C15, C16 = 100pF (size 0402) L1, L2, L3, L4 = open (size 0805) R2, R3, R13, R14, R15, R16, R20, R21 = 0Ω (size 0402) R6, R7 = open (size 0402) T2, T4 = TC4-1W+ (MiniCircuits)
C2, C3, R4, R5, T1, LO	LO Interface. C2 and C3 provide ac-coupling for the local oscillator input. T1 is a 1:1 balun to allow single-ended interfacing to the differential 50-Ω local oscillator input. R4 and R5 provide the options when differential LO interfaces are needed.	C2, C3 = 1nF (size 0402) R4, R5 = 0Ω (size 0402) T1 = ETC1-1-13 (M/A-Com)
R1, R9, R11, ENBL1	ENABLE Interface. The ADL5802 can be disabled using the 3-pin ENBL1 header. The ENBL pin is pulled up to VPOS through R9. R1 is provided as an optional termination for the high impendace enable interface.	R9 = 10kΩ (size 0402) R11 = 0Ω (size 0402) R1 = open (size 0402) ENBL1 = 3-pin header and shunt
R22, R23, VSET	VSET Bias Control. R22 and R23 form an optional resistor divider network between VPOS and GND, allowing for a fixed bias setting. The default values are set up for 3.8 V at the VSET pin.	R22 = 866Ω (size 0402) R23 = 10kΩ (size 0402)

OUTLINE DIMENSIONS

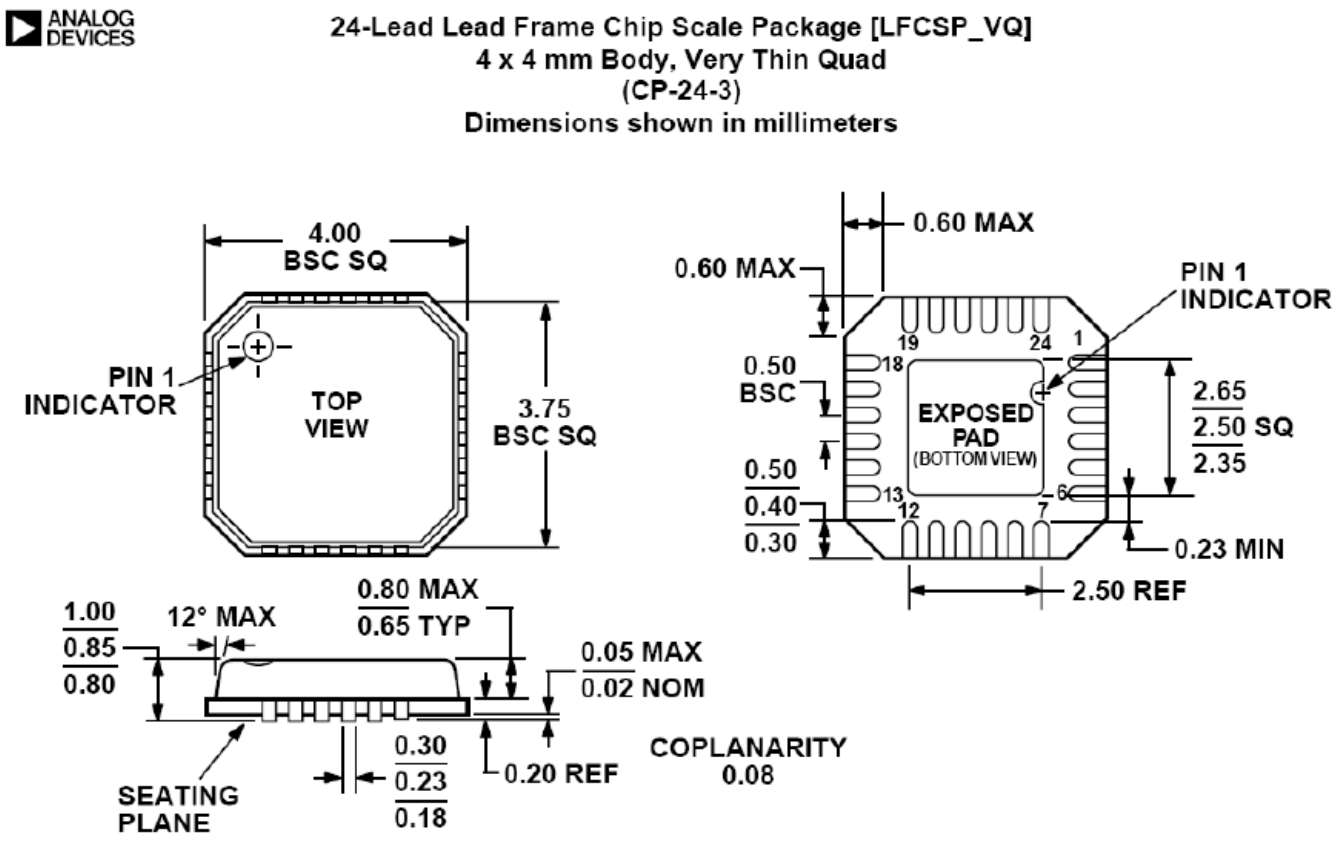

Figure 12. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4mm × 4mm Body, Very Thin Quad (CP-24-2))
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option	Branding	Transport Media Quantity
ADL5802XCPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-2	TBD	TBD, Reel
ADL5802XCPZ-WP	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-2	TBD	TBD, Waffle Pack
ADL5802-EVALZ		Evaluation Board			1