3.3 GHz Ultralow Distortion RF/IF Differential Amplifier

ADL5562

FEATURES

−3 dB bandwidth of 3.3 GHz (A_V = 6 dB)
Pin-strappable gain adjust: 6 dB, 12 dB, 15.5 dB
Differential or single-ended input to differential output
Low noise input stage: 2.1 nV/√Hz RTI @ A_V = 12 dB
Low broadband distortion (Av = 6 dB)
- **10 MHz: −91 dBc HD2, −98 dBc HD3**
- **70 MHz: −102 dBc HD2, −90 dBc HD3**
- **140 MHz: −104 dBc HD2, −84 dBc HD3**
- **250 MHz: −98 dBc HD2, −94 dBc HD3**

IMD3s of −93 dBc at 250 MHz center
Slew rate: 9.8 V/ns
Fast settling and overdrive recovery of 3 ns
Single-supply operation: 3 V to 3.6 V
Power-down control
Fabricated using the high speed XFCB3 SiGe process

APPLICATIONS

Differential ADC drivers
Single-ended to differential conversion
RF/IF gain blocks
SAW filter interfacing

FUNCTIONAL BLOCK DIAGRAM

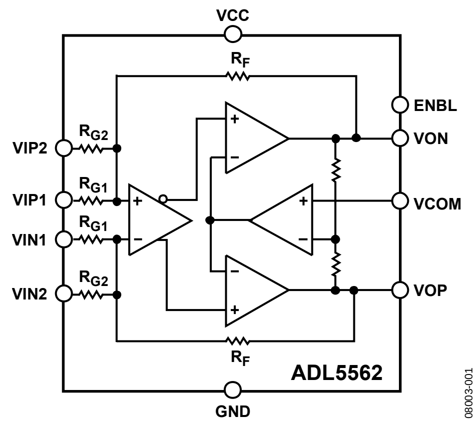

Figure 1.

GENERAL DESCRIPTION

The ADL5562 is a high performance differential amplifier optimized for RF and IF applications. The amplifier offers low noise of 2.1 nV/√Hz and excellent distortion performance over a wide frequency range, making it an ideal driver for high speed 8-bit to 16-bit ADCs.

The ADL5562 provides three gain levels of 6 dB, 12 dB, and 15.5 dB through a pin-strappable configuration. For the single-ended input configuration, the gains are reduced to 5.6 dB, 11.1 dB, and 14.1 dB. Using an external series input resistor expands the amplifier gain flexibility and allows for any gain selection from 0 dB to 15.5 dB.

The quiescent current of the ADL5562 is typically 80 mA and, when disabled, consumes less than 3 mA, offering excellent input-to-output isolation.

The device is optimized for wideband, low distortion performance. These attributes, together with its adjustable gain capability, make this device the amplifier of choice for general-purpose IF and broadband applications where low distortion, noise, and power are critical. This device is optimized for the best combination of slew speed, bandwidth, and broadband distortion. These attributes allow it to drive a wide variety of ADCs and make it ideally suited for driving mixers, pin diode attenuators, SAW filters, and multielement discrete devices.

Fabricated on an Analog Devices, Inc., high speed SiGe process, the ADL5562 is supplied in a compact 3 mm × 3 mm, 16-lead LFCSP package and operates over the temperature range of −40°C to + 85°C.

Rev. 0

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REVISION HISTORY

5/09—Revision 0: Initial Version

SPECIFICATIONS

VCC = 3.3 V, VCOM = 1.65 V, R_L = 200 Ω differential, A_V = 6 dB, C_L = 1 pF differential, *f* = 140 MHz, T_A = 25°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	A_V = 6 dB, V_{OUT} ≤ 1.0 V p-p		3300		MHz
	A_V = 12 dB, V_{OUT} ≤ 1.0 V p-p		3900		MHz
	A_V = 15.5 dB, V_{OUT} ≤ 1.0 V p-p		1900		MHz
Bandwidth for 0.1 dB Flatness	A_V = 6 dB, V_{OUT} ≤ 1.0 V p-p		220		MHz
	A_V = 12 dB, V_{OUT} ≤ 1.0 V p-p		270		MHz
	A_V = 15.5 dB, V_{OUT} ≤ 1.0 V p-p		270		MHz
Gain Accuracy	A_V = 6 dB, R_L = open		0.17		dB
	A_V = 12 dB, R_L = open		0.05		dB
	A_V = 15.5 dB, R_L = open		0.06		dB
Gain Supply Sensitivity	VCC ± 5%		−0.005		dB/V
Gain Temperature Sensitivity	−40°C to +85°C, A_V = 15.5 dB		0.32		mdB/°C
Slew Rate	Rise, A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V step		9.8		V/ns
	Fall, A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V step		10.1		V/ns
Settling Time	2 V step to 1%		2		ns
Overdrive Recovery Time	V_{IN} = 4 V to 0 V step, V_{OUT} ≤ ±10 mV		3		ns
Reverse Isolation (S12)			60		dB
INPUT/OUTPUT CHARACTERISTICS					
Output Common Mode			VCC/2		V
Voltage Adjustment Range			1.4 to 1.8		V
Maximum Output Voltage Swing	1 dB compressed		4.9		V p-p
Output Common-Mode Offset	Referenced to VCC/2		60		mV
Output Common-Mode Drift	−40°C to +85°C		285		μV/°C
Output Differential Offset Voltage			1		mV
CMRR			65		dB
Output Differential Offset Drift	−40°C to +85°C		15		μV/°C
Input Bias Current			3		μA
Input Resistance (Differential)	A_V = 6 dB		400		Ω
	A_V = 12 dB		200		Ω
	A_V = 15.5 dB		133		Ω
Input Resistance (Single-Ended)[1]	A_V = 5.6 dB, R_S = 50 Ω		307		Ω
	A_V = 11.1 dB, R_S = 50 Ω		179		Ω
	A_V = 14.1 dB, R_S = 50 Ω		132		Ω
Input Capacitance (Single-Ended)			0.3		pF
Output Resistance (Differential)			12		Ω
POWER INTERFACE					
Supply Voltage		3	3.3	3.6	V
ENBL Threshold			1		V
ENBL Input Bias Current	ENBL high		−27		μA
	ENBL low		−300		μA
Quiescent Current	ENBL high		75		mA
	ENBL low		3.5		mA

Parameter	Conditions	Min	Typ	Max	Unit
10 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−91/−98		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−95/−98		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−96/−92		dBc
Output Third-Order Intercept/ Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+42/−97		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite. (2 MHz spacing)		+43/−93		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+43/−91		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		3		nV/√Hz
	A_V = 12 dB		2.1		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		19.7		dBm
	A_V = 12 dB		19.6		dBm
	A_V = 15.5 dB		18.2		dBm
70 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−102/−90		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−97/−85		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−93/−83		dBc
Output Third-Order Intercept/ Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+46/−96		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+44/−93		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+43/−91		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		3		nV/√Hz
	A_V = 12 dB		2.1		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		19.6		dBm
	A_V = 12 dB		19.6		dBm
	A_V = 15.5 dB		18.2		dBm
140 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−104/−84		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−82/−81		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−80/−80		dBc
Output Third-Order Intercept/ Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+47/−100		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+45/−95		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+43/−92		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		3		nV/√Hz
	A_V = 12 dB		2.1		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		19.6		dBm
	A_V = 12 dB		19.4		dBm
	A_V = 15.5 dB		18.1		dBm

Parameter	Conditions	Min	Typ	Max	Unit
250 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−98/−94		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−74/−86		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		−74/−84		dBc
Output Third-Order Intercept/ Third-Order Intermodulation Distortion	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+41/−87		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		+40/−86		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		3.2		nV/√Hz
	A_V = 12 dB		2.2		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		19.8		dBm
	A_V = 12 dB		19.3		dBm
	A_V = 15.5 dB		19.1		dBm
500 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−75/−69		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−69/−73		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−72/−75		dBc
Output Third-Order Intercept/ Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+40/−98		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+39/−97		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+38/−93		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		3.7		nV/√Hz
	A_V = 12 dB		2.2		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		18.1		dBm
	A_V = 12 dB		18.1		dBm
	A_V = 15.5 dB		18.1		dBm
1000 MHz NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−70/−60		dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−69/−61		dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p		−66/−59		dBc
Output Third-Order Intercept/ Third-Order Intermodulation Distortion	A_V = 6 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+24/−65		dBm/dBc
	A_V = 12 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+24/−66		dBm/dBc
	A_V = 15.5 dB, R_L = 200 Ω, V_{OUT} = 1 V p-p composite (2 MHz spacing)		+25/−66		dBm/dBc
Noise Spectral Density (RTI)	A_V = 6 dB		4.7		nV/√Hz
	A_V = 12 dB		2.2		nV/√Hz
	A_V = 15.5 dB		1.6		nV/√Hz
1 dB Compression Point (RTO)	A_V = 6 dB		15		dBm
	A_V = 12 dB		15.1		dBm
	A_V = 15.5 dB		15.1		dBm

[1] See the Applications Information section for a discussion of single-ended input, dc-coupled operation.

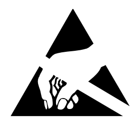
ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VCC)	3.6 V
VIP1, VIP2, VIN1, VIN2	VCC + 0.5 V
Internal Power Dissipation	310 mW
θ_{JA}	98.3°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

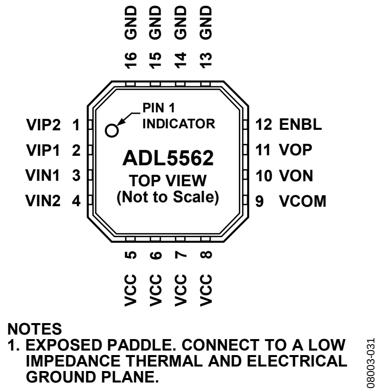


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIP2	Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for A_V = 12 dB gain, strapped to VIP1 for A_V = 15.5 dB.
2	VIP1	Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for A_V = 6 dB gain, strapped to VIP2 for A_V = 15.5 dB.
3	VIN1	Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for A_V = 6 dB gain, strapped to VIN2 for A_V = 15.5 dB.
4	VIN2	Balanced Differential Input. Biased to VCOM, typically ac-coupled. Input for A_V = 12 dB gain, strapped to VIN1 for A_V = 15.5 dB.
5, 6, 7, 8	VCC	Positive Supply.
9	VCOM	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the input and output. Typically decoupled to ground with a 0.1 µF capacitor. With no reference applied, input and output common mode floats to midsupply (VCC/2).
10	VON	Balanced Differential Output. Biased to VCOM, typically ac-coupled.
11	VOP	Balanced Differential Output. Biased to VCOM, typically ac-coupled.
12	ENBL	Enable. Apply positive voltage (1.0 V < ENBL < VCC) to activate device.
13, 14, 15, 16	GND	Ground. Connect to low impedance ground.
	EP	Exposed Pad. Connect to a low impedance thermal and electrical ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

VCC = 3.3 V, VCOM = 1.65 V, R_L = 200 Ω differential, A_V = 6 dB, C_L = 1 pF differential, *f* = 140 MHz, T = 25°C.

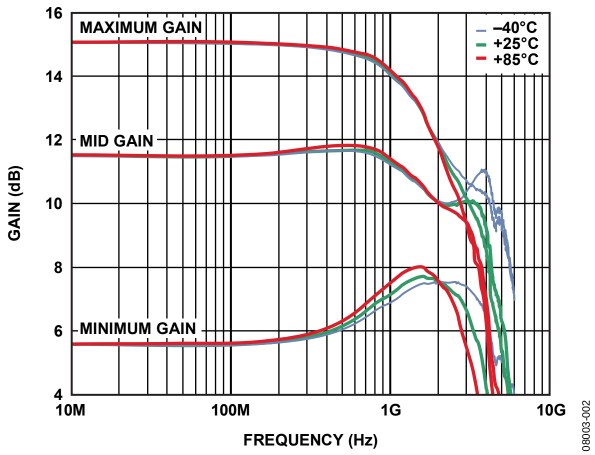


Figure 3. Gain vs. Frequency Response for 200 Ω Differential Load, A_V = 6 dB, 12 dB, and 15.5 dB over Temperature

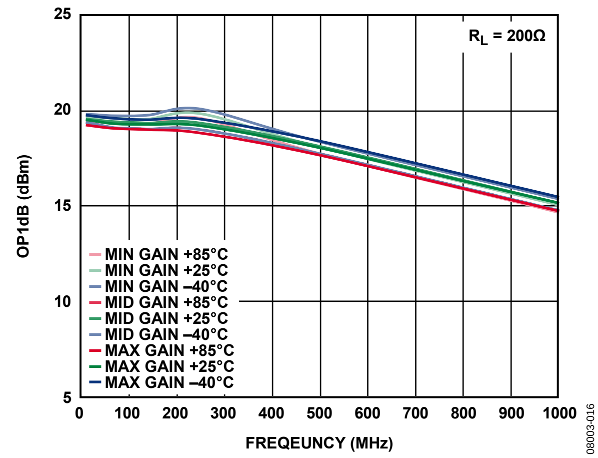


Figure 6. P1 dB vs. Frequency at A_V = 6 dB, 12 dB, and 15.5 dB over Temperature, 200 Ω Differential Load

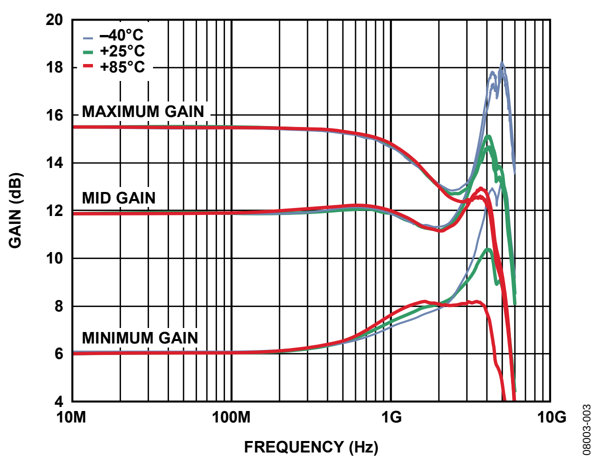


Figure 4. Gain vs. Frequency Response for 1 kΩ Differential Load, A_V = 6 dB, 12 dB, and 15.5 dB over Temperature

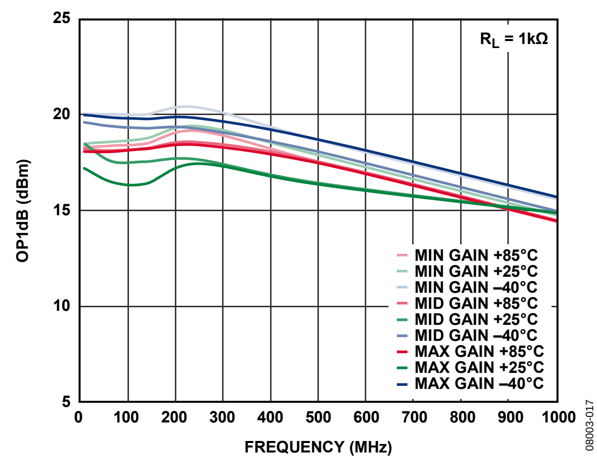


Figure 7. P1 dB vs. Frequency at A_V = 6 dB, 12 dB, and 15.5 dB over Temperature, 1 kΩ Differential Load

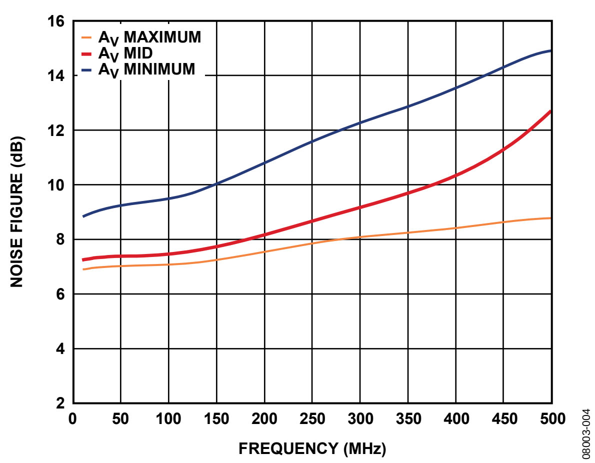


Figure 5. NF vs. Frequency at A_V = 6 dB, 12 dB, and 15.5 dB

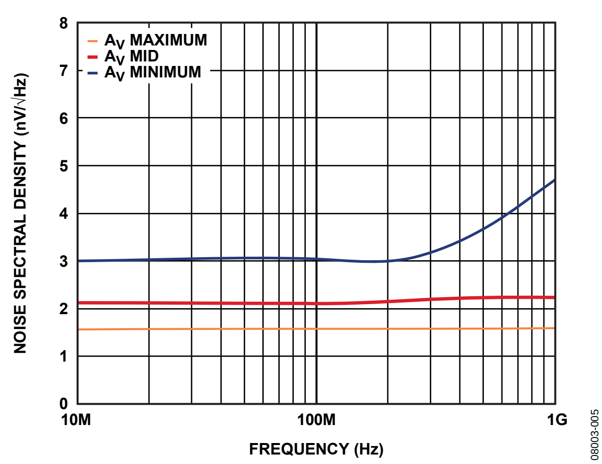


Figure 8. Noise Spectral Density vs. Frequency at A_V = 6 dB, 12 dB, and 15.5 dB

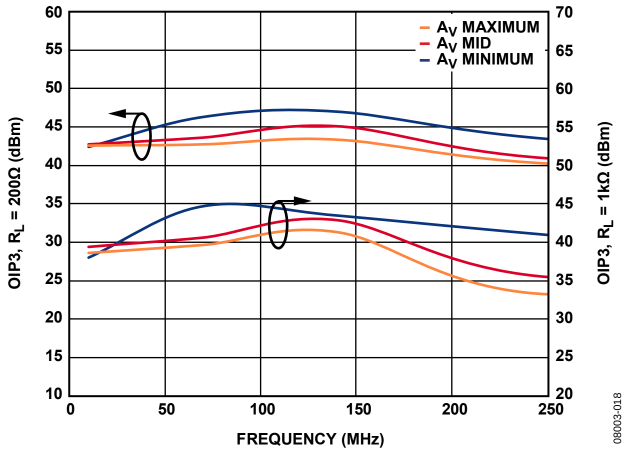


Figure 9. Output Third-Order Intercept at Three Gains, Output Level at 2 V p-p Composite, R_L = 200 Ω and 1 kΩ

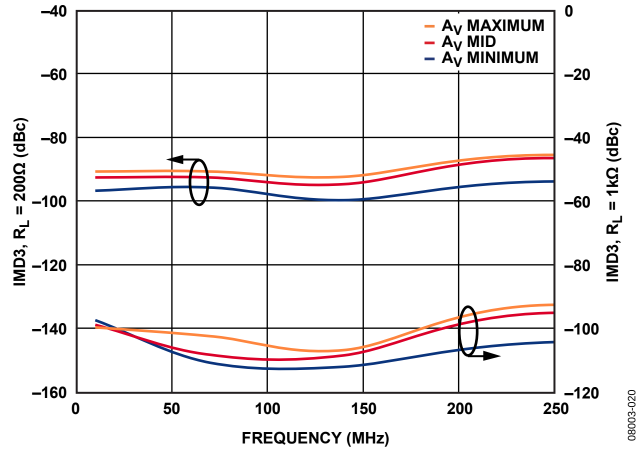


Figure 12. Two-Tone Output IMD vs. Frequency, Output Level at 2 V p-p Composite, R_L = 200 Ω and R_L = 1 kΩ

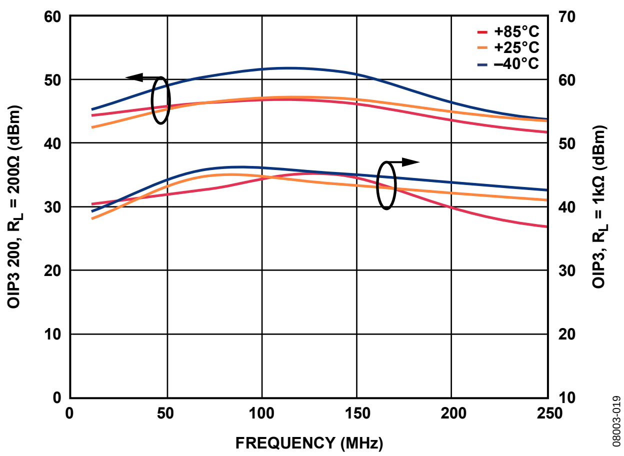


Figure 10. Output Third-Order Intercept vs. Frequency, Over Temperature, Output Level at 2 V p-p Composite, R_L = 200 Ω and R_L = 1 kΩ

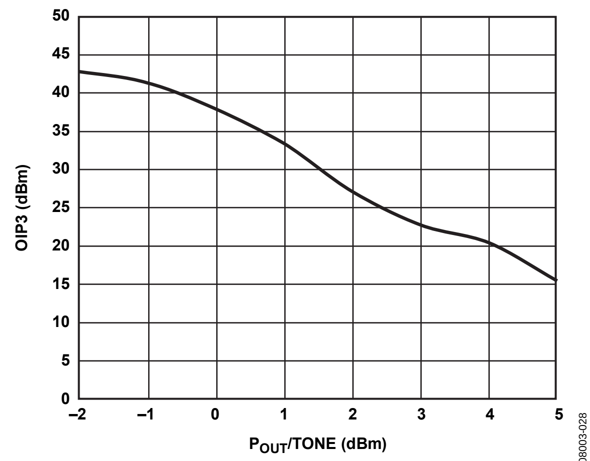


Figure 13. Output Third-Order Intercept vs. Power, Frequency 140 MHz, A_V = 15.5 dB

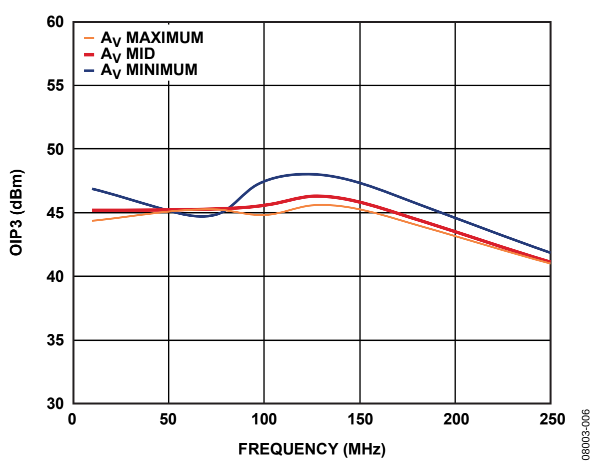


Figure 11. OIP3 vs. Frequency (Single-Ended Input)

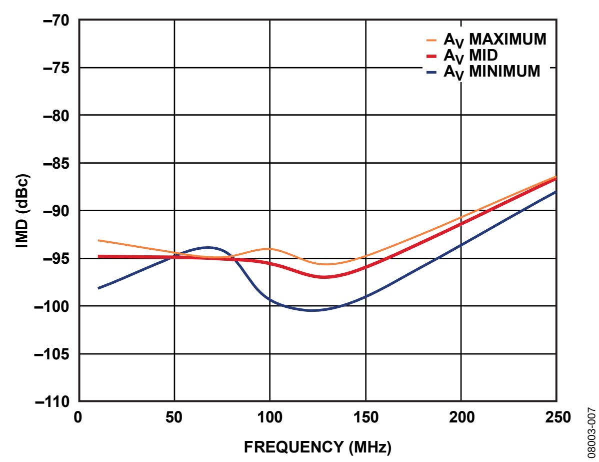


Figure 14. IMD vs Frequency (Single-Ended Input)

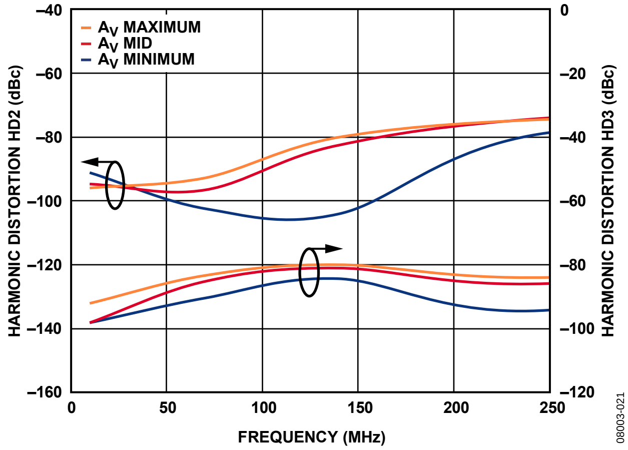


Figure 15. Harmonic Distortion vs. Frequency at A_V = 6 dB, 12 dB, and 15.5 dB, Output Level at 2 V p-p, R_L = 200 Ω

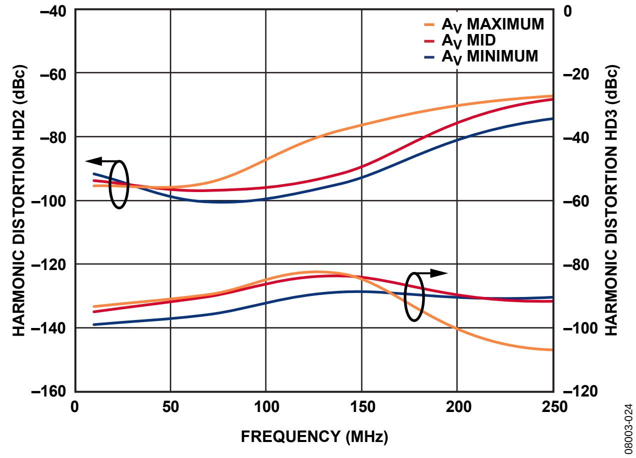


Figure 18. Harmonic Distortion vs. Frequency at A_v = 6 dB, 12 dB, and 15.5 dB, Output Level at 2 V p-p, R_L = 1 k Ω

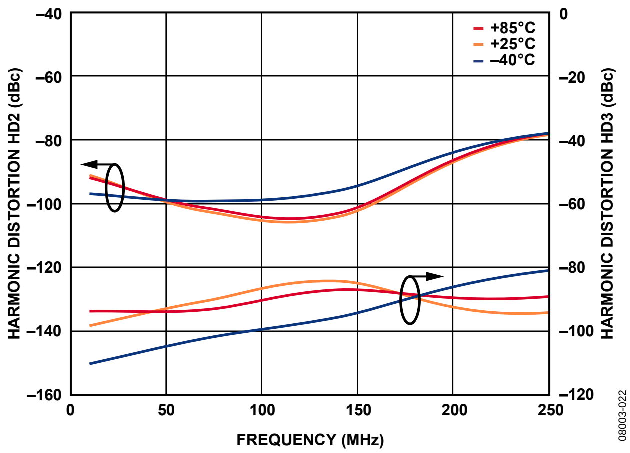


Figure 16. Harmonic Distortion vs. Frequency, Three Temperatures, Output Level at 2 V p-p, R_L = 200 Ω

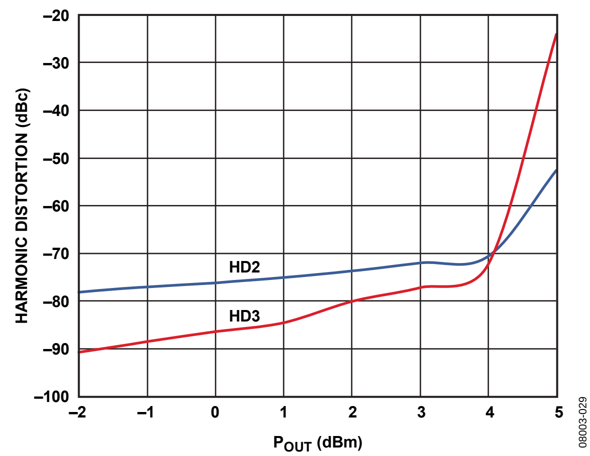


Figure 19. Harmonic Distortion vs. Power, Frequency 140 MHz, A_V = 15.5 dB

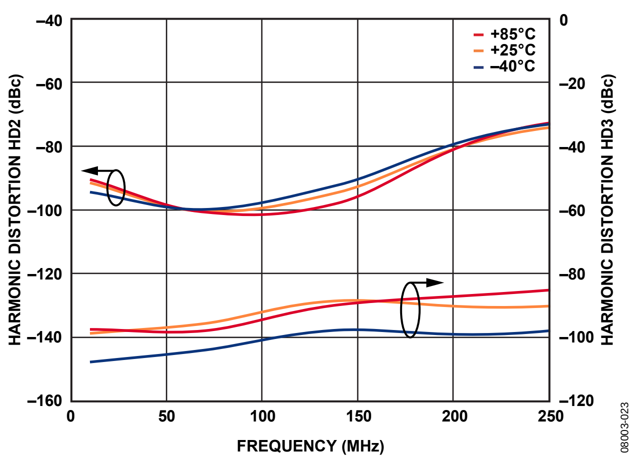


Figure 17. Harmonic Distortion vs. Frequency, Over Temperature, Output Level at 2 V p-p , R_L = 1 kΩ

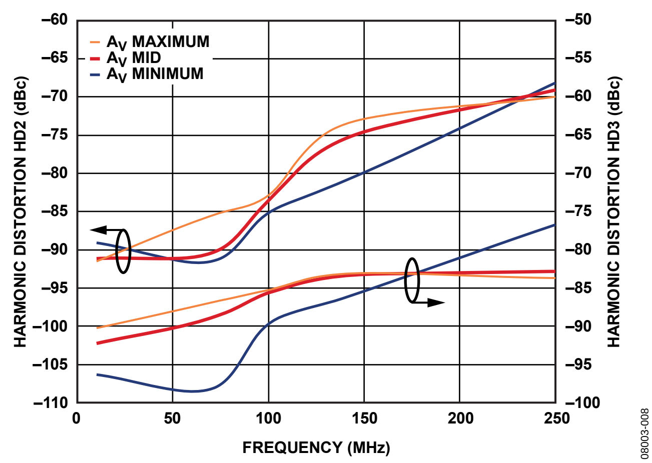


Figure 20. HD2/HD3 vs. Frequency (Single-Ended Input)

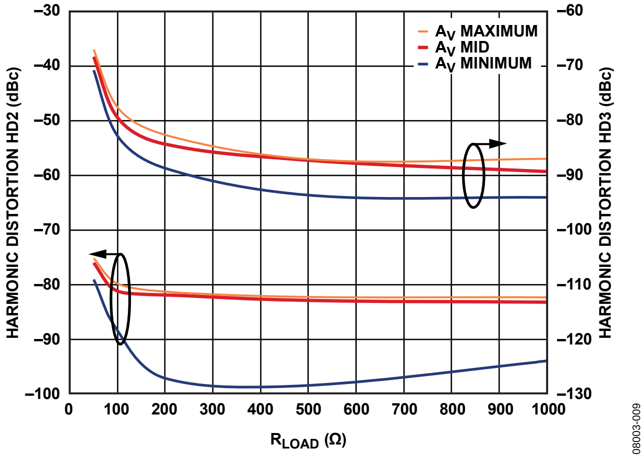


Figure 21. HD2/HD3 vs. Load

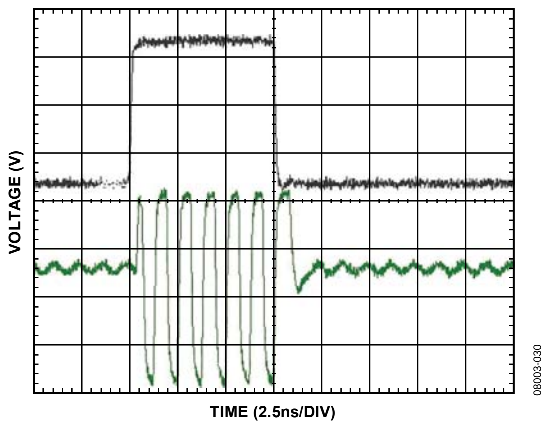


Figure 22. ENBL Time Domain Response

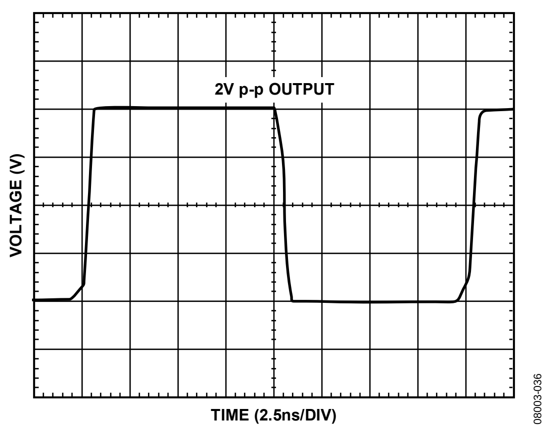


Figure 23. Large Signal Pulse Response, $A_V = 15.5$ dB

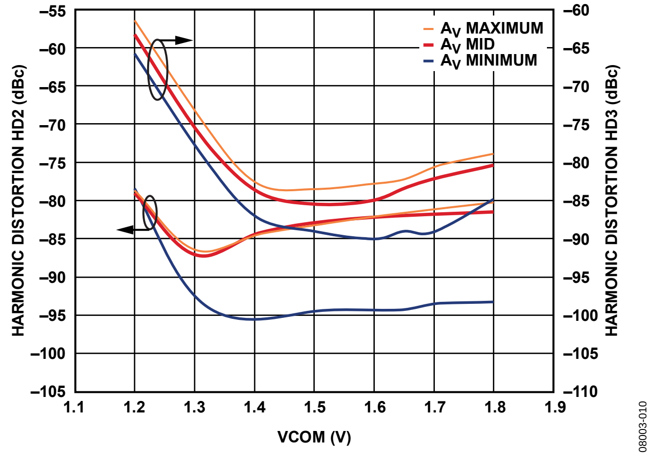


Figure 24. HD2/HD3 vs. VCOM

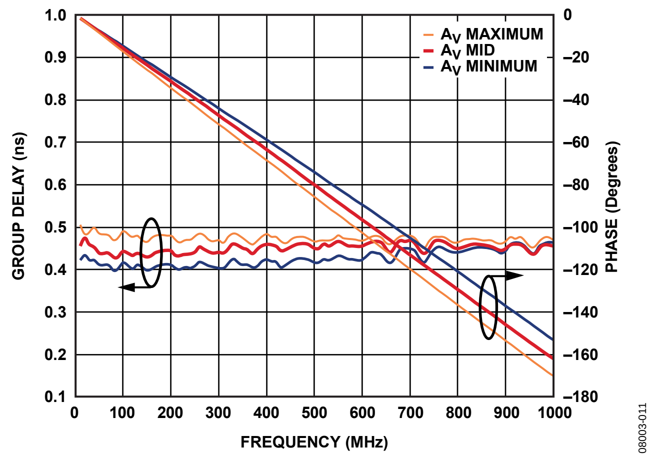


Figure 25. Group Delay and Phase vs. Frequency

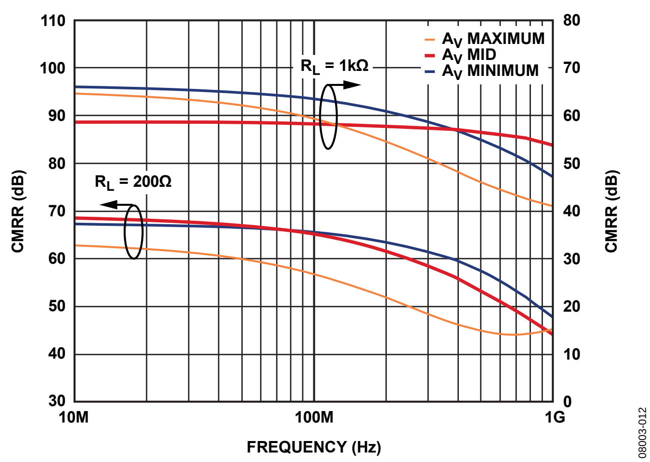


Figure 26. Common-Mode Rejection Ratio vs. Frequency

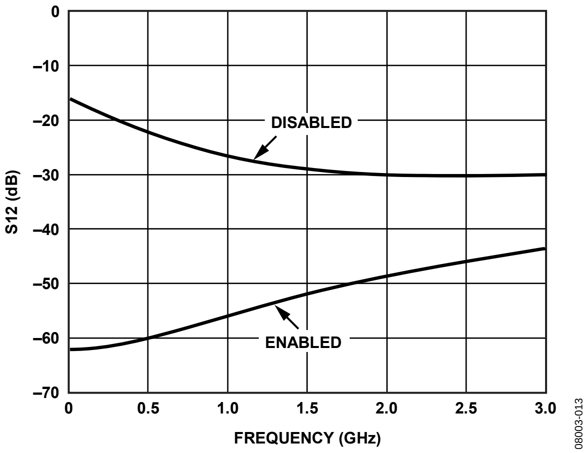


Figure 27. Reverse Isolation vs. Frequency

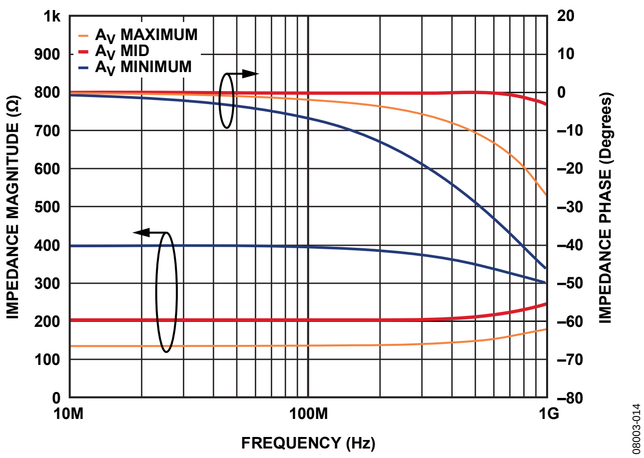


Figure 28. Input Impedance vs. Frequency

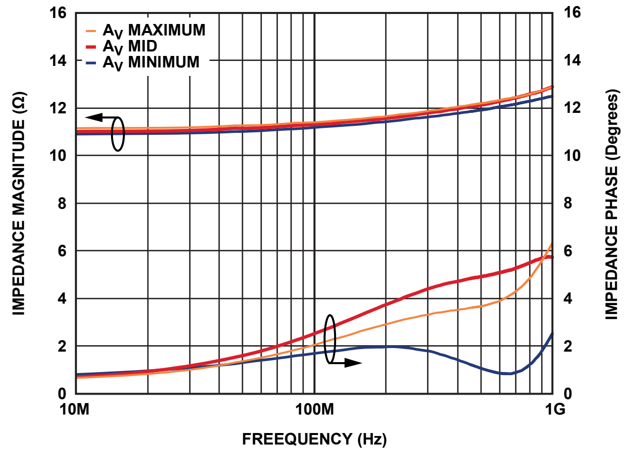


Figure 29. Output Impedance vs. Frequency

CIRCUIT DESCRIPTION

BASIC STRUCTURE

The ADL5562 is a low noise, fully differential amplifier/ADC driver that uses a 3.3 V supply. It provides three gain options (6 dB, 12 dB, and 15.5 dB) without the need for external resistors and has wide bandwidths of 2.6 GHz for 6 dB, 2.3 GHz for 12 dB, and 2.1 GHz for 15.5 dB. Input impedance is 400 Ω differential for 6 dB, 200 Ω for 12 dB, and 133 Ω for 15.5 dB. It has a differential output impedance of 10 Ω and a common-mode adjust voltage of 1.25 V to 1.85 V.

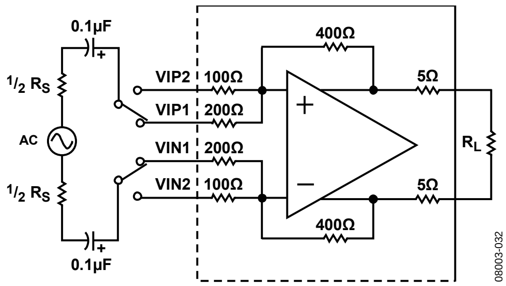


Figure 30. Basic Structure

The ADL5562 is composed of a fully differential amplifier with on-chip feedback and feed-forward resistors. The two feed-forward resistors on each input set this pin-strappable amplifier in three different gain configurations of 6 dB, 12 dB, and 15.5 dB. The amplifier is designed to provide high differential open-loop gain and an output common-mode circuit that enables the user to change the common-mode voltage from a VCOM pin. The amplifier is designed to provide superior low distortion at frequencies up to and beyond 300 MHz with low noise and low power consumption. The low distortion and noise are realized with a 3.3 V power supply at 80 mA.

The ADL5562 is very flexible in terms of I/O coupling. It can be ac-coupled or dc-coupled at the inputs and/or the outputs within the specified input and output common-mode levels. The input of the device can be configured as single-ended or differential with similar distortion performance. Due to the internal connections between the inputs and outputs, the user should keep the output common-mode voltage between 1.25 V and 1.85 V for the best distortion. For a dc-coupled input, the input common mode should be between 1 V and 2.3 V for the best distortion. The device has been characterized using 2 V p-p into 200 Ω. If the inputs are ac-coupled, the input and output common-mode voltages are set by VCC/2 when no external circuitry is used. The ADL5562 provides an output common-mode voltage set by VCOM, which allows driving an ADC directly without external components such as a transformer or ac-coupling capacitors, provided the VCOM of the amplifier is within the VCOM of the ADC. For dc-coupled requirements, the input VCM must be set by the VCOM pin in all three gain settings.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 31 shows the basic connections for operating the ADL5562. VCC should be 3.3 V with each supply pin decoupled with at least one low inductance surface-mount ceramic capacitor of 0.1 uF placed as close as possible to the device. The VCOM pin (Pin 9) should also be decoupled using a 0.1 uF capacitor.

The gain of the part is determined by the pin-strappable input configuration. When Input A is applied to VIP1 and Input B is applied to VIN1, the gain is 6 dB (minimum gain, see the gain vs. load equations). When Input A is applied to VIP2 and Input B is applied to VIN2, the gain is 12 dB (middle gain). When Input A is applied to VIP1 and VIP2 and Input B is applied to VIN1 and VIN2, the gain is 15.5 dB (maximum gain).

Input Pin 1 to Input Pin 4, Output Pin 10, and Output Pin 11 are biased at 1/2 VCC above ground and can be dc-coupled (if within the specified input or output common mode voltage levels) or ac-coupled as shown in Figure 31.

To enable the ADL5562, the ENBL pin must be pulled high. Pulling the ENBL pin low puts the ADL5562 in sleep mode, reducing the current consumption to 3 mA at ambient.

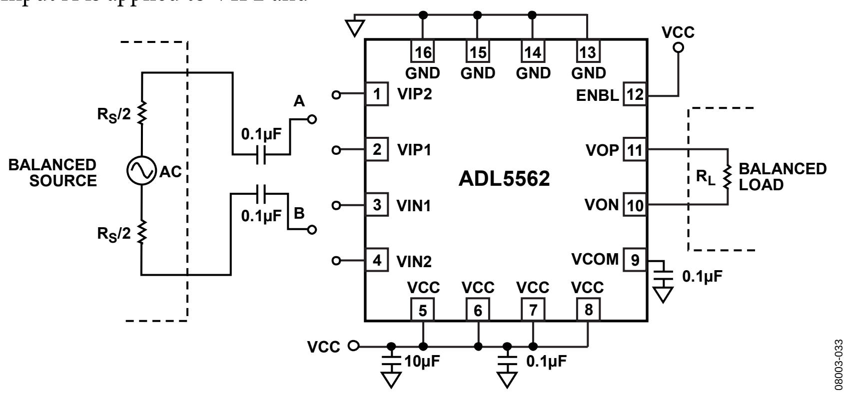


Figure 31. Basic Connections

INPUT AND OUTPUT INTERFACING

The ADL5562 can be configured as a differential-input to differential-output driver as shown in Figure 32. The differential broadband input is provided by the ETC1-1-13 balun transformer, and the two 34.8 Ω resistors provide a 50 Ω input match for the three input impedances that change with the variable gain strapping. The input and output 0.1 µF capacitors isolate the VCC/2 bias from source and balanced load. The load should equal 200 Ω to provide the expected ac performance (see the Specifications section and the Typical Performance Characteristics section).

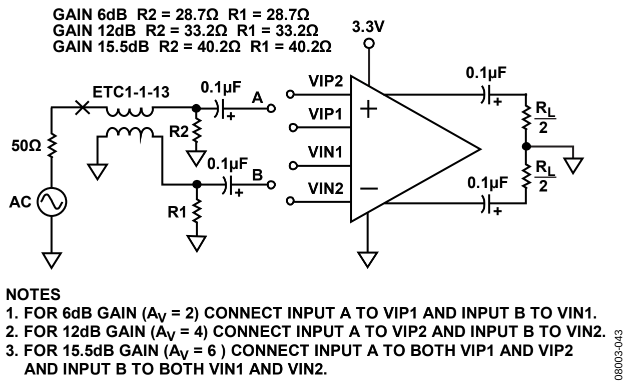


Figure 32. Differential-Input to Differential-Output Configuration

Table 4. Differential Termination Values for Figure 32

Gain (dB)	R1 (Ω)	R2 (Ω)
6	28.7	28.7
12	33.2	33.2
15.5	40.2	40.2

The differential gain of the ADL5562 is dependent on the source impedance and load, as shown in Figure 33.

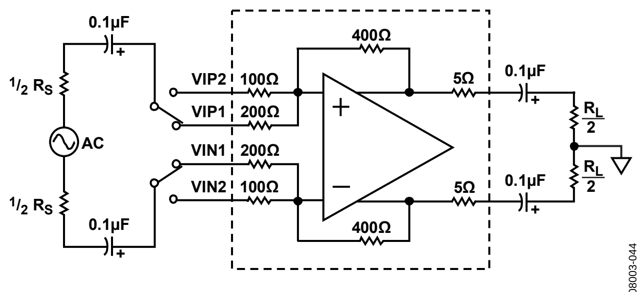


Figure 33. Differential Input Loading Circuit

The differential gain can be determined using the formula below. The values of R_{IN} for each gain configuration are shown in Table 5.

$$A_V = \frac{800}{R_S + 2R_{IN}} \times \frac{R_L}{10 + R_L} \quad (1)$$

Table 5. Values of R_{IN} for Differential Gain

Gain (dB)	R_{IN} (Ω)
6	200
12	100
15.5	66.7

Single-Ended Input to Differential Output

The ADL5562 can also be configured in a single-ended input to differential output driver, as shown in Figure 34. In this configuration, the gain of the part is reduced due to the application of the signal to only one side of the amplifier. The strappable gain values are listed in Table 6 with the required terminations to match to a 50 Ω source using R1 and R2. Note that R1 must equal the parallel value of the source and R2. The input and output 0.1 µF capacitors isolate the VCC/2 bias from the source and the balanced load. The performance for this configuration is shown in Figure 11, Figure 14, and Figure 20.

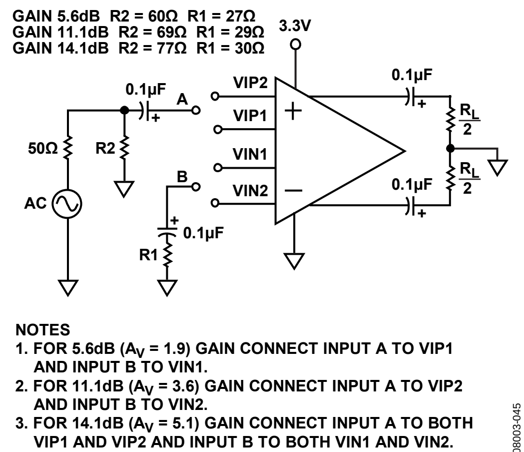


Figure 34. Single-Ended Input to Differential Output Configuration

Table 6. Single-Ended Termination Values for Figure 34

Gain (dB)	R1 (Ω)	R2 (Ω)
5.6	27	60
11.1	29	69
14.1	30	77

The single-ended gain configuration of the ADL5562 is dependent on the source impedance and load, as shown in Figure 35.

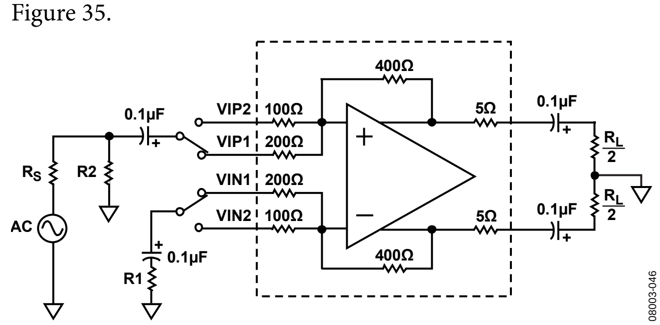


Figure 35. Single-Ended Input Loading Circuit

The single-ended gain can be determined using the following formula below. The values of R_{IN} and R_X for each gain configuration are shown in Table 7.

$$A_{V1} = \frac{400}{R_N + \left(\frac{R_S \times R2}{R_S + R2}\right)} \times \frac{R2}{R_S + R2} \times \frac{R_X + R_S}{R_X} \times \frac{R_L}{10 + R_L} \quad (2)$$

Table 7. Values of R_{IN} and R_X for Single-Ended Gain

Gain (dB)	R_{IN} (Ω)	R_X (Ω)
5.6	200	R2 || 307[1]
11.1	100	R2 || 179[1]
14.1	66.7	R2 || 132[1]

[1] These values based on a 50 Ω input match.

GAIN ADJUSTMENT AND INTERFACING

The effective gain of the ADL5562 can be reduced using a number of techniques. A matched attenuator network can reduce the effective gain, but this requires the addition of a separate component that can be prohibitive in size and cost. Instead, a simple voltage divider can be implemented using the combination of additional series resistors at the amplifier input and the input impedance of the ADL5562, as shown in Figure 36. A shunt resistor is used to match to the impedance of the previous stage.

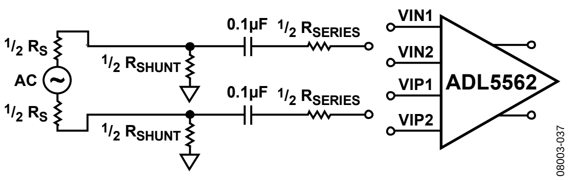


Figure 36. Gain Adjustment Using a Series Resistor

Figure 36 shows a typical implementation of the divider concept that effectively reduces the gain by adding attenuation at the input. For frequencies less than 100 MHz, the input impedance of the ADL5562 can be modeled as a real 133 Ω, 200 Ω, or 400 Ω resistance (differential) for maximum, middle, and minimum gains, respectively. Assuming that the frequency is low enough to ignore the shunt reactance of the input and high enough so that the reactance of moderately sized ac-coupling capacitors can be considered negligible, the insertion loss, Il, due to the shunt divider can be expressed as

$$Il(dB) = 20\log\left(\frac{R_{IN}}{R_{SERIES} + R_{IN}}\right) \quad (3)$$

The necessary shunt component, R_{SHUNT}, to match to the source impedance, R_S, can be expressed as

$$R_{SHUNT} = \frac{1}{\frac{1}{R_s} - \frac{1}{R_{SERIES} + R_{IN}}} \quad (4)$$

The insertion loss and the resultant power gain for multiple shunt resistor values are summarized in Table 8. The source resistance and input impedance need careful attention when using Equations 3 and 4. The reactance of the input impedance of the ADL5562 and the ac-coupling capacitors must be considered before assuming that they make a negligible contribution.

Table 8. Gain Adjustment Using Series Resistor

Il (dB)	R_{IN} (Ω)	R_S (Ω)	R_{SERIES} (Ω)	R_{SHUNT} (Ω)
2	400	50	105	54.9
4	400	50	232	54.9
2	200	50	51.1	61.9
4	200	50	115	59
2	133	50	34.8	71.5
2	400	200	102	332
4	400	200	232	294
2	200	200	51.1	976
4	200	200	115	549
2	400	50	105	54.9
4	400	50	232	54.9
2	200	50	51.1	61.9

ADC INTERFACING

The ADL5562 is a high output linearity amplifier that is optimized for ADC interfacing. There are several options available to the designer when using the ADL5562. Figure 37 shows a simplified wideband interface with the ADL5562 driving a AD9445. The AD9445 is a 14-bit, 125 MSPS ADC with a buffered wideband input.

For optimum performance, the ADL5562 should be driven differentially using an input balun. Figure 37 uses a wideband 1:1 transmission line balun followed by two 34.8 Ω resistors in parallel with the three input impedances, which change with the gain selection of the AD5562, to provide a 50 Ω differential input impedance. This provides a wideband match to a 50 Ω source. The ADL5562 is ac coupled from the AD9445 to avoid common-mode dc loading. The 33 Ω series resistors help to improve the isolation between the ADL5562 and any switching currents present at the analog-to-digital sample and hold input circuitry. The AD9445 input presents a 2 kΩ differential load impedance and requires a 2 V p-p differential input swing to reach full scale (VREF = 1 V).

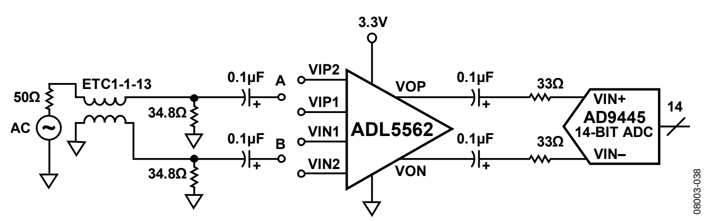


Figure 37. Wideband ADC Interfacing Example Featuring the AD9445

This circuit provides variable gain, isolation, and source matching for the AD9445. Using this circuit with the ADL5562 in a gain of 6 dB, an SFDR performance of 87 dBc is achieved at 140 MHz and a −3 dB bandwidth of 760 MHz, as indicated in Figure 38 and Figure 39.

The wideband frequency response is an advantage in broadband applications such as predistortion receiver designs and instrumentation applications. However, by designing for a wide analog input frequency range, the cascaded SNR performance is somewhat degraded due to high frequency noise aliasing into the wanted Nyquist zone.

An alternative narrow-band approach is presented in Figure 40. By designing a narrow band-pass antialiasing filter between the ADL5562 and the target ADC, the output noise of the ADL5562 outside of the intended Nyquist zone can be attenuated, helping to preserve the available SNR of the ADC. In general, the SNR improves several decibels when including a reasonable order antialiasing filter. In this example, a low loss 1:1 input transformer is used to match the ADL5562 balanced input to a 50 Ω unbalanced source, resulting in minimum insertion loss at the input.

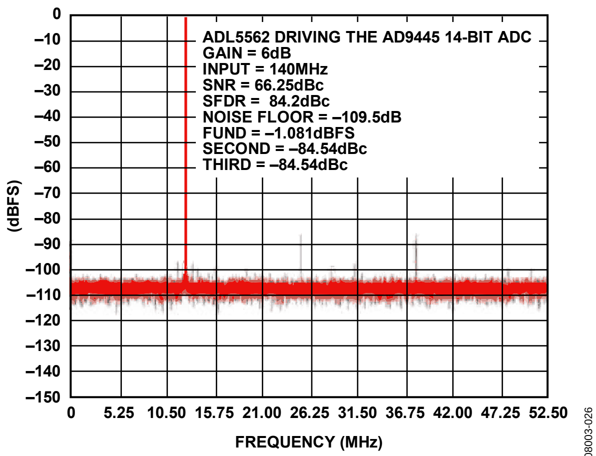


Figure 38. Measured Single-Tone Performance of the Circuit in Figure 37 for a 100 MHz Input Signal

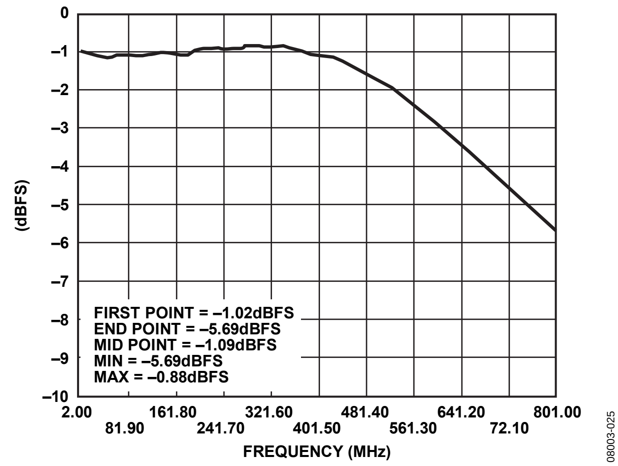


Figure 39. Measured Frequency Response of the Wideband ADC Interface Depicted in Figure 37

Figure 40 is optimized for driving some of the Analog Devices popular unbuffered ADCs, such as the AD9246, AD9640, and AD6655. Table 9 includes antialiasing filter component recommendations for popular IF sampling center frequencies. Inductor L5 works in parallel with the on-chip ADC input capacitance and a portion of the capacitance presented by C4 to form a resonant tank circuit. The resonant tank helps to ensure that the ADC input looks like a real resistance at the target center frequency. The L5 inductor shorts the ADC inputs at dc, which introduces a zero into the transfer function. In addition, the ac-coupling capacitors introduce additional zeros into the transfer function. The final overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. Table 9 provides initial suggestions for prototyping purposes. Some empirical optimization may be needed to help compensate for actual PCB parasitics.

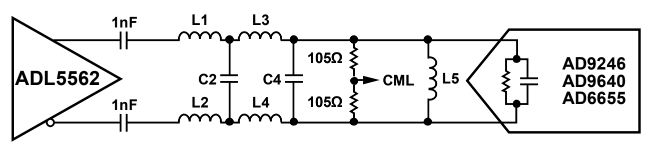


Figure 40. Narrow-Band IF Sampling Solution for an Unbuffered ADC Application

Table 9. Interface Filter Recommendations for Various IF Sampling Frequencies

Center Frequency	1 dB Bandwidth	L1	C2	L3	C4	L5
96 MHz	28 MHz	5.1 nH	56 pF	18 nH	75 pF	250 nH
140 MHz	33 MHz	5.1 nH	43 pF	12 nH	68 pF	39 nH
170 MHz	32 MHz	2.2 nH	30 pF	10 nH	75 pF	22 nH
211 MHz	30 MHz	2.2 nH	16 pF	10 nH	51 pF	18 nH

LAYOUT CONSIDERATIONS

High Q inductive drives and loads, as well as stray transmission line capacitance in combination with package parasitics, can potentially form a resonant circuit at high frequencies, resulting in excessive gain peaking or possible oscillation. If RF transmission lines connecting the input or output are used, they should be designed such that stray capacitance at the input/output pins is minimized. In many board designs, the signal trace widths should be minimal where the driver/receiver is more than one-eighth of the wavelength from the amplifier. This nontransmission line configuration requires that underlying and adjacent ground and low impedance planes be dropped from the signal lines

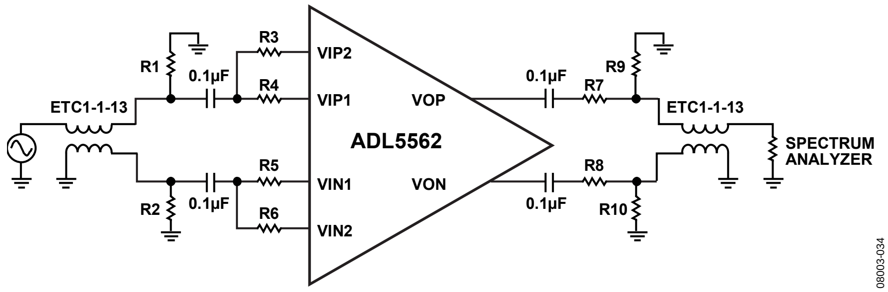


Figure 41. General Purpose Characterization Circuit

Table 10. Gain Setting and Input Termination Components for Figure 41

A_V	R1	R2	R3	R4	R5	R6
6 dB	29	29	Open	0	0	Open
12 dB	33	33	0	Open	Open	0
15.5 dB	40.2	40.2	0	0	0	0

Table 11. Output Matching Network for Figure 41

R_L	R7	R8	R9	R10
200	84.5	84.5	34.8	34.8
1 K	487	487	25	25

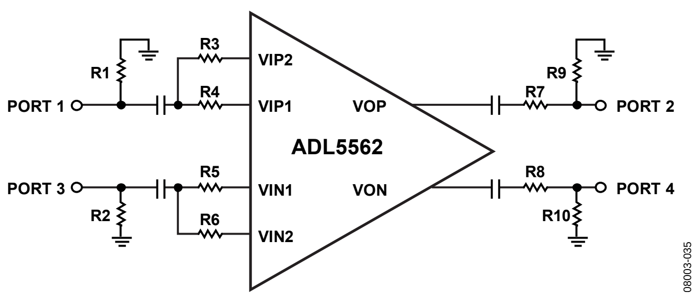


Figure 42. Differential Characterization Circuit Using Agilent E8357A 4-Port PNA

Table 12. Gain Setting and Input Termination Components for Figure 42

A_V	R1	R2	R3	R4	R5	R6
6 dB	67	67	Open	0	0	Open
12 dB	100	100	0	Open	Open	0
15.5 dB	200	200	0	0	0	0

Table 13. Output Matching Network for Figure 42

R_L	R7	R8	R9	R10
200	50	50	Open	Open
1 K	475	475	61.9	61.9

SOLDERING INFORMATION

On the underside of the chip scale package, there is an exposed compressed paddle. This paddle is internally connected to the ground of the chip. Solder the paddle to the low impedance ground plane on the PCB to ensure the specified electrical performance and to provide thermal relief. To further reduce thermal impedance, it is recommended that the ground planes on all layers under the paddle be stitched together with vias.

EVALUATION BOARD

Figure 43 shows the schematic of the ADL5562 evaluation board. The board is powered by a single supply in the 3.0 V to 3.6 V range. The power supply is decoupled by 10 µF and 0.1 µF capacitors.

Table 14 details the various configuration options of the evaluation board. Figure 44 and Figure 45 show the component and circuit layouts of the evaluation board.

To realize the minimum gain (6 dB into a 200 Ω load), Input 1 (VIN1 and VIP1) must be used by installing 0 Ω resistors at R3 and R4, leaving R5 and R6 open. R1 and R2 must be 33 Ω for a 50 Ω input impedance.

Likewise, driving Input 2 (VIN2 and VIP2) realizes the middle gain (12 dB into a 200 Ω load) by installing 0 Ω at R5 and R6 and leaving R3 and R4 open. R1 and R2 must be 29 Ω for a 50 Ω input impedance.

For the maximum gain (15.5 dB into a 200 Ω load), both inputs are driven by installing 0 Ω resistors at R3, R4, R5, and R6. R1 and R2 must be 40.2 Ω for a 50 Ω input impedance.

Both the input and output are converted to single-ended with a pair of baluns (M/A-COM ETC1-1-13). The balun at the input, T1, provides a 50 Ω single-ended to differential transformation. The output balun, T2, and the matching components are configured to provide a 200 Ω to 50 Ω impedance transformation with an insertion loss of about 17 dB.

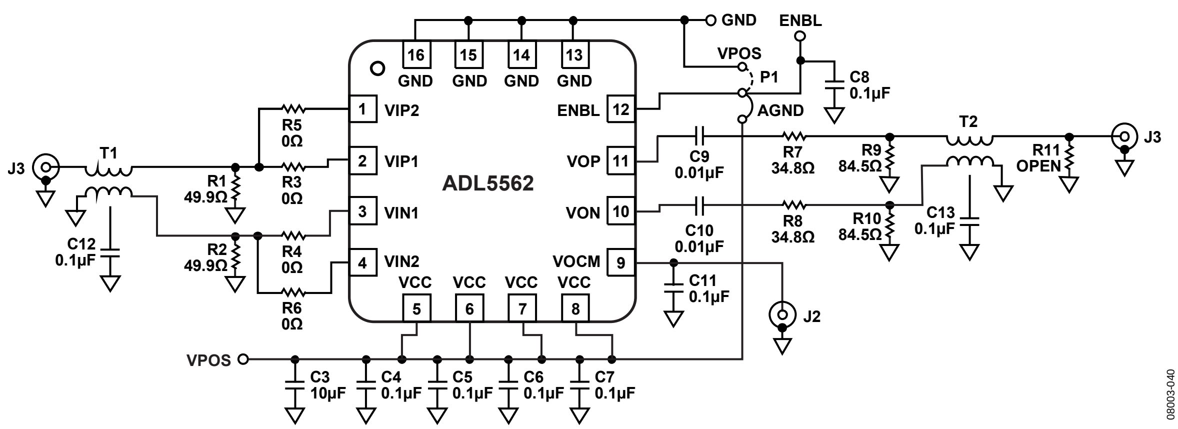


Figure 43. Evaluation Board Schematic

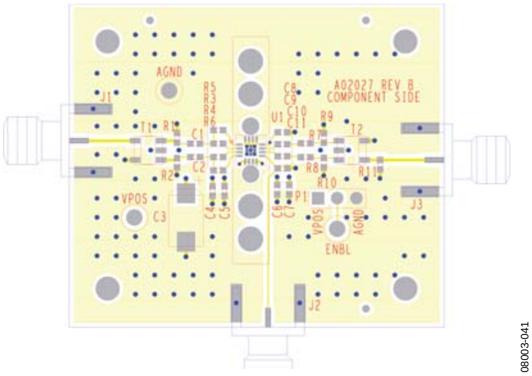


Figure 44. Layout of Evaluation Board, Component Side

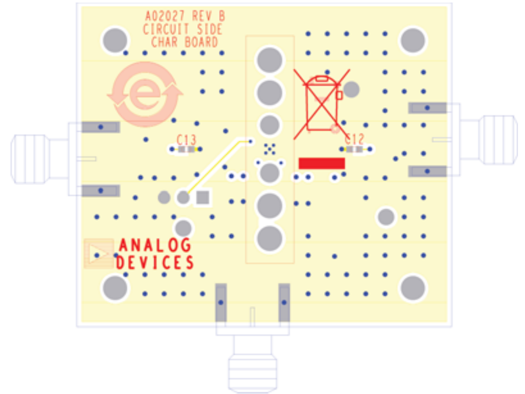


Figure 45. Layout of Evaluation Board, Circuit Side

Table 14. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Ground and supply vector pins.	VPOS, GND = installed
C3, C4, C5, C6, C7, C11	Power supply decoupling. The supply decoupling consists of a 10 μF capacitor (C3) to ground. C4 to C7 are bypass capacitors.	C3 = 10 μF (Size D) C4, C5, C6, C7, Cll = 0.1 μF (Size 0402)
J1, R1, R2, R3, R4, R5, R6, C1, C2, C12	Input interface. The SMA labeled J1 is the input. T1 is a 1-to-1 impedance ratio balun to transform a single-ended input into a balanced differential signal. C1 and C2 provide ac-coupling. C12 is a bypass capacitor. R1 and R2 provide a differential 50 Ω input termination. R3 to R6 are used to select the input for the pin-strappable gain. Maximum gain: R3, R4, R5, R6 = 0 Ω; R1, R2 = 40.2 Ω Middle gain: R5, R6 = 0 Ω; R3, R4 = open; R1, R2 = 33 Ω Minimum gain: R3, R4 = 0 Ω; R5, R6 = open; R1, R2 = 29 Ω	J1 = installed R1, R2 = 40.2 Ω (Size 0402) R3, R4, R5, R6 = 0 Ω (Size 0402) C1, C2 = 0.01 μF (Size 0402) C12 = 0.1 μF (Size 0402)
J3, R7, R8, R9, R10, R11, C9, C10, C13	Output interface. The SMA labeled J3 is the output. T2 is a 1-to-1 impedance ratio balun to transform a balanced differential signal to a single-ended signal. C13 is a bypass capacitor. R7, R8, R9, and R10 are provided for generic placement of matching components. The evaluation board is configured to provide a 200 Ω to 50 Ω impedance transformation with an insertion loss of 17 dB. C9 and C10 provide ac-coupling.	J3 = installed R7, R8 = 84.5 Ω (Size 0402) R9, R10 = 34.8 Ω (Size 0402) R11 = open (Size 0402) C9, C10 = 0.01 μF (Size 0402) C13 = 0.1 μF (Size 0402)
ENBL, P1, C8	Device enable. C8 is a bypass capacitor. When the P1 jumper is set toward the VPOS label, the ENBL pin is connected to the supply, enabling the device. In the opposite direction, toward the GND label, the ENBL pin is grounded, putting the device in power-down mode.	ENBL, P1= installed C8 = 0.1 μF (Size 0402)

OUTLINE DIMENSIONS

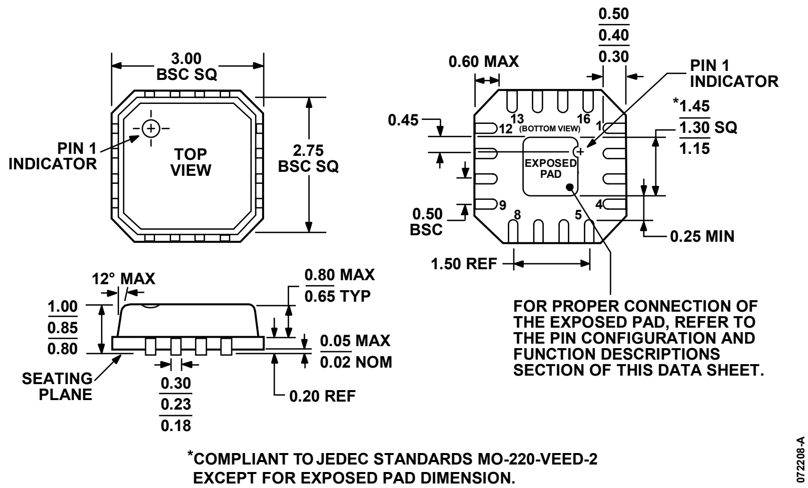


Figure 46. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5562ACPZ-R7[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7" Reel	CP-16-2	Q1Q	1,500
ADL5562ACPZ-WP[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ], Waffle Pack	CP-16-2	Q1Q	64
ADL5562-EVALZ[1]		Evaluation Board			

[1] Z = RoHS Compliant Part.

NOTES

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