900MHz Balanced Mixer with High Side LO Buffer, and RF Balun

Preliminary Technical Data

ADL5367

FEATURES

Power Conversion Loss of 7.0dB
RF Frequency 500MHz to 1500MHz
IF Frequency DC to 450 MHz
SSB Noise Figure with 10dBm Blocker of 17dB
Input IP3 of 37dBm
Input P_{1dB} of 25 dBm
Typical LO Drive of 0 dBm
Single-ended, 50Ω RF and LO Input Ports
High Isolation SPDT LO Input Switch
Single Supply Operation: 3.3 to 5 V
Exposed Paddle 5 x 5 mm, 20 Lead LFCSP Package
2000V HBM / 500V FICDM ESD Performance

APPLICATIONS

Cellular Base Station Receivers
Transmit Observation Receivers
Radio Link Downconverters

GENERAL DESCRIPTION

The ADL5367 utilizes a highly linear doubly balanced passive mixer core along with integrated RF and LO balancing circuitry to allow for single-ended operation. The ADL5367 incorporates an RF balun allowing for optimal performance over a 700 to 1000 MHz RF input frequency range using high-side LO injection. (Pin compatible parts for low side injection are also available). The balanced passive mixer arrangement provides good LO to RF leakage, typically better than -20dBm, and excellent intermodulation performance. The balanced mixer core also provides extremely high input linearity allowing the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in the degradation of dynamic performance. For low voltage applications, the ADL5367 is capable of operation at voltages down to 3V with substantially reduced current.

Two digital logic inputs allowed the user to control an internal resistor string D/A converter to optimize the intermodulation or noise performance of the application. LO current can be

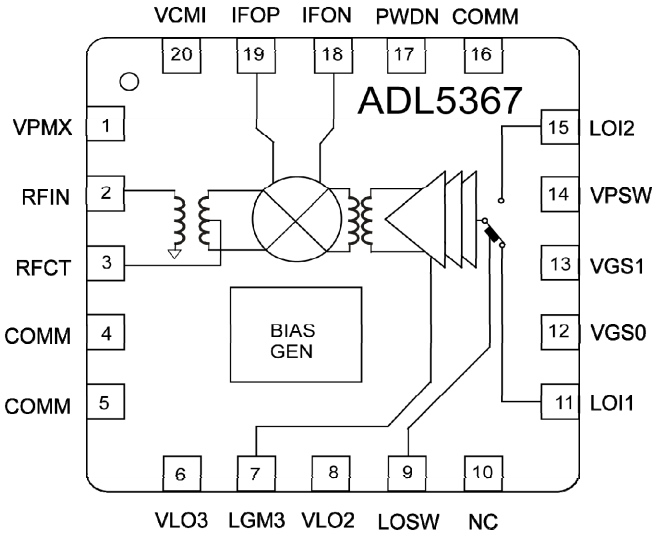

Figure 1. Functional Block Diagram

externally set using a resistor to minimize DC current commensurate with the desired level of performance. An additional logic pin is provided to power down (<100uA) the circuit when desired.

The ADL5367 is fabricated using a BiCMOS high performance IC process. The device is available in a 5mm x 5mm 20-lead LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

RF Frequency	Single Mixer	Single Mixer + IF Amp	Dual Mixer + IF Amp
500MHz to 1500MHz	ADL5367	ADL5357	ADL5358
1500MHz to 2500MHz	ADL5365	ADL5355	ADL5356

REV. PrB

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ADL5367—Specifications

Table 1. V_S = 5 V, T_A = 25°C, f_{RF} = 900 MHz, f_{LO} = 1103 MHz, LO power = 0 dBm, Zo = 50Ω, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20dB over a limited bandwidth		16		dB
Input Impedance			50		Ω
RF Frequency Range		500		1500	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		50		Ω
IF Frequency Range		DC		450	MHz
LO INTERFACE					
LO Power		-3	0	+10	dBm
Return Loss			10		dB
Input Impedance			50		Ω
LO Frequency Range	High Side LO	700		1700	MHz
DYNAMIC PERFORMANCE					
Power Conversion Gain	Including 1:1 IF port transformer and PCB loss		-7.0		dB
Voltage Conversion Gain	Z_{SOURCE} = 50Ω, Differential Z_{LOAD} = 50Ω Differential		-7.0		dB
SSB Noise Figure			7.4		dB
SSB Noise Figure Under-Blocking	10dBm Blocker present +/-5MHz from wanted RF input, LO source filtered		17		dB
Input Third Order Intercept	f_{RF1} = 900 MHz, f_{RF2} = 901 MHz, f_{LO} = 1103 MHz, each RF tone at 0 dBm		37		dBm
Input Second Order Intercept	f_{RF1} = 900 MHz, f_{RF2} = 950 MHz, f_{LO} = 1103 MHz, each RF tone at 0 dBm		63		dBm
Input 1 dB Compression Point			25		dBm
LO to IF Output Leakage	Unfiltered IF Output		-13		dBm
LO to RF Input Leakage			-28		dBm
RF to IF Output Isolation			42		dB
IF/2 Spurious	0 dBm Input Power		-66		dBc
IF/3 Spurious	0dBm Input Power		-72		dBc
POWER INTERFACE					
Supply Voltage		3	5	5.5	V
Quiescent Current	Resistor Programmable		100		mA

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ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
PWDN, LOSW, VGS0, VGS1	TBD
RF Input Power RFIN	TBD
Internal Power Dissipation	TBD
θ_{JA} (Exposed Paddle Soldered Down)	TBD
θ_{JC} (At Exposed Paddle)	TBD
Maximum Junction Temperature	TBD
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

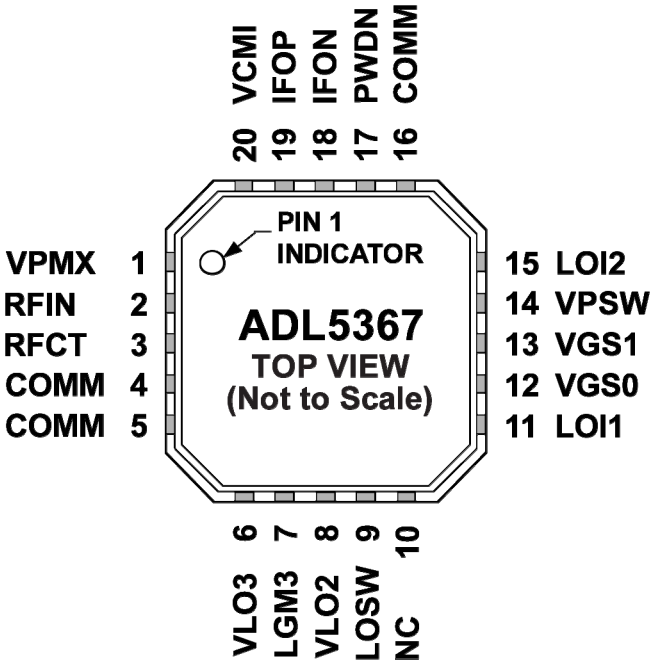

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VPMX	Positive Supply Voltage for the mixer: 5.00 V.
2	RFIN	RF Input. Must be ac-coupled.
3	RFCT	RF Balun Center Tap (AC Ground).
4, 5, 16	COMM	Device Common (DC Ground).
6, 8	VLO3, VLO2	Positive Supply Voltage for LO Amplifier.
7	LGM3	LO Amplifier Bias Control.
9	LOSW	LO Switch.
10	NC	No Connect.
11, 15	LOI1, LOI2	LO Input. Must be ac-coupled.
12, 13	VGS0, VGS1	Mixer Gate Bias Control. Ground for nominal operation.
14	VPSW	Positive Supply Voltage for LO Switch.
17	PWDN	Connect to Ground for Normal Operation. Connect pin to 3.3V for disable mode.
18, 19	IFON, IFOP	Differential IF Output.
20	VCMI	No Connect.

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TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, as measured using typical circuit schematic with high-side LO unless otherwise noted.

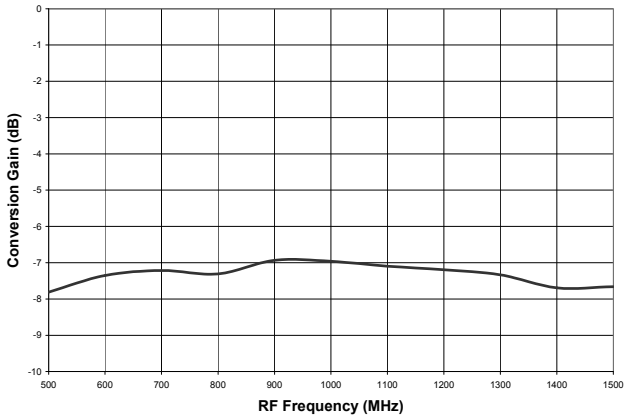

Figure 3. Conversion Gain versus RF Frequency

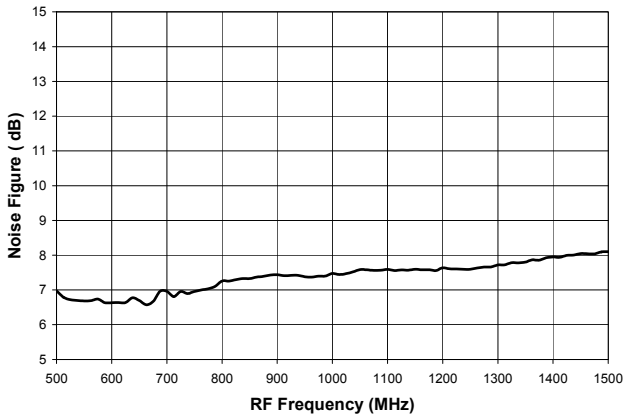

Figure 6. Single-Sideband NF versus RF Frequency

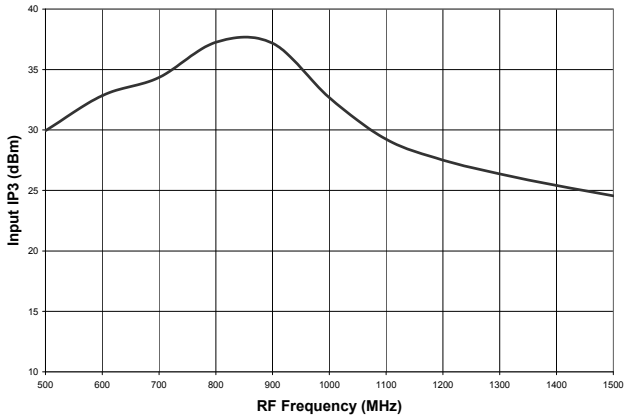

Figure 4. IIP3 versus RF Frequency

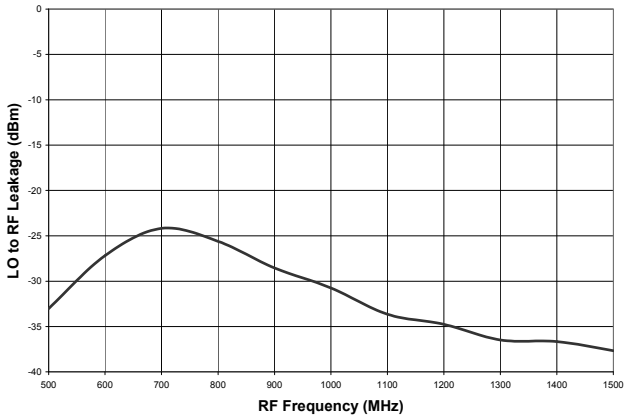

Figure 8. LO to RF Leakage versus LO Frequency

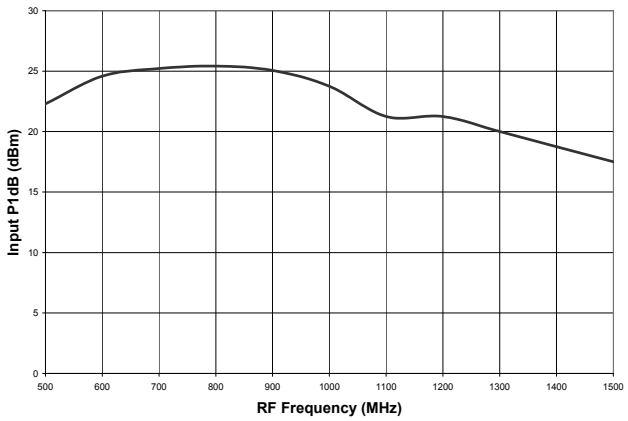

Figure 5. IP1dB versus RF Frequency

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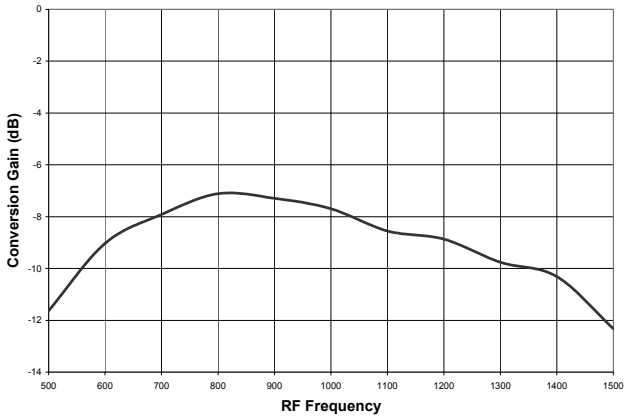

Figure 8. Up Conversion: Conversion Gain vs. RF frequency

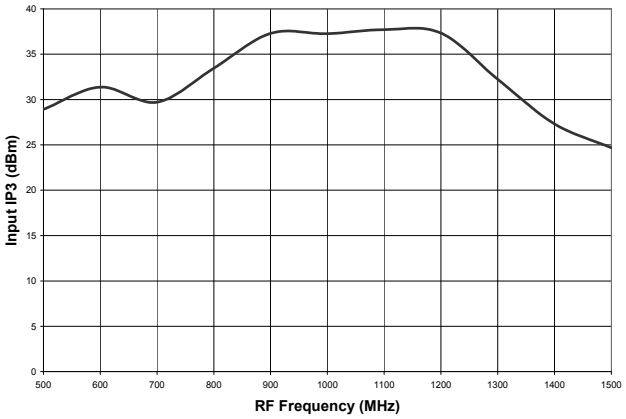

Figure 9. Up Conversion: Input IP3 vs. RF Frequency

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EVALUATION BOARD

An evaluation board is available for the family of double balanced mixers, including ADL5365 and ADL5367. The standard evaluation board schematic is presented in Figure 10. The evaluation board is fabricated on a multilayer Rogers board. Table 4 details the various configuration options of the evaluation board.

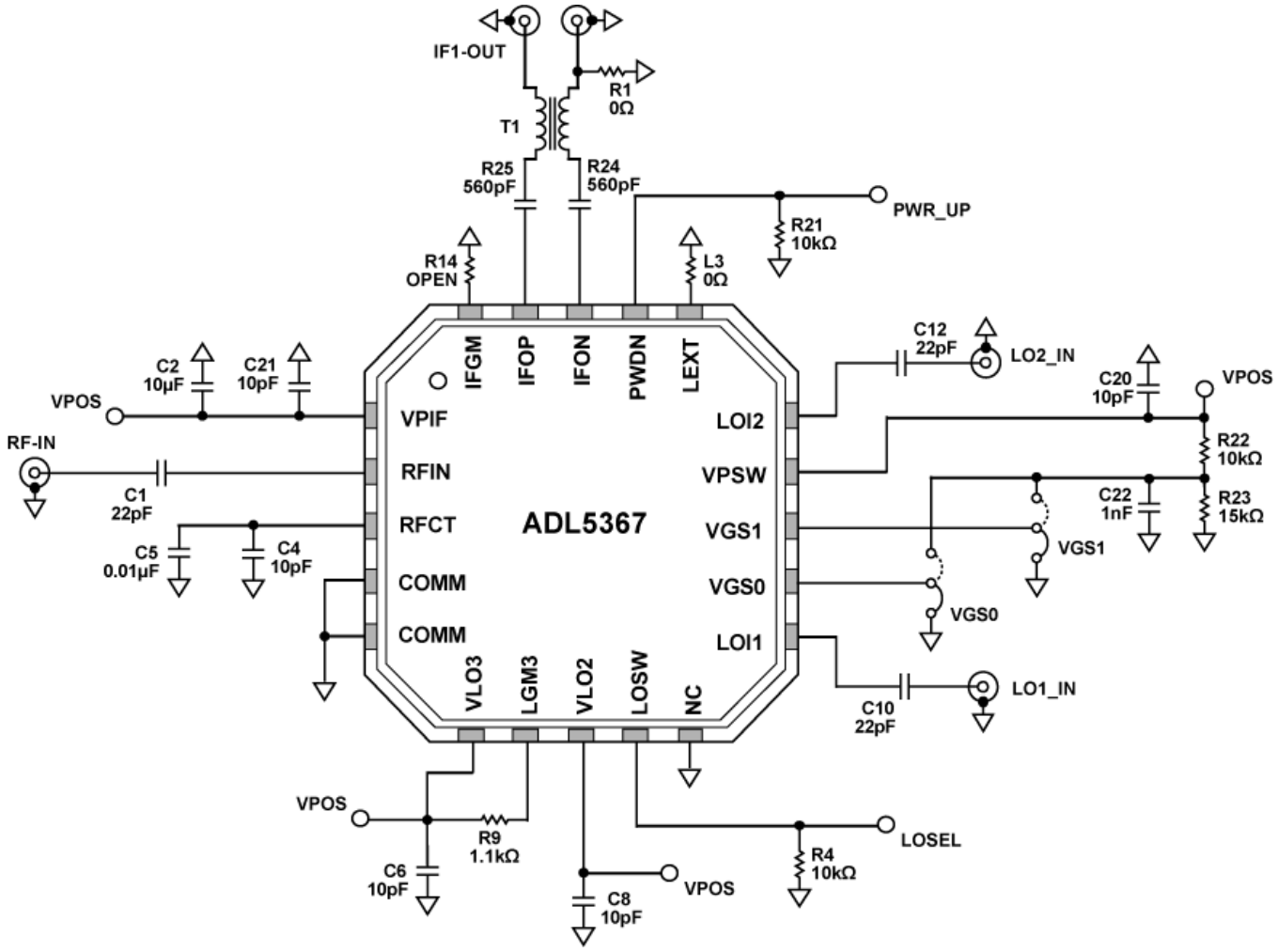

Figure 10. Evaluation Board Schematic.

Table 4. Eval Board Configuration

Components	Function	Default Conditions
C2, C6, C8, C20, C21	Power Supply Decoupling. Nominal supply decoupling consists a 10µF capacitor to ground in parallel with 10pF capacitors to ground positioned as close to the device as possible.	C2 = 10 µF (size 0603) C6, C8, C20, C21 = 10 pF (size 0402)
C1, C4, C5	RF Input Interface. The input channels is ac-coupled through C1. C4 and C5 provide bypassing for the center taps of the RF input baluns.	C1 = 22 pF (size 0402) C4 = 10 pF (size 0402) C5 = 0.01 µF (size 0402)
T1, R1, R24, R25	IF Output Interface. T1is a 1:1 impedance transformer used to provide a single ended IF output interface. R1 should be removed for balanced output operation.	T1 = TC1-1-13M+ (MiniCircuits) R1 = 0 Ω (size 0402) R24, R25 = 560 pF (size 0402)

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C10, C12, R4	LO Interface. C10 and C12 provide ac-coupling for the LO1_IN and LO2_IN local oscillator inputs. LOSEL selects the appropriate LO input for both mixer cores. R4 provides a pull-down to ensure LO1_IN is enabled when the LOSEL test point has logic low. LO2_IN is enabled when LOSEL is pulled to logic high.	C10, C12 = 22pF (size 0402) R4 = 10kΩ (size 0402)
R21	PWDN Interface. R21 pulls the PWDN logic low and enables the device. PWR_UP test point allows PWDN interface to be excercised using external logic generator. It is permissible to ground the PWDN pin for nominal operation.	R21 = 10kΩ (size 0402)
C22, L3, R9, R14, R22, R23, VGS0, VGS1	Bias Control. R22 and R23 form a voltage divider to provide a 3V for logic control, bypassed to ground through C22. VGS0 and VGS1 jumpers provide programmability at pin VGS0 and VGS1. It is recommeded to pull these two pins to ground for nominal operation. R9 sets the bias point for the internal LO buffers. R14 is essentially no connect.	C22 = 1 nF (size 0402) L3 = 0 Ω (size 0603) R9 = 1.1 kΩ (size 0402) R14 = OPEN R22 = 10kΩ (size 0402) R23 = 15kΩ (size 0402) VGS0 = VGS1 = 3-pin shunt

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OUTLINE DIMENSIONS

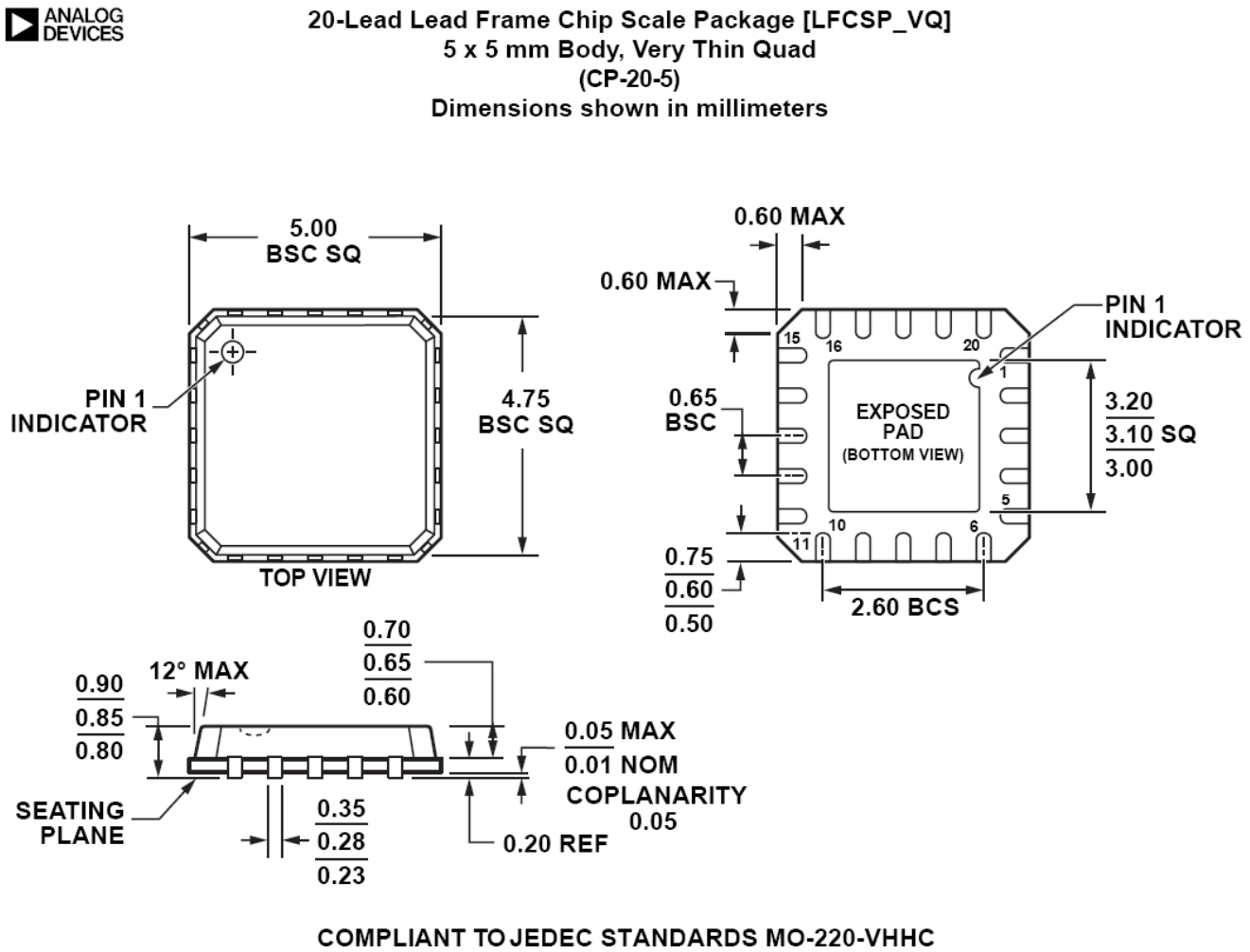

Figure 11. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad (CP-20-5)
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option	Branding	Transport Media Quantity
ADL5367XCPZ-R7[1]	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-5	TBD	TBD, Reel
ADL5367-EVALZ		Evaluation Board			1

[1] *Z = Pb-free part.*

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