400 MHz to 6 GHz Broadband Quadrature Modulator

Preliminary Technical Data

ADL5375

FEATURES

Output frequency range: 400 MHz to 6 GHz
Modulation bandwidth: 500 MHz (3 dB)
1 dB output compression: ≥ 9.4 dBm from 500 MHz to 4 GHz
Output return loss: ≤ 15 dB from 500 MHz to 5 GHz
Noise floor: −161 dBm/Hz @ 900 MHz
SB suppression: ≤ −40 dBc, 450 MHz to 4 GHz and vs. temp
LO leakage: ≤ −40 dBm, 450 MHz to 2 GHz and vs. temp
Baseband bias levels of 500 mV and 1.5 V
Single supply: 4.75 V to 5.25 V
24-lead LFCSP_VQ package

APPLICATIONS

Cellular communications systems
GSM/EDGE, CDMA2000, WCDMA, TDSCDMA
WiMAX/broadband wireless access systems
Multi-band, Multi-standard radios
Satellite modems

GENERAL DESCRIPTION

The ADL5375 is a broadband quadrature modulator designed for operation from 400 MHz to 6 GHz. Its excellent phase accuracy and amplitude balance enable high performance intermediate frequency or direct radio frequency modulation for communications systems.

The ADL5375 provides a greater than 500 MHz, 3 dB baseband bandwidth, making it ideally suited for use in broadband zero IF or low IF-to-RF applications and in broadband digital predistortion transmitters. In addition, the ADL5375 offers output gain flatness of ±0.5 dB from 450 MHz to 3 GHz and a broadband output return loss of less than −15 dB.

The ADL5375 accepts two differential baseband inputs and a single-ended LO and generates a single-ended 50 Ω output. Two versions offer input baseband bias levels of 500 mV (ADL5375-05) and 1.5 V (ADL5375-15).

The ADL5375 is fabricated using an advanced silicon-germanium bipolar process. It is available in a 24-lead, exposed-paddle, Pb-free, LFCSP_VQ package. Performance is specified over a −40°C to +85°C temperature range. A Pb-free evaluation board is available.

FUNCTIONAL BLOCK DIAGRAM

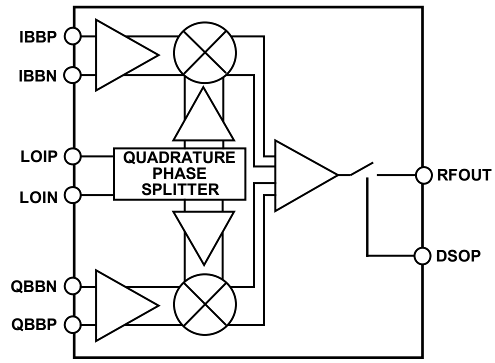

Figure 1.

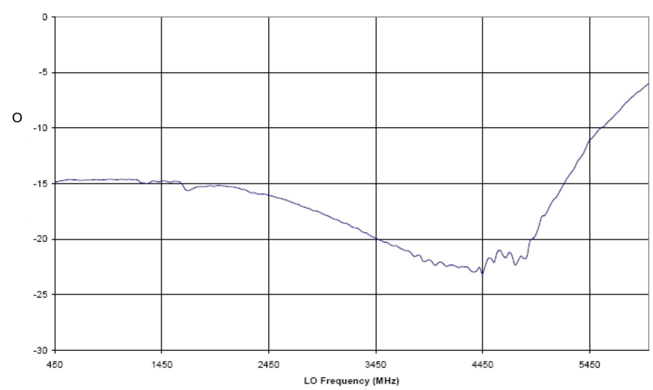

Figure 2. Typical RF Output Return Loss

Rev. PrE

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REVISION HISTORY

12/07—Revision PrE

SPECIFICATIONS

V_S = 5 V; T_A = 25°C; LO = 0 dBm single-ended; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 500 mV (ADL5375-05) or 1.5 V (ADL5375-15) dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OPERATING FREQUENCY RANGE	Low frequency		400		
	High frequency		6000		MHz
OUTPUT FREQUENCY = 900 MHz					
Output Power	V_{IQ} = 1 V p-p differential		1		dBm
Output P1 dB			9.4		dBm
Output Return Loss			−15		
Carrier Leakage			−46		dBm
Sideband Suppression			−52		dBc
Second Harmonic	P_{OUT} − (f_{LO} + (2 × f_{BB})), P_{OUT} = 1 dBm		−72		dBc
Third Harmonic	P_{OUT} − (f_{LO} + (3 × f_{BB})), P_{OUT} = 1 dBm		−52		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		66		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		26		dBm
Noise Floor	I/Q inputs = 0 V differential with a 500 mV common-mode bias, 20 MHz LO offset		−161		dBm/Hz
GSM	6 MHz carrier offset, P_{OUT} = 4 dBm, P_{LO} = 0 dBm		−158		dBc/Hz
OUTPUT FREQUENCY = 1900 MHz					
Output Power	V_{IQ} = 1 V p-p differential		1		dBm
Output P1 dB			9.8		dBm
Output Return Loss			−15		dB
Carrier Leakage			−41		dBm
Sideband Suppression			−55		dBc
Second Harmonic	P_{OUT} − (f_{LO} + (2 × f_{BB})), P_{OUT} = 1 dBm		−67		dBc
Third Harmonic	P_{OUT} − (f_{LO} + (3 × f_{BB})), P_{OUT} = 1 dBm		−52		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		62		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		24		dBm
Noise Floor	I/Q inputs = 0 V differential with a 500 mV or 1.5 V common-mode bias, 20 MHz LO offset		−161		dBm/Hz
OUTPUT FREQUENCY = 2140 MHz					
Output Power	V_{IQ} = 1 V p-p differential		1		dBm
Output P1 dB			10		dBm
Output Return Loss			−16		dB
Carrier Leakage			−40		dBm
Sideband Suppression			−45		dBc
Second Harmonic	P_{OUT} − (f_{LO} + (2 × f_{BB})), P_{OUT} = 1 dBm		−68		dBc
Third Harmonic	P_{OUT} − (f_{LO} + (3 × f_{BB})), P_{OUT} = 1dBm		−53		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		57		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		24		dBm
Noise Floor	I/Q inputs = 0 V differential with a 500 mV or 1.5 V common-mode bias, 20 MHz LO offset		−160		dBm/Hz

Parameter	Conditions	Min	Typ	Max	Unit
OUTPUT FREQUENCY = 2600 MHz					
Output Power	V_{IQ} = 1 V p-p differential		1.1		dBm
Output P1 dB			10.3		dBm
Output Return Loss			−17		dB
Carrier Leakage			−40		dBm
Sideband Suppression			−44		dBc
Second Harmonic	P_{OUT} − (f_{LO} + (2 × f_{BB})), P_{OUT} = 1 dBm		−58		dBc
Third Harmonic	P_{OUT} − (f_{LO} + (3 × f_{BB})), P_{OUT} = 1 dBm		−52		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		56		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		23		dBm
Noise Floor	I/Q inputs = 0 V differential with a 500 mV common-mode bias, 20 MHz LO offset		−158		dBm/Hz
OUTPUT FREQUENCY = 3.5 GHz					
Output Power	V_{IQ} = 1 V p-p differential		1.7		dBm
Output P1 dB			10.4		dBm
Output Return Loss			−20		dB
Carrier Leakage			−31		dBm
Sideband Suppression			−50		dBc
Second Harmonic	P_{OUT} − (f_{LO} + (2 × f_{BB})), P_{OUT} = 1 dBm		−54		dBc
Third Harmonic	P_{OUT} − (f_{LO} + (3 × f_{BB})), P_{OUT} = 1 dBm		−52		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		50		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		24		dBm
Noise Floor	I/Q inputs = 0 V differential with a 500 mV common-mode bias, 20 MHz LO offset		−158		dBm/Hz
OUTPUT FREQUENCY = 5.8 GHz					
Output Power	V_{IQ} = 1 V p-p differential		2.5		dBm
Output P1 dB			7.3		dBm
Output Return Loss			−6		
Carrier Leakage			−18		dBm
Sideband Suppression			−30		dBc
Second Harmonic	P_{OUT} − (f_{LO} + (2 × f_{BB})), P_{OUT} = 0 dBm		−46		dBc
Third Harmonic	P_{OUT} − (f_{LO} + (3 × f_{BB})), P_{OUT} = 0 dBm		−43		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		37		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} = −8 dBm per tone		13		dBm
Noise Floor	I/Q inputs = 500 mV common-mode bias, 20 MHz LO offset		−152		dBm/Hz
OUTPUT DISABLE	Pin DSOP				
Off Isolation	LO = 0 dBm; measured at LO frequency				
	900 MHz		−83		dBm
	1900 MHz		−55		dBm
	3500 MHz		−42		dBm
DSOP High Level (Logic 1)	Logic high disables output	2.0			V
DSOP Low Level (Logic 0)	Logic low or floating enables output.			0.8	V
LO INPUTS					
LO Drive Level	Characterization performed at typical level		0		dBm
Input Return Loss	500 MHz to 3 GHz		−10		dB
BASEBAND INPUTS	Pin IBBP, Pin IBBN, Pin QBBP, Pin QBBN				
I and Q Input Bias Level	ADL5375-05		500		mV
	ADL5375-15		1.5		V
Bandwidth (3 dB)			500		MHz
POWER SUPPLIES	Pin VPS1 and Pin VPS2				
Voltage		4.75		5.25	V
Supply Current			190		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPOS	5.5 V
IBBP, IBBN, QBBP, QBBN	TBD V
LOIP and LOIN	13 dBm
Internal Power Dissipation	1375 mW
θ_{JA} (Exposed Paddle Soldered Down)	TBD°C/W
Maximum Junction Temperature	159°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

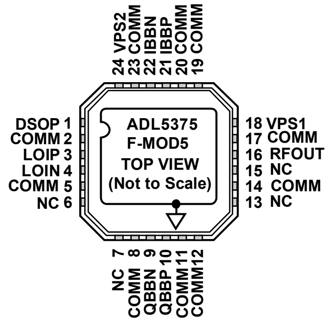


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DSOP	Output Disable. A logic high on this pin disables the RF output (Pin 16). Connecting this pin to ground or leaving it floating enable the RF output.
2, 5, 8, 11, 12, 14, 17, 19, 20, 23	COMM	Input Common Pins. Connect to ground plane via a low impedance path.
3, 4	LOIP, LOIN	Local Oscillator Input. 50 Ω single-ended local oscillator input. Internally dc-biased. Pins must be ac-coupled. AC-couple LOIN to ground and drive LO through LOIP.
6, 7, 13, 15,	NC	No Connect. These pins can be left open or tied to ground
9, 10, 21, 22	QBBN, QBBP, IBBP, IBBN,	Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs should be dc-biased to 500 mV (ADL5375-05) or 1.5 V (ADL5375-15). Nominal characterized ac signal swing is 500 mV p-p on each pin. This results in a differential drive of 1 V p-p with a 500 mV dc bias. These inputs are not self-biased and must be externally biased.
16	RFOUT	Device Output. Single-ended, 50 Ω internally biased RF output. AC-couple to the output load.
18, 24	VPS1, VPS2	Positive Supply Voltage Pins. All pins should be connected to the same supply (V_S). To ensure adequate external bypassing, connect 0.1 μF and 100 pF capacitors between each pin and ground.
	EP	Exposed Paddle. Connect to ground plan via a low impedance path.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V; T_A = 25°C; LO = 0 dBm single-ended; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 500 mV dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz, unless otherwise noted. Red = +85°C, Green = +25°C, Blue = −40°C.

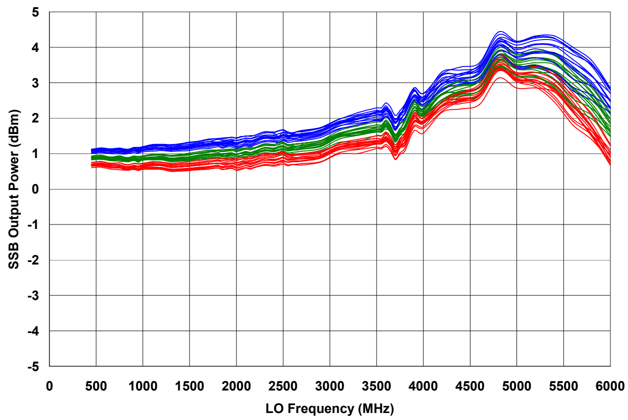


Figure 4. SSB Output Power vs. Frequency and Temperature, Baseband Drive = 1 V p-p Differential, Multiple Devices

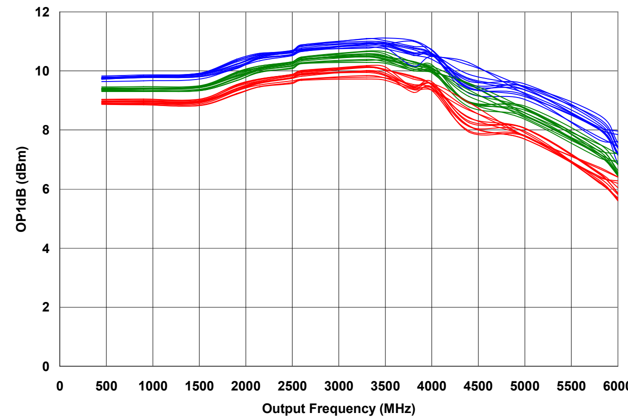


Figure 7. SSB Output 1 dB Compression Point (OP1dB) vs. Frequency and Temperature, Multiple Devices

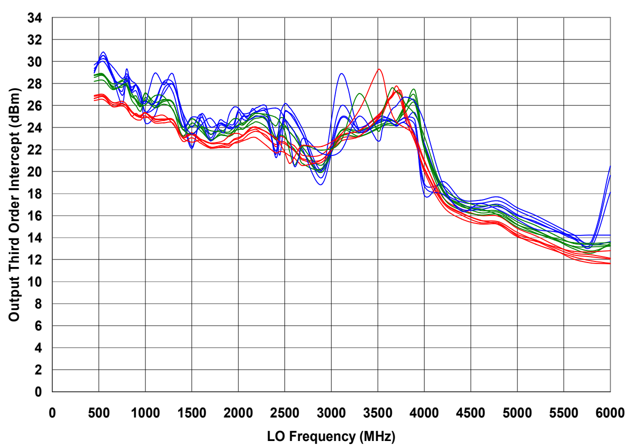


Figure 5. Third-Order Intercept (OIP3) vs. Frequency and Temperature, Multiple Devices

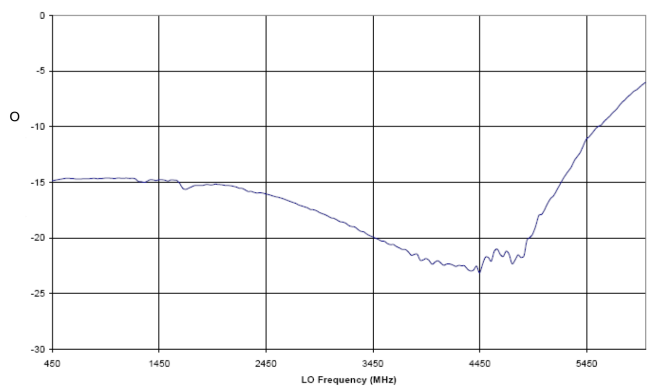


Figure 8. Typical RF Output Return Loss

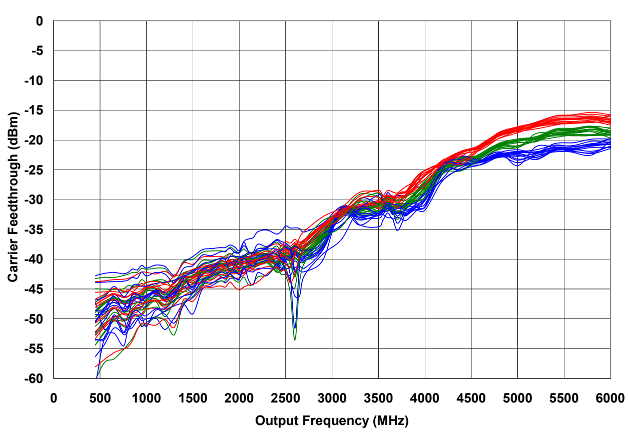


Figure 6. Carrier Leakage vs. Frequency and Temperature, Multiple Devices

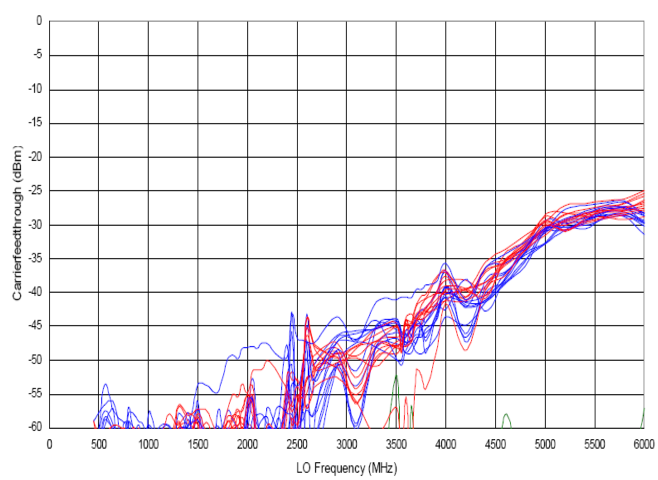


Figure 9. Carrier Leakage vs. Frequency and Temperature After Nulling at 25°C, Multiple Devices

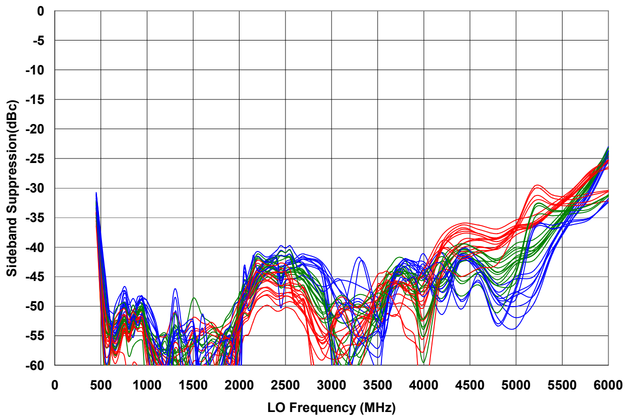


Figure 10. Sideband Suppression vs. Frequency and Temperature, Multiple Devices

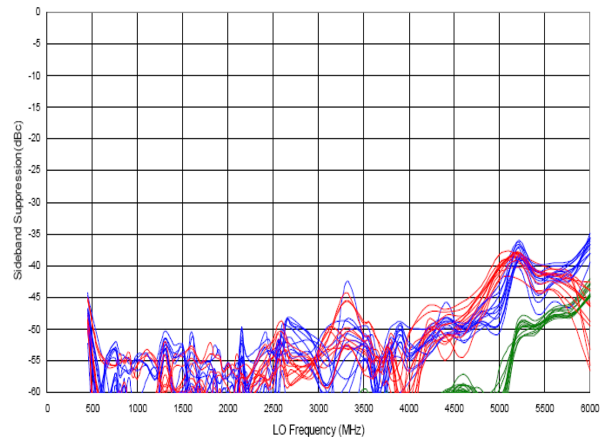


Figure 11. Sideband Suppression vs. Frequency and Temperature After Nulling at 25°C, Multiple Devices

EVALUATION BOARD

Populated RoHS-compliant evaluation boards are available for evaluation of both versions of the ADL5375. The ADL5375 package has an exposed paddle on the underside. This exposed paddle must be soldered to the board for good thermal and electrical grounding. The evaluation board is designed without any components on the underside, so heat can be applied to the underside for easy removal and replacement of the ADL5375 should it become necessary.

Both versions of the ADL5375 share the same evaluation board and schematic. To differentiate the boards from each other, the silkscreen on the underside of the board has a table that is marked to indicate which version (-05 or -15) is populated on the board.

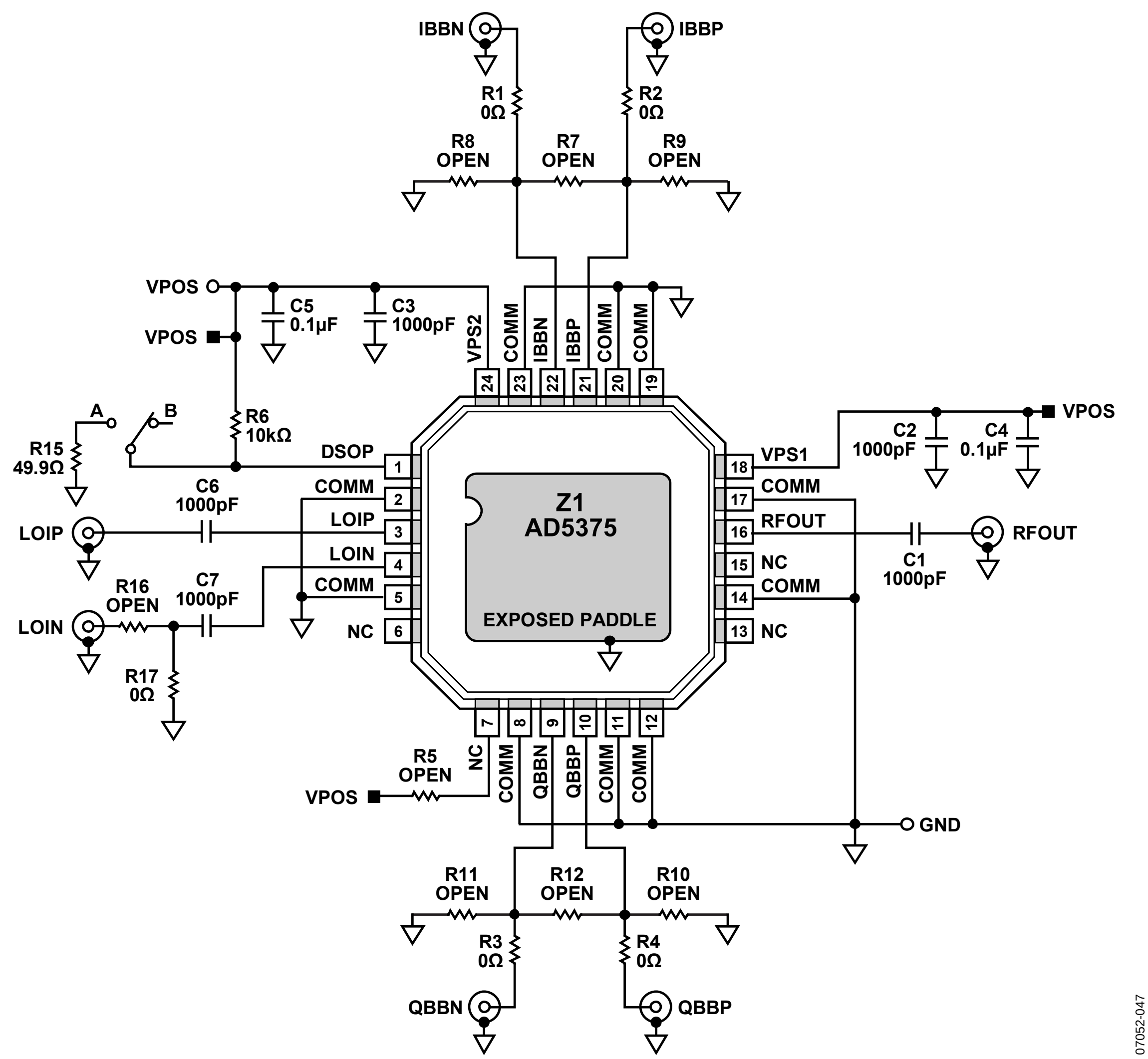


Figure 12. ADL5375 Evaluation Board Schematic

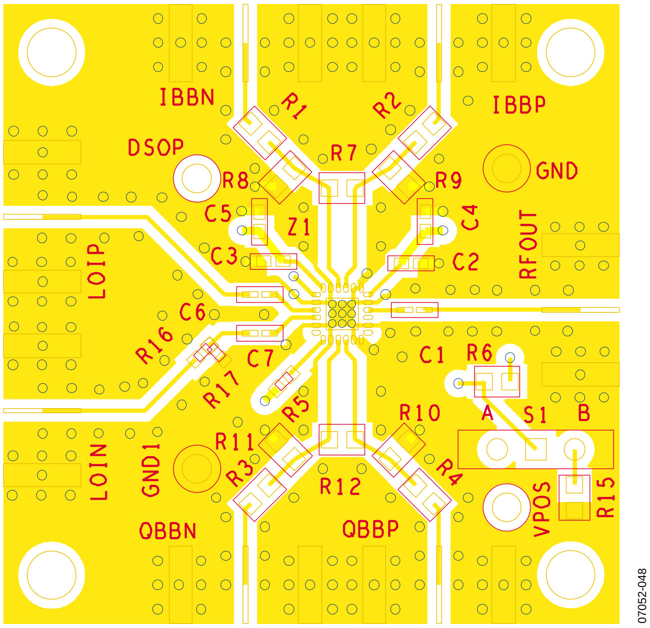


Figure 13. Evaluation Board Layout, Top Layer

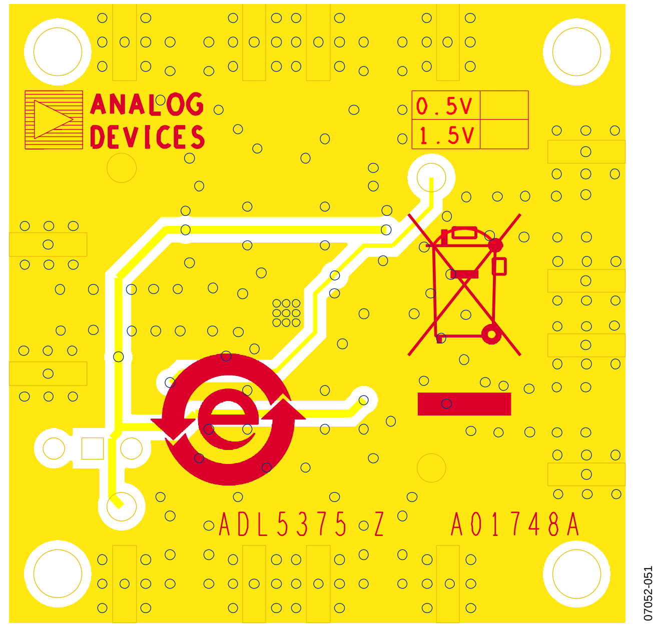
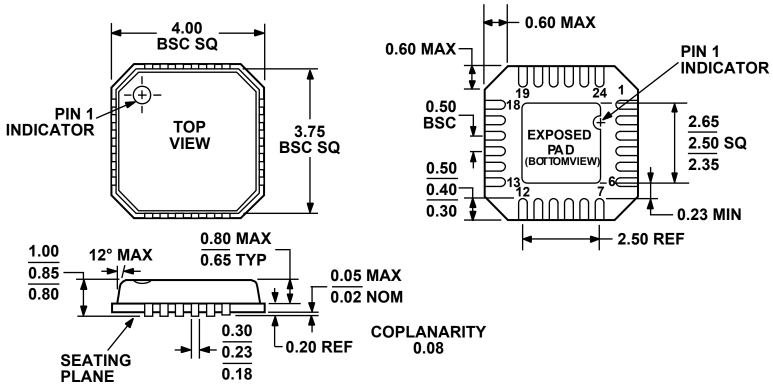


Figure 14. Evaluation Board Layout, Bottom Layer

Table 4. Evaluation Board Description and Configuration Options

Component	Description	Default Condition/Option Settings
VPOS, GND Test Points	Power supply and ground test points for clip leads.	Red = VPOS, black = GND
SW1 Switch	DSOP output disable select	Position A = output enabled Position B = output disabled
R1 thru R4, R7 thru R12	Optional baseband input filtering components	R1 through R4 = 0 Ω (0402) R7 through R12 = open (0402)
LOIP SMA, R16, R17	Single-ended local oscillator input	R16 = open, R17 = 0 Ω (0402)
LOIN SMA, R16, R17	Optional SMA for differential local oscillator input	R16 = 0 Ω (0402), R17 = open

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8

Figure 15. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range (°C)	Package Description	Package Option	Ordering Quantity
ADL5375ACPZ-05-R7[1,2]	–40°C to +85°C	24-Lead LFCSP_VQ, 7" Tape and Reel	CP-24-3	1,500
ADL5375ACPZ-15-R7[1,3]	–40°C to +85°C	24-Lead LFCSP_VQ, 7" Tape and Reel	CP-24-3	1,500
ADL5375ACPZ-05-WP[1,2]	–40°C to +85°C	24-Lead LFCSP_VQ, Waffle Pack	CP-24-3	64
ADL5375ACPZ-15-WP[1,3]	–40°C to +85°C	24-Lead LFCSP_VQ, Waffle Pack	CP-24-3	64
ADL5375-05-EVALZ[1]		Evaluation Board		
ADL5375-15-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] 500 mV baseband bias level.
[3] 1.5 V baseband bias level.

NOTES

PR07052-0-12/07(PrE)

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