# 1:3 and 1:4 Single-Ended, Low Cost, Active RF Splitters

# ADA4304-3/ADA4304-4

## FEATURES

- Ideal for CATV and terrestrial applications
- 2.4 GHz, −3 dB bandwidth
  - 1 dB flatness: 54 MHz to 865 MHz
- Low noise figure: 4.6 dB
- Low distortion
  - Composite second-order (CSO): −62 dBc
  - Composite triple beat (CTB): −72 dBc
- Nominal 3 dB gain per output channel
- 25 dB output-to-output isolation, 50 MHz to 1000 MHz
- 75 Ω input and outputs
- Small package size: 16-lead, 3 mm × 3 mm LFCSP

## APPLICATIONS

- Set-top boxes
- Residential gateways
- CATV distribution systems
- Splitter modules
- Digital cable ready (DCR) TVs

## FUNCTIONAL BLOCK DIAGRAMS

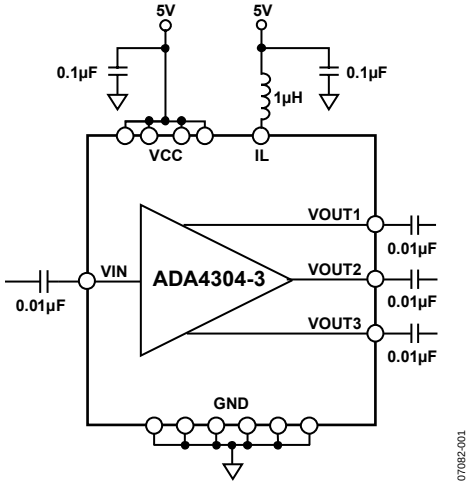


*Figure 1.*

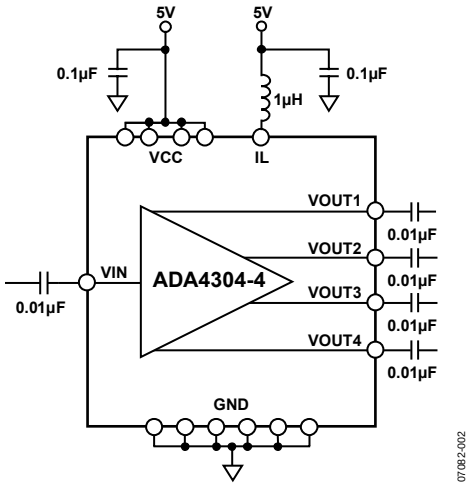


*Figure 2.*

## GENERAL DESCRIPTION

The ADA4304-3/ADA4304-4 are 75 Ω active splitters for use in applications where a lossless signal split is required. Typical applications include multituner digital set-top boxes, cable splitter modules, multituners/digital cable ready (DCR) televisions, and home gateways where traditional solutions require discrete passive splitter modules with separate fixed gain amplifiers.

The ADA4304-3/ADA4304-4 are fabricated using the Analog Devices, Inc., proprietary silicon germanium (SiGe), complementary bipolar process, enabling them to achieve very low levels of distortion with a noise figure of 4.6 dB. The parts provide low cost alternatives that simplify designs and improve system performance by integrating a signal splitter element and a gain block into a single IC. The ADA4304-3/ADA4304-4 are available in a 16-lead LFCSP and operate in the extended industrial temperature range of −40°C to +85°C.

**Rev. 0**



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## REVISION HISTORY

**11/07—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{CC}$ = 5 V, 75 Ω system, $T_A$ = 25°C, unless otherwise noted.

**Table 1.**

| Parameter | Conditions | ADA4304-3 | | | ADA4304-4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| DYNAMIC PERFORMANCE | See Figure 19 for test circuit | | | | | | | |
| Bandwidth (−3 dB) | | | 2400 | | | 2400 | | MHz |
| Frequency Range | | 54 | | 865 | 54 | | 865 | MHz |
| Gain | f = 100 MHz | | 3.3 | | | 2.9 | | dB |
| Gain Flatness | 54 MHz to 865 MHz | | 1.0 | | | 1.0 | | dB |
| NOISE/DISTORTION PERFORMANCE | | | | | | | | |
| Noise Figure[1] | @ 54 MHz | | 4.0 | | | 4.0 | | dB |
| | @ 550 MHz | | 4.6 | | | 4.6 | | dB |
| | @ 865 MHz | | 4.8 | | | 4.8 | | dB |
| Output IP3 | $f_1$ = 97.25 MHz, $f_2$ = 103.25 MHz | | 26 | | | 26 | | dBm |
| Output IP2 | $f_1$ = 97.25 MHz, $f_2$ = 103.25 MHz | | 43 | | | 43 | | dBm |
| Composite Triple Beat (CTB) | 135 channels, 15 dBmV/channel, f = 865 MHz | | −72 | | | −72 | | dBc |
| Composite Second Order (CSO) | 135 channels, 15 dBmV/channel, f = 865 MHz | | −62 | | | −62 | | dBc |
| Cross Modulation (CXM) | 135 channels, 15 dBmV/channel, 100% modulation @ 15.75 kHz, f = 865 MHz | | −68 | | | −68 | | dBc |
| INPUT CHARACTERISTICS | See Figure 19 for test circuit | | | | | | | |
| Input Return Loss | @ 54 MHz | | −17 | −13 | | −18 | −14 | dB |
| | @ 550 MHz | | −22 | −16 | | −21 | −15 | dB |
| | @ 865 MHz | | −12 | −8 | | −12 | −8 | dB |
| Output-to-Input Isolation | Any output, 54 MHz to 865 MHz | | | | | | | |
| | @ 54 MHz | | −33 | −30 | | −33 | −31 | dB |
| | @ 550 MHz | | −33 | −30 | | −33 | −31 | dB |
| | @ 865 MHz | | −34 | −31 | | −35 | −32 | dB |
| OUTPUT CHARACTERISTICS | See Figure 19 and Figure 20 for test circuits | | | | | | | |
| Output Return Loss | Any output, 54 MHz to 865 MHz | | | | | | | |
| | @ 54 MHz | | −21 | −17 | | −21 | −17 | dB |
| | @ 550 MHz | | −16 | −11 | | −17 | −12 | dB |
| | @ 865 MHz | | −14 | −9 | | −14 | −9 | dB |
| Output-to-Output Isolation | Any output, 54 MHz to 865 MHz | | | | | | | dB |
| | @ 54 MHz | | −26 | | | −26 | | dB |
| | @ 550 MHz | | −25 | | | −25 | | dB |
| | @ 865 MHz | | −25 | | | −25 | | dB |
| 1 dB Compression (P1dB) | Output referred, f = 100 MHz | | 9.0 | | | 8.7 | | dBm |
| POWER SUPPLY | | | | | | | | |
| Nominal Supply Voltage | | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| Quiescent Supply Current | | | 92 | 105 | | 92 | 105 | mA |

[1] Characterized with 50 Ω noise figure analyzer.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 5.5 V |
| Power Dissipation | See Figure 3 |
| Storage Temperature Range | −65°C to +125°C |
| Operating Temperature Range | −40°C to +85°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the device (including exposed pad) soldered to a high thermal conductivity 4-layer (2s2p) circuit board, as described in EIA/JESD 51-7.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 16-Lead LFCSP (Exposed Pad) | 98 | °C/W |

### *Maximum Power Dissipation*

The maximum safe power dissipation in the ADA4304-3/ADA4304-4 package is limited by the associated rise in junction temperature ($T_J$) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package ($P_D$) is essentially equal to the quiescent power dissipation, that is, the supply voltage ($V_S$) times the quiescent current ($I_S$). In Table 1, the maximum power dissipation of the ADA4304-3/ADA4304-4 can be calculated as

$$P_{D\,(MAX)} = 5.25\ \text{V} \times 105\ \text{mA} = 551\ \text{mW}$$

Airflow increases heat dissipation, effectively reducing $\theta_{JA}$. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through-holes, ground, and power planes reduces the $\theta_{JA}$.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 16-lead LFCSP (98°C/W) on a JEDEC standard 4-layer board.

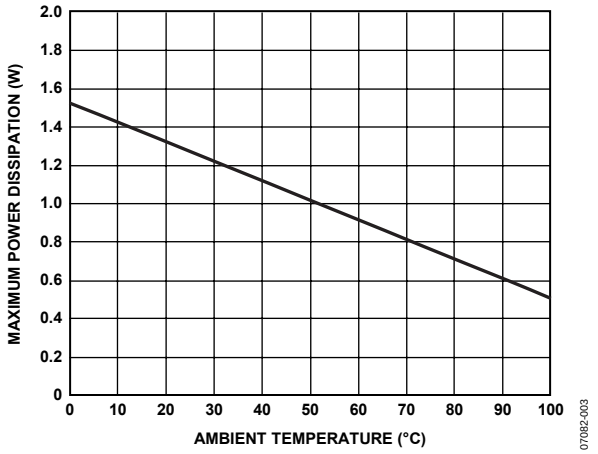


*Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board*

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

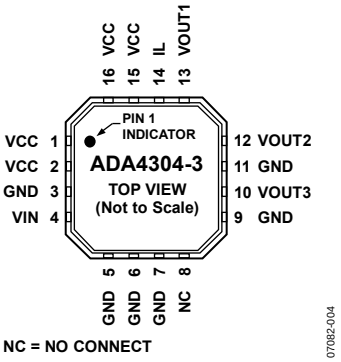


*Figure 4. ADA4304-3 Pin Configuration*

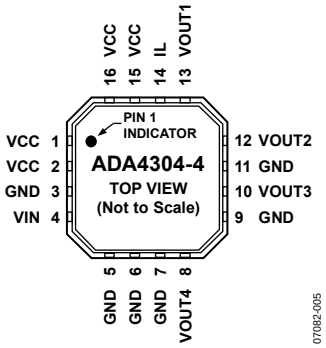


*Figure 5. ADA4304-4 Pin Configuration*

**Table 4. ADA4304-3 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 2, 15, 16 | VCC | Supply Pin. |
| 3, 5 to 7, 9, 11 | GND | Ground. |
| 4 | VIN | Input. |
| 8 | NC | No Connection. |
| 10 | VOUT3 | Output 3. |
| 12 | VOUT2 | Output 2. |
| 13 | VOUT1 | Output 1. |
| 14 | IL | Bias Pin. |

**Table 5. ADA4304-4 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 2, 15, 16 | VCC | Supply Pin. |
| 3, 5 to 7, 9, 11 | GND | Ground. |
| 4 | VIN | Input. |
| 8 | VOUT4 | Output 4. |
| 10 | VOUT3 | Output 3. |
| 12 | VOUT2 | Output 2. |
| 13 | VOUT1 | Output 1. |
| 14 | IL | Bias Pin. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC}$ = 5 V, 75 Ω system, $T_A$ = 25°C, unless otherwise noted.

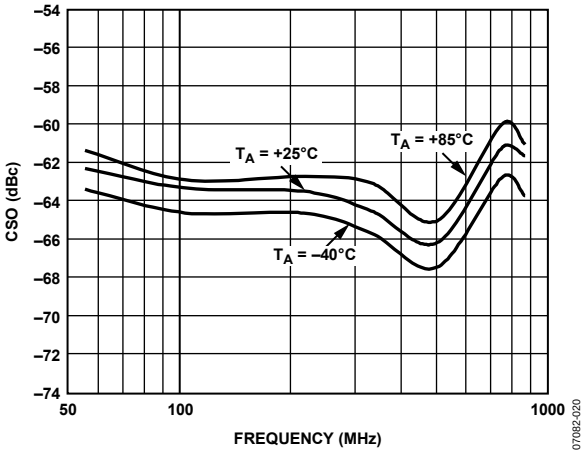


Figure 6. Composite Second Order (CSO) vs. Frequency

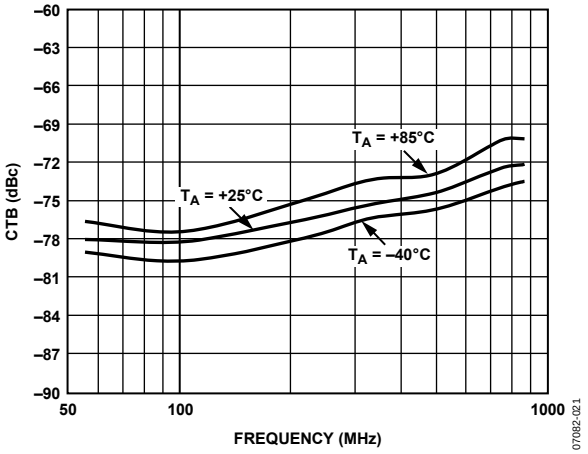


Figure 7. Composite Triple Beat (CTB) vs. Frequency

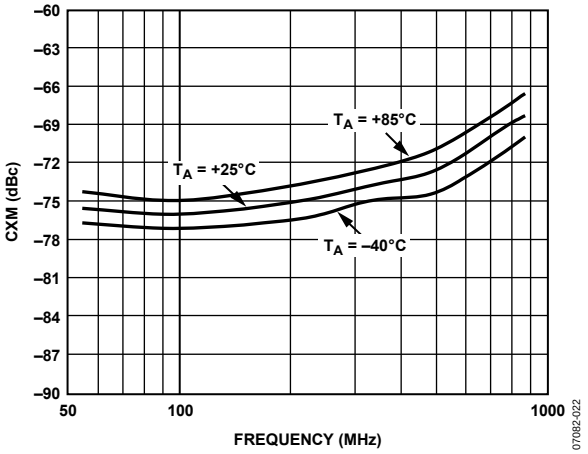


Figure 8. Cross Modulation (CXM) vs. Frequency

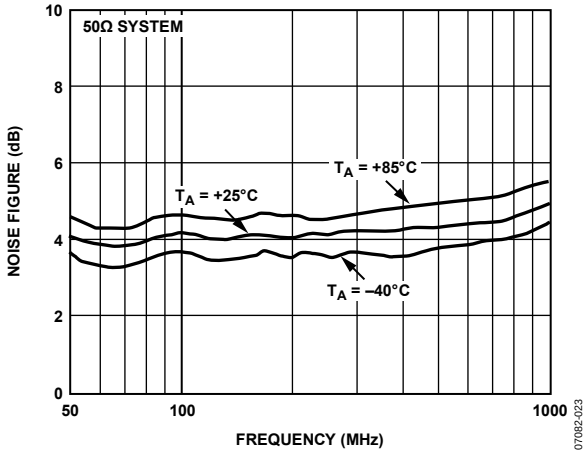


Figure 9. Noise Figure vs. Frequency

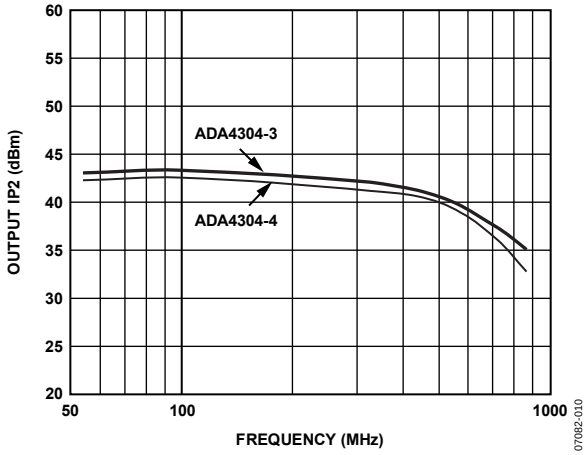


Figure 10. Output IP2 vs. Frequency

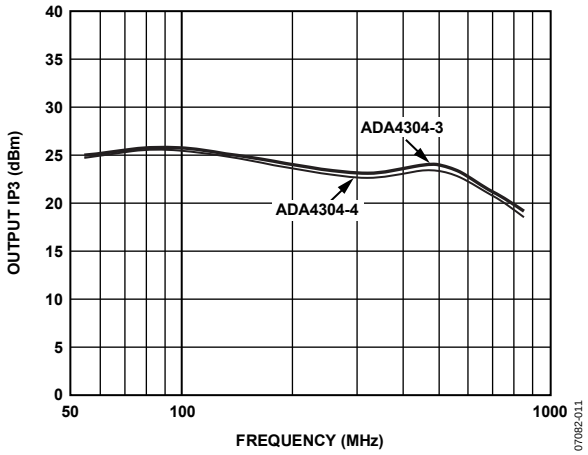


Figure 11. Output IP3 vs. Frequency

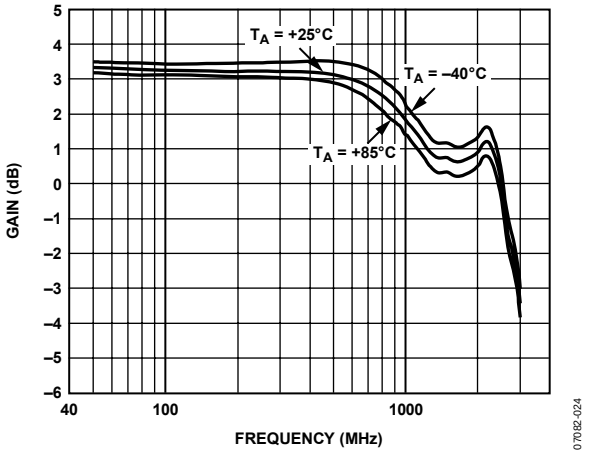


Figure 12. ADA4304-3 Gain vs. Frequency

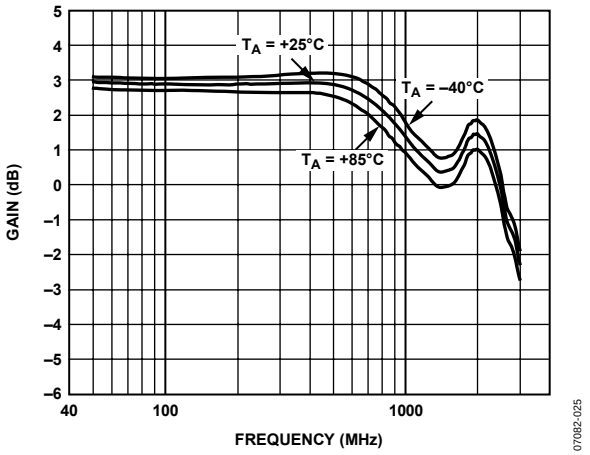


Figure 13. ADA4304-4 Gain vs. Frequency

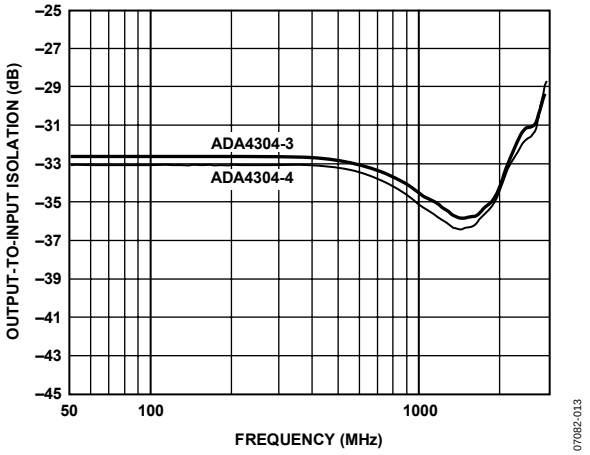


Figure 14. Output-to-Input Isolation vs. Frequency

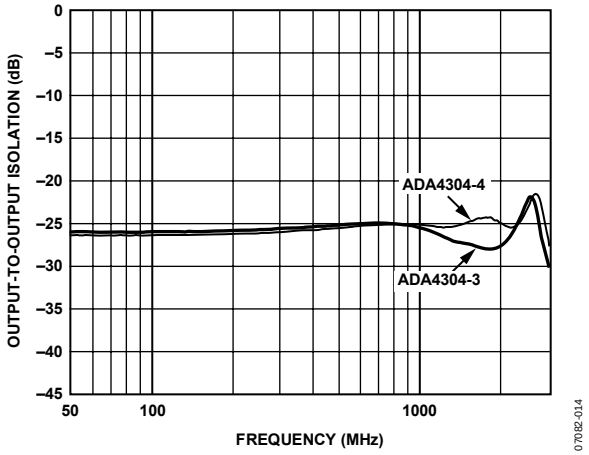


Figure 15. Output-to-Output Isolation vs. Frequency

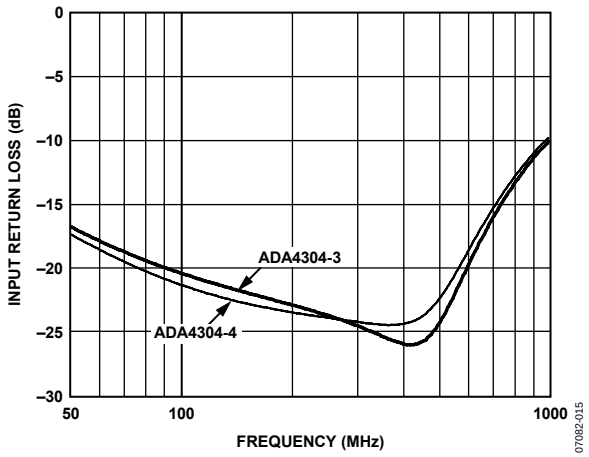


Figure 16. Input Return Loss vs. Frequency

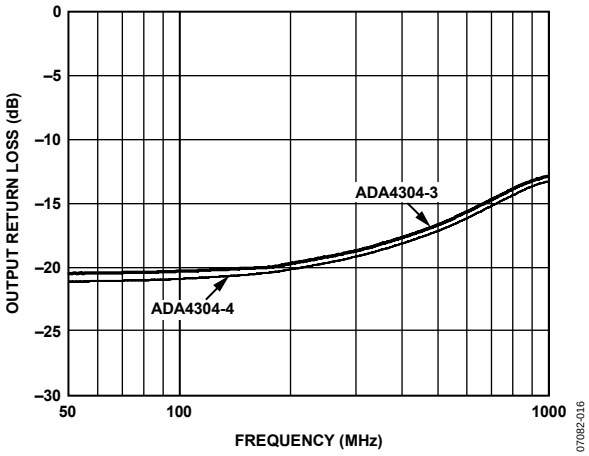


Figure 17. Output Return Loss vs. Frequency

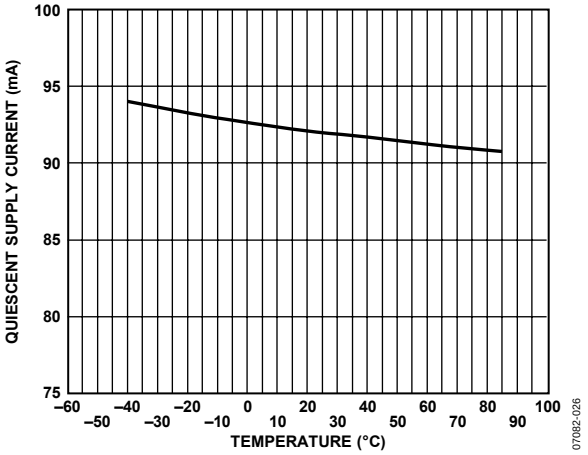


*Figure 18. Quiescent Supply Current vs. Temperature*

# TEST CIRCUITS

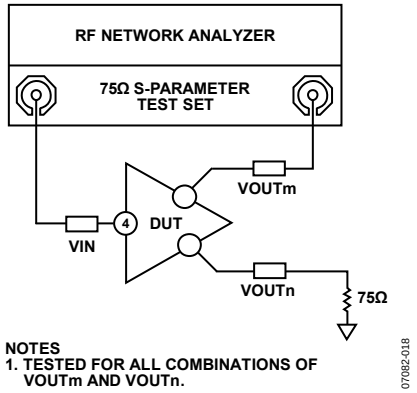


*Figure 19. Test Circuit for Transmission, Isolation, and Reflection Measurements*

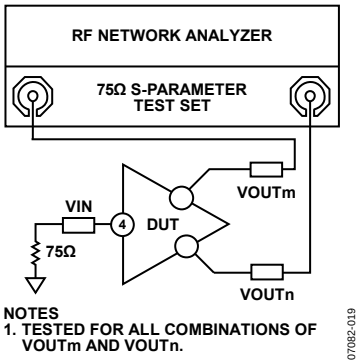


*Figure 20. Test Circuit for Output-to-Output Isolation Measurements*

# APPLICATIONS

The ADA4304-3/ADA4304-4 active splitters are primarily intended for use in the downstream path of television set-top boxes (STBs) that contain multiple tuners. They are typically located directly after the diplexer in a bidirectional CATV customer premise unit. The ADA4304-3/ADA4304-4 provide a single-ended input and three or four single-ended outputs that allow the delivery of the RF signal to multiple signal paths. These paths can include, but are not limited to, a main picture tuner, the picture-in-picture (PIP) tuner, an out-of-band (OOB) tuner, a digital video recorder (DVR), and a cable modem (CM).

The ADA4304-3/ADA4304-4 exhibit composite second-order (CSO) and composite triple beat (CTB) products that are −62 dBc and −72 dBc, respectively. The use of the SiGe bipolar process also allows the ADA4304-3/ADA4304-4 to achieve a noise figure (NF) of 4.6 dB at 550 MHz.

## CIRCUIT DESCRIPTION

The ADA4304-3/ADA4304-4 consist of a low noise buffer amplifier followed by a resistive power divider. This arrangement provides 3.3 dB (ADA4304-3) or 2.9 dB (ADA4304-4) of gain relative to the RF signal present at the input of the device. The input and each output must be properly matched to a 75 Ω environment for distortion and noise performance to match the data sheet specifications. AC coupling capacitors of 0.01 µF are recommended for the input and outputs.

A 1 µH RF choke (Coilcraft chip inductor 0805LS-102X) is required to correctly bias the internal nodes of the ADA4304-3/ADA4304-4. It should be connected between the 5 V supply and the IL pin (Pin 14). The choke should be placed as close as possible to the ADA4304-3/ADA4304-4 to minimize parasitic capacitance on the IL pin, which is critical for achieving the specified bandwidth and flatness.

## EVALUATION BOARDS

The ADA4304-3/ADA4304-4 evaluation board allows designers to assess the performance of the parts in their particular application. The board includes 75 Ω coaxial connectors and 75 Ω controlled-impedance signal traces that carry the input and output signals. Power (5 V) is applied to the red VCC loop connector, and ground is connected to the black GND loop connector. Figure 21 is a schematic of the evaluation board. On the ADA4304-3 evaluation board, connector VO4 and C7 are not populated.

## RF LAYOUT CONSIDERATIONS

Appropriate impedance matching techniques are mandatory when designing circuit boards for the ADA4304-3/ADA4304-4. Improper characteristic impedances on traces can cause reflections that can lead to poor linearity. The characteristic impedance of the signal trace to the input and from each output should be 75 Ω. Any ground metal on the top surface near signal lines should be stitched with vias to the internal ground plane, as shown in Figure 22. The device package exposed paddle must be reflow soldered to a low inductance ground to achieve data sheet performance specifications. This is achieved by connecting the footprint ground pad with vias to a ground plane below (see Figure 22).

## POWER SUPPLY

The 5 V supply should be applied to each VCC pin and RF choke via a low impedance power bus. The power bus should be decoupled to ground using a 10 µF tantalum capacitor and a 0.1 µF ceramic chip capacitor located close to the ADA4304-3/ADA4304-4. In addition, the VCC pins should be decoupled to ground with a 0.1 µF ceramic chip capacitor located as close to each pin as possible.

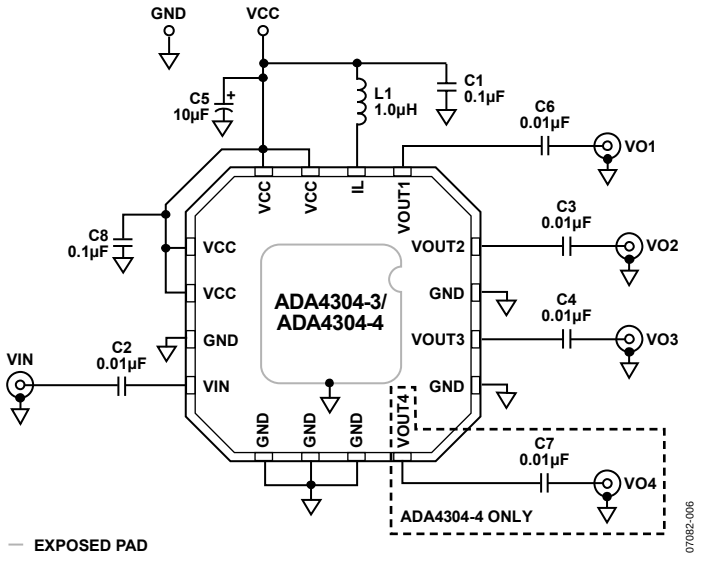


*Figure 21. Evaluation Board Schematic*

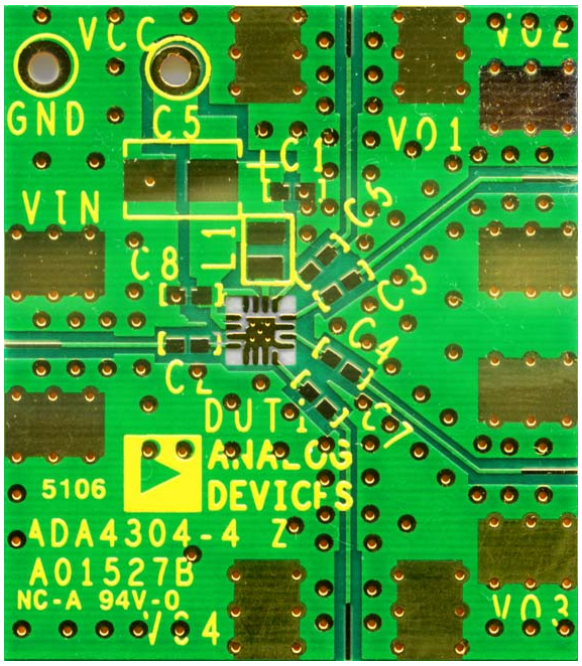


Figure 22. Evaluation Board

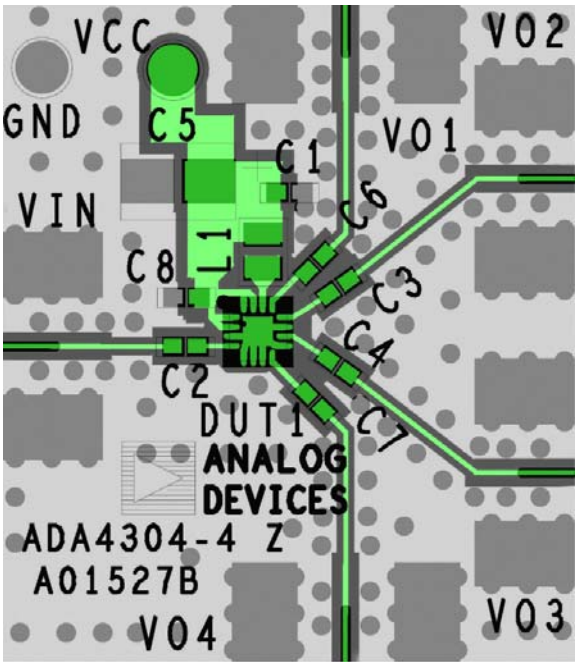


Figure 23. Evaluation Board Component Layout

# OUTLINE DIMENSIONS

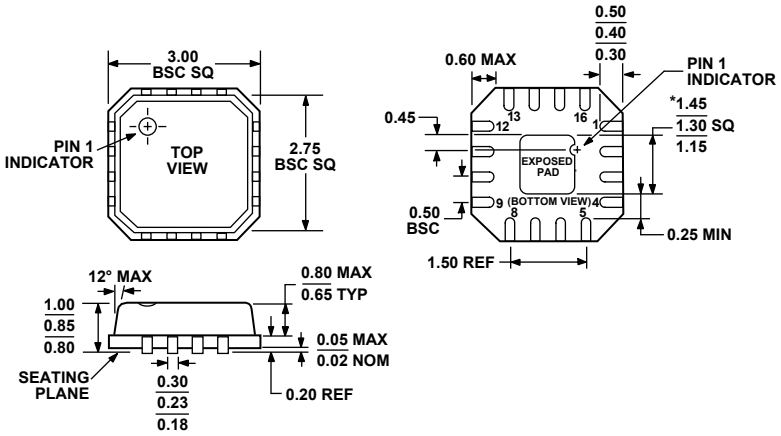


*Figure 24. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*3 mm × 3 mm Body, Very Thin Quad*
*(CP-16-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Ordering Quantity | Branding |
|---|---|---|---|---|---|
| ADA4304-3ACPZ-RL[1] | −40°C to +85°C | 16-Lead LFCSP_VQ | CP-16-2 | 5,000 | H16 |
| ADA4304-3ACPZ-R7[1] | −40°C to +85°C | 16-Lead LFCSP_VQ | CP-16-2 | 1,500 | H16 |
| ADA4304-3ACPZ-R2[1] | −40°C to +85°C | 16-Lead LFCSP_VQ | CP-16-2 | 250 | H16 |
| ADA4304-4ACPZ-RL[1] | −40°C to +85°C | 16-Lead LFCSP_VQ | CP-16-2 | 5,000 | H10 |
| ADA4304-4ACPZ-R7[1] | −40°C to +85°C | 16-Lead LFCSP_VQ | CP-16-2 | 1,500 | H10 |
| ADA4304-4ACPZ-R2[1] | −40°C to +85°C | 16-Lead LFCSP_VQ | CP-16-2 | 250 | H10 |

[1] Z = RoHS Compliant Part.