Low Noise, Low Input Bias Current, Wide Bandwidth JFET Operational Amplifiers

Preliminary Technical Data

ADA4001-2

FEATURES

Low T_CV_{OS}: 2 µV/°C typical
Low input bias current: TBD pA typical at V_S = ±15 V
Dual-supply operation: ±4.5 V to ±15 V
Low noise:
8.5 nV/√Hz typical at f = 1 kHz
0.7 $µV_{P-P}$ at 0.1 Hz to 10 Hz
Low distortion: 0.00008%
No phase reversal
Rail-to-Rail Output
Unity gain stable

APPLICATIONS

Instrumentation
Medical Instruments
Multipole filters
Precision current measurement
Photodiode amplifiers
Sensors
Audio

PIN CONFIGURATIONS

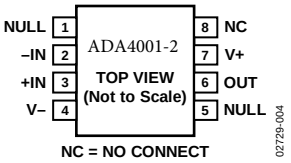

Figure 1. 8-Lead SOIC_N (R Suffix)

GENERAL DESCRIPTION

The ADA4001-2 is a dual JFET amplifier that features low input bias current, input voltage noise, input current noise, and rail-to-rail output.

The combination of low noise and very low input bias currents makes these amplifiers especially suitable for high impedance sensor amplification. Unlike many competitive amplifiers, the ADA4001-2 maintain their fast settling performance even with substantial capacitive loads. Unlike many older JFET amplifiers, the ADA4001-2 do not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range.

Fast slew rate and great stability with capacitive loads make the ADA4001-2 a perfect fit for high performance filters. Low input bias currents, low offset, and low noise result in a wide dynamic range of photodiode amplifier circuits. Low noise and distortion, high output current, Rail-to-Rail Output and excellent speed make the ADA4001-2 a great choice for audio frequency applications.

The ADA4001-2 is specified over the −40°C to +125°C extended industrial temperature range.

The ADA4001-2 is available in 8-lead narrow SOIC, 8-lead.

Rev. PrA

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SPECIFICATIONS

@ V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			±0.5	±1.5	mV
		−40°C < T_A < +125°C			±2.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			±2		µV/°C
Input Bias Current	I_B			TBD	30	pA
		−40°C < T_A < +125°C			4	nA
Input Offset Current	I_{OS}				20	pA
		−40°C < T_A < +125°C			2	nA
Input Voltage Range			−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12.5V	96	110		dB
		−40°C < T_A < +125°C	90			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = ±13.5 V	104	110		dB
		−40°C < T_A < +125°C	90			dB
Input Capacitance, Differential Mode	C_{INDM}			3.1		pF
Input Capacitance, Common Mode	C_{INCM}			4.8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	14.8	14.9		V
		−40°C < T_A < +125°C	TBD			V
		R_L = 600 Ω	14.2	14.3		V
		−40°C < T_A < +125°C	TBD			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ		−14.8	−14.7	V
		−40°C < T_A < +125°C			TBD	V
		R_L = 600 Ω		-14.7	-14.6	V
		−40°C < T_A < +125°C			TBD	V
Output Current	I_{OUT}			±40		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	96	120		dB
		−40°C < T_A < +125°C	100			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		2	3	mA
		−40°C < T_A < +125°C			4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	±15[1]	±25		V/µs
Gain Bandwidth Product	GBP			8		MHz
Settling Time	t_S	To 0.1%, 0 V to 10 V step, G = +1		TBD		µs
		To 0.01%, 0 V to 10 V step, G = +1		TBD		µs
Total Harmonic Distortion (THD) + Noise	THD + N	1 kHz, G = +1, R_L = 2 kΩ		0.00008		%
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz bandwidth		0.8		µV p-p
Voltage Noise Density	e_n	f = 100 Hz		8.5		nV/√Hz
		f = 1 kHz		7.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		3		fA/√Hz

[1]Guaranteed by design and characterization

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$\pm V_S$
Output Short-Circuit Duration to GND	Observe derating curves
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Electrostatic Discharge (Human Body Model)	3000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead SOIC_N (R)	120	45	°C/W

[1] θ_{JA} is specified for worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages. This was measured using a standard 4-layer board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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