Preliminary

Elan Microelectronics Crop.

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ELAN RISC II™ series

ePC160

160 x 160 dot matrix monochrome LCD controller
Suggest use EK7011 LCD driver

January 24, 2005
Version 1.0

Specification Revision History		
Version	**Content**	**Date**
0.1	Initial version	2/17/2004
0.2	Add pad diagram Modify used body by the EPG6400, change pad list EPG1280 to EPG6400. Add command X & Y to SPI timing diagram.	3/23/2004
0.3	Add new no command & successive more than 2 commands in SPI control. Modify SPI maximum bit rate 625000	3/26/2004
1.0	Modify main part by ePC160.	8/31/2004

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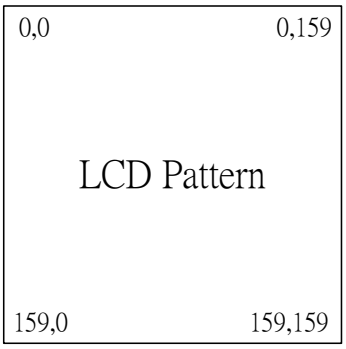
I. General Description

The **ePC160** is a dot matrix monochrome LCD controller supporting resolutions up to 160 x 160. Data control user serial peripheral interface (SPI).

II. Features

- ✧ CMOS process.
- ✧ Logic power supply: 2.2V ~ 3.6V.
- ✧ Two clock mode: Low frequency is 32KHz (RC oscillator) & High frequency is 9.83MHz (PLL capacitor).
- ✧ SPI (Serial Peripheral Interface) maximum bit rate is 625000.
- ✧ Power down mode.
- ✧ Package: QFP100.

III. LCD pattern format



Pattern format:

=> (0,0) … (0,159),
(1,0) … (1,159),
(2,0) … (158,159),
:
:
(158,0) … (158,159),
(159,0) … (159,159).

Display data map:

Y \ X		X axis data location (20)									
		00	01	02	03	…….	0F	10	11	12	13
Y axis data location	00	0~7	8~15	16~23	24~31	…….	120~127	128~135	136~143	144~151	152~159
	01	0~7	8~15	16~23	24~31	…….	120~127	128~135	136~143	144~151	152~159
	9E	0~7	8~15	16~23	24~31	…….	120~127	128~135	136~143	144~151	152~159
	9F	0~7	8~15	16~23	24~31	……	120~127	128~135	136~143	144~151	152~159

Command & Data receiver format:

1. Normal format:

   Command [address X] => Command [address Y] => Data [8 bits]…Data [8 bits] => STB toggle.

2. Successive more than 2 command format:

   Command [address X] => Command [address Y] => Data [8 bits]…Data [8 bits]
   => Command [address X] => Command [address Y] => Data [8 bits]…Data [8 bits] => STB toggle.

3. No command format:

   Address X & Y (0 & 0): Data [8 bits]…Data [8 bits] => STB toggle.

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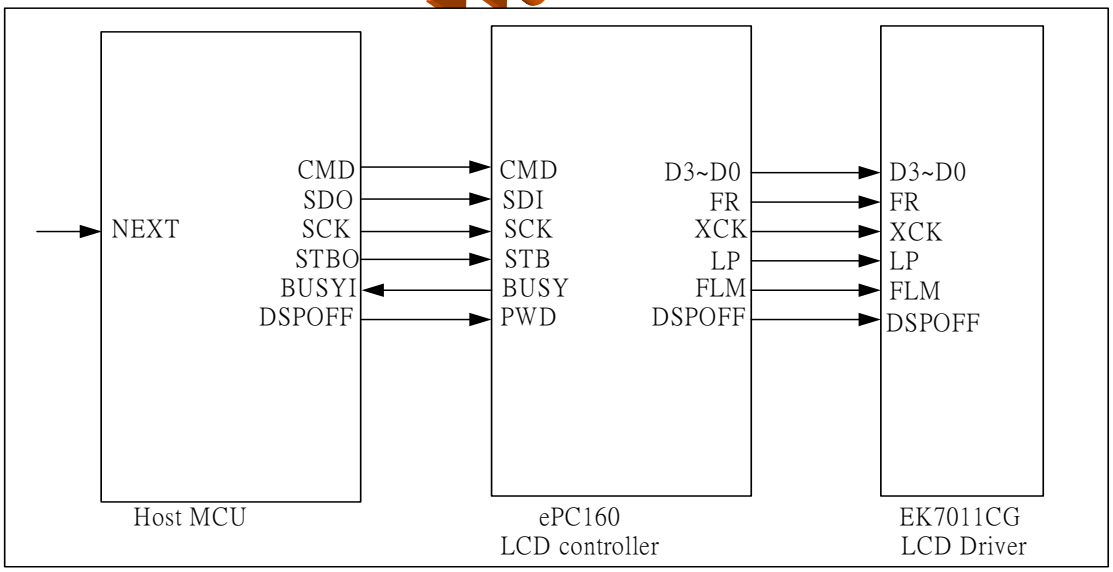
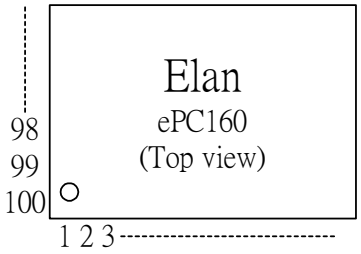
IV. Function Block



V. Pin Assignment



No.	Pin NAME	No.	Pin NAME	No.	Pin NAME	No.	Pin NAME	No.	Pin NAME
1	N.C.	21	N.C.	41	N.C.	61	N.C.	81	N.C.
2	N.C.	22	N.C.	42	N.C.	62	N.C.	82	N.C.
3	N.C.	23	N.C.	43	N.C.	63	N.C.	83	N.C.
4	RESET KEY	24	N.C.	44	N.C.	64	N.C.	84	N.C.
5	SYS RESET	25	N.C.	45	FLM	65	N.C.	85	N.C.
6	VDD	26	PWD	46	LP	66	N.C.	86	N.C.
7	N.C.	27	BUSY	47	XCK	67	N.C.	87	N.C.
8	N.C.	28	SCK	48	N.C.	68	N.C.	88	N.C.
9	N.C.	29	N.C.	49	N.C.	69	N.C.	89	N.C.
10	N.C.	30	N.C.	50	N.C.	70	N.C.	90	N.C.
11	N.C.	31	N.C.	51	D0	71	N.C.	91	N.C.
12	N.C.	32	SDI	52	D1	72	N.C.	92	N.C.
13	PLLC	33	CMD	53	D2	73	N.C.	93	N.C.
14	VSS	34	N.C.	54	D3	74	N.C.	94	N.C.
15	RC	35	FR	55	N.C.	75	N.C.	95	N.C.
16	N.C.	36	DSPOFF	56	N.C.	76	N.C.	96	N.C.
17	TEST	37	N.C.	57	N.C.	77	N.C.	97	N.C.
18	N.C.	38	N.C.	58	N.C.	78	N.C.	98	N.C.
19	N.C.	39	N.C.	59	N.C.	79	N.C.	99	N.C.
20	STB	40	N.C.	60	N.C.	80	N.C.	100	N.C.

VI. Pin Description

✧ System control pin list:

Name	I/O/P type	Description
VDD VSS	P	Digital power supply, the range is from 2.2V to 3.6V. Suggest is connect to VSS through capacitors (0.1uF).
AVDD VSS	P	Analog power supply, the range is from 2.2V to 3.6V. Suggest is connect to VSS through capacitors (0.1uF).
SYS RESET	I	System reset input with built-in pull up resistor (100K ohm typically).
RESET KEY	I	Low voltage related reset pin. Low: RESET asserted, High: RESET released.
TEST	I	Normal connects to VSS, reserved for testing.
RC	I	RC oscillator connect pin, Should be connect to VDD through resistor (2M ohm).
PLLC	I	PLL capacitor connect pin, Should be connect to VSS through capacitors (0.047uF).

✧ LCD controller control pin list:

Name	I/O/P type	Description
PWD	I	Control LCD operator to power down mode. Active low.
SDI	I	Serial data input pin.
SCK	I	Serial clock input pin.
STB	I	Data receive ending strobe signal.
BUSY	O	LCD controller change pattern operation signal.
CMD	O	Command operation signal, 0: X & Y display address, 1: Display data.
D0~D3	O	Output for LCD data. (In 4-bit parallel data bus)
FR	O	Alternation signal. The LCD driver output voltage level of output pin can be sated using the line latch output signal and the FR signal.
XCK	O	Clock signal shifting data. Data is read on the falling edge of the clock pulse.
LP	O	Data latch signal. Data is latch on the falling edge of the clock pulse.
FLM	O	First line marker.
DSPOFF	O	Display on/off control signal. The output signal is level-shifted from logic voltage level to LCD driver voltage level, and controls LCD driver circuit.

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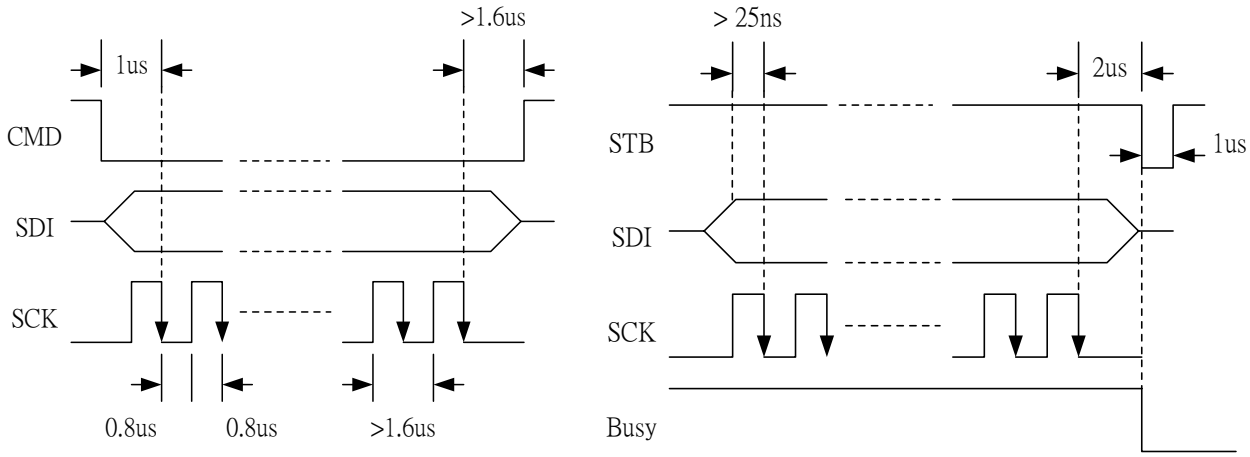
VII. SPI control timing

SPI control description:

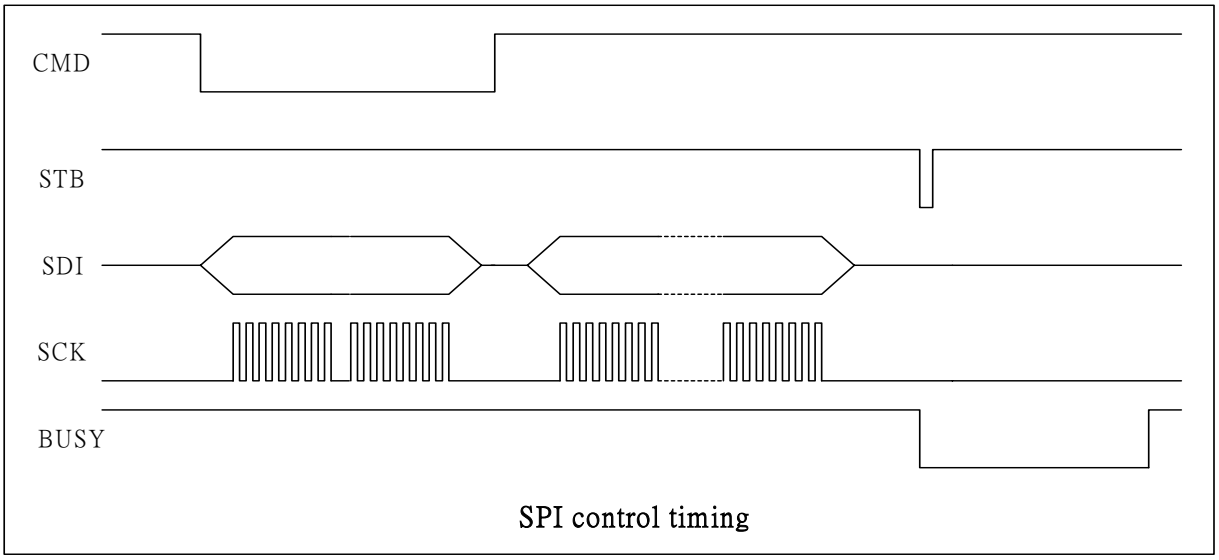
- ✧ Shift buffer length 8 bits.
- ✧ Transmit bit rate is 625000. (max.)
- ✧ Latch is falling edge.
- ✧ Data transmission order is shift right. (LSB first)

SPI control timing:



1. Normal format:

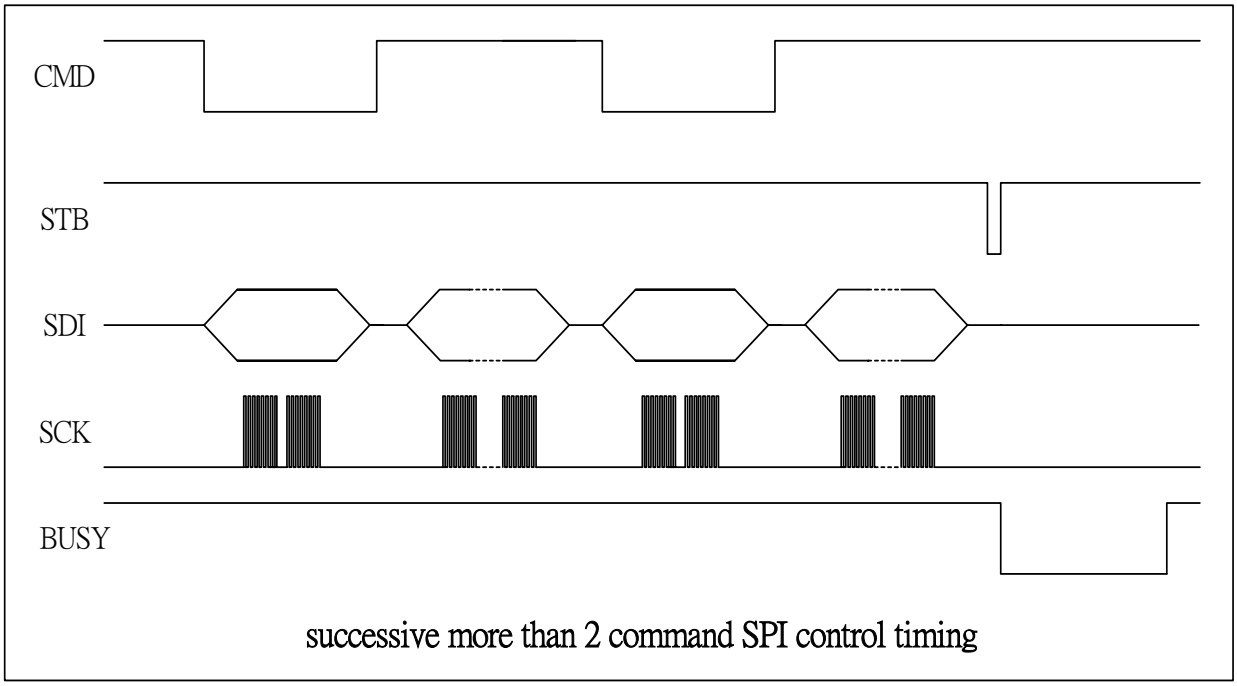
Command [address X] => Command [address Y] => Data [8 bits]…Data [8 bits] => STB toggle.



SPI control timing

2. Successive more than 2 command format:

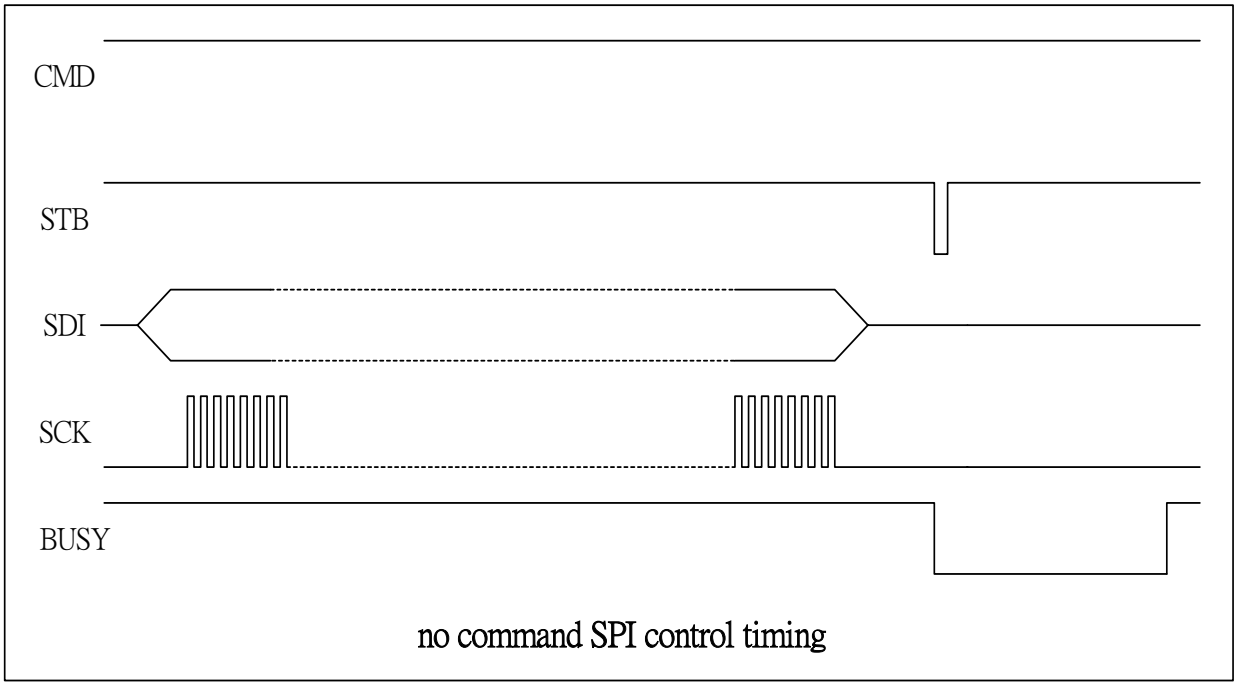
Command [address X] => Command [address Y] => Data [8 bits]…Data [8 bits]
=> Command [address X] => Command [address Y] => Data [8 bits]…Data [8 bits] => STB toggle.



successive more than 2 command SPI control timing

3. No command format:

Address X & Y (0 & 0): Data [8 bits]…Data [8 bits] => STB toggle.



no command SPI control timing

VIII. Application circuit

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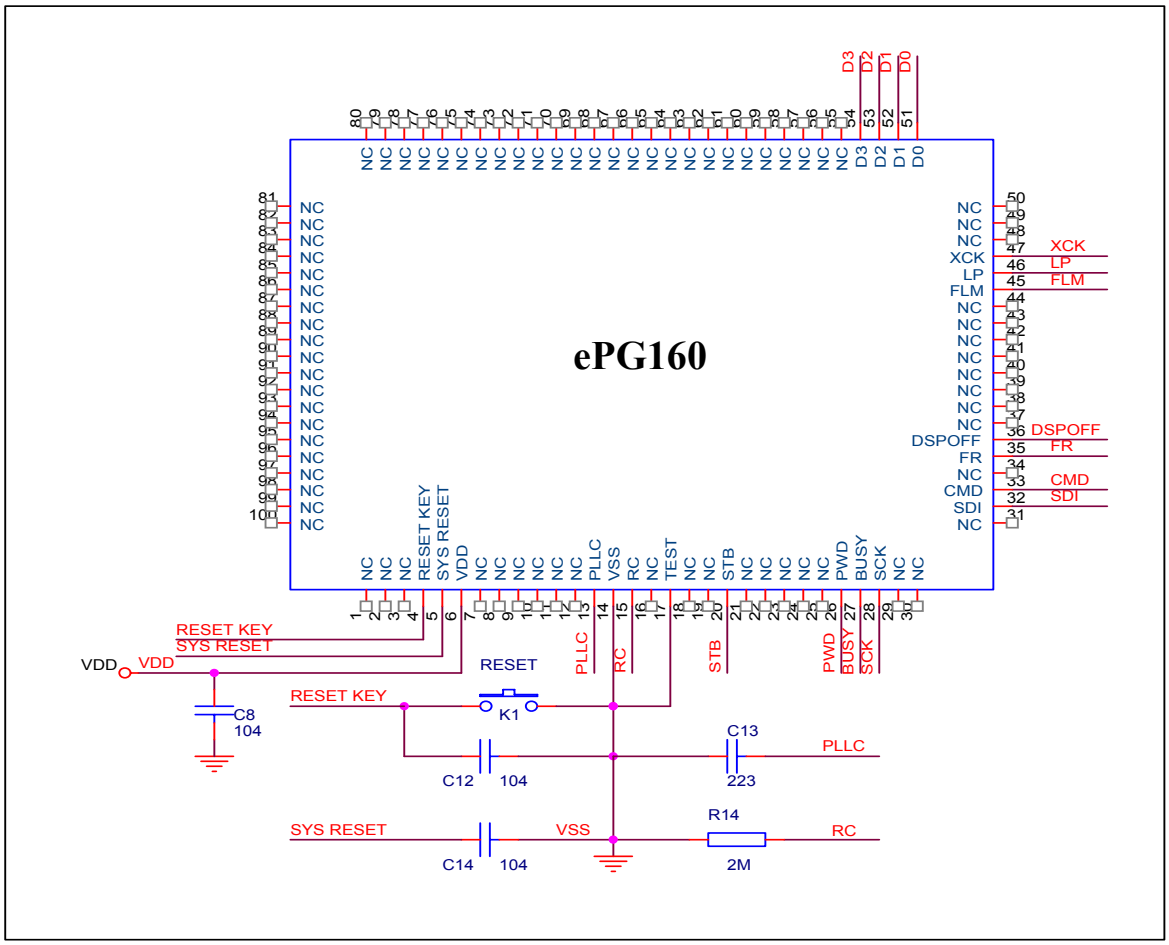
Application circuit BOM list

LCD controller:		Charge bump circuit:			
ePC160	1 pcs	MC34063A	1 pcs	LM324	1 pcs
C 104	3 pcs	L > 170uH	1 pcs	C 1uF/25V	5 pcs
C 473	1 pcs	C 104	1 pcs	C 104	1 pcs
R 2Mohm	1 pcs	C 470pF	1 pcs	R 100Kohm	4 pcs
		C 100uF	1 pcs	R 910Kohm	1 pcs
		C 200uF/25V	1 pcs	R 33 ohm	4 pcs
		R 1 ohm	1 pcs		
		R 180 ohm			
		R 2.7Kohm			
		VR 50Kohm			
		D 1N5819			



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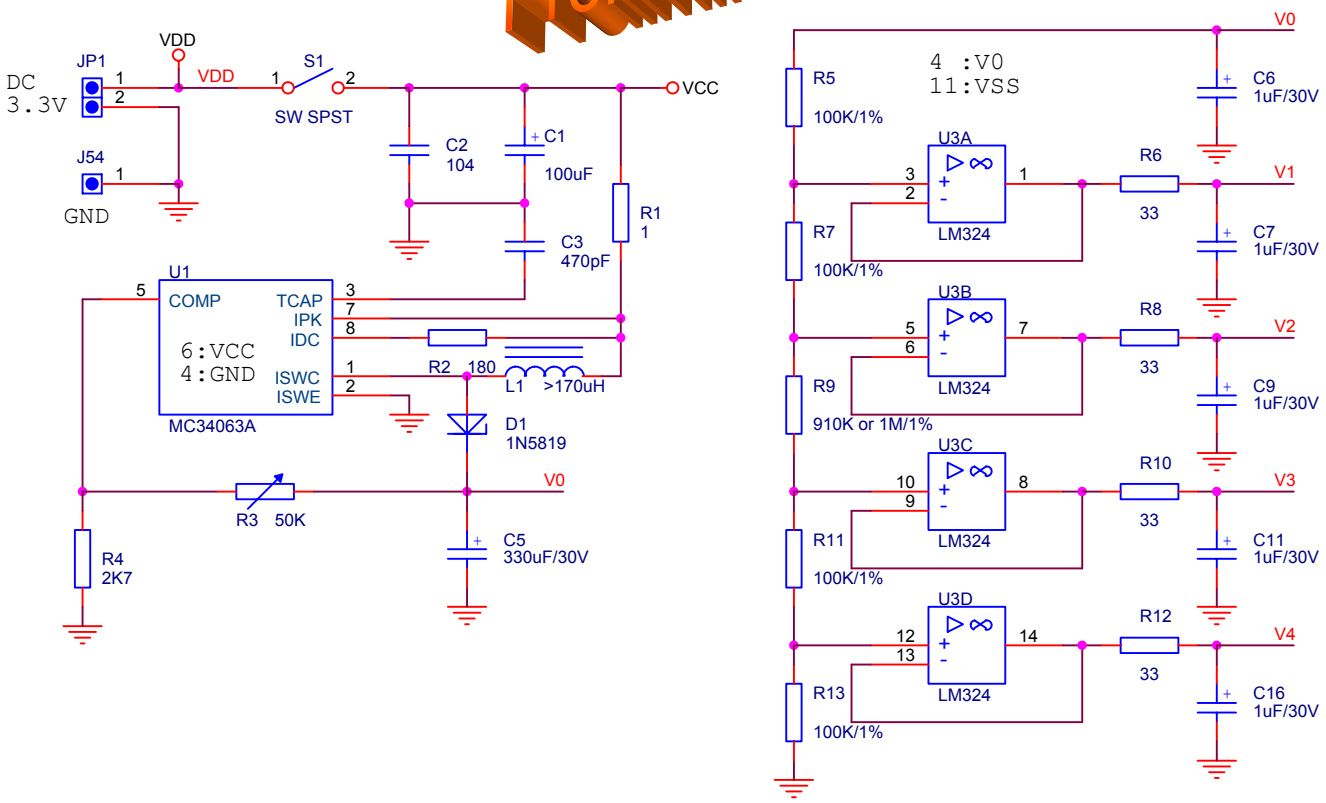
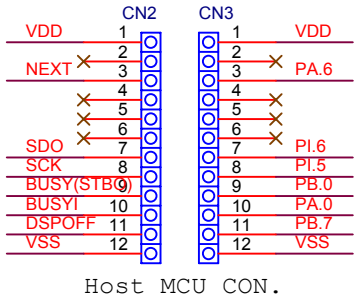
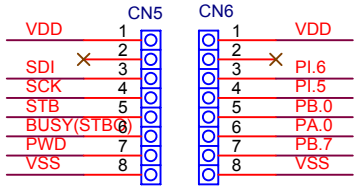
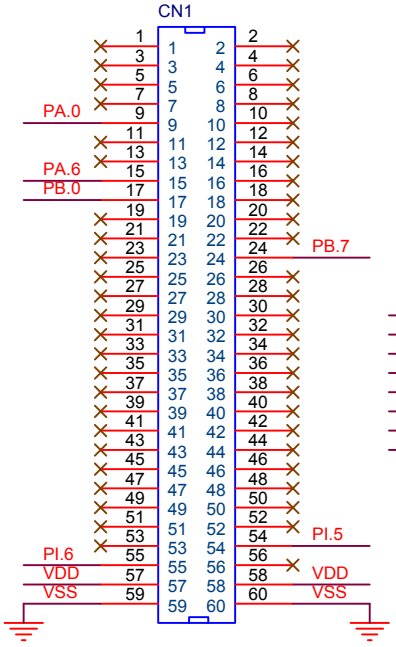


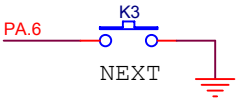


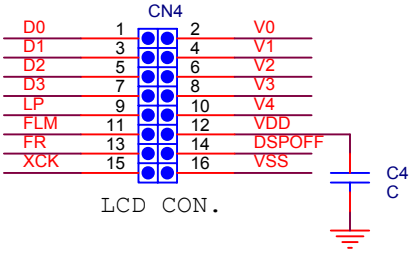
Host MCU CON.



LCD controller CON.







LCD CON.

IX. Electrical characteristic

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ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Limits	Unit
Supply voltage	VDD		-0.3 to +3.6	V
Input voltage	VIN		-0.5 to VDD +0.5	V
Operating temperature range	TOPR		-10 to +60	°C
Storage temperature range	TSTR		-55 to +125	°C

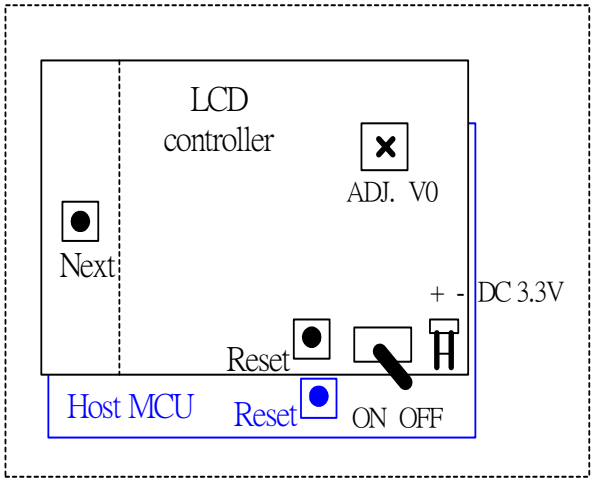
RECOMMENDED OPERATING CONDITIONS

Items	Sym.	Condition	Limits	Unit
Supply voltage	VDD		2.6 to 3.2	V
Input voltage	VIH		VDD*0.9 to VDD	V
	VIL		0 to VDD*0.1	V
Operating temperature	TOPR		-10 to +60	°C

DC ELECTRICAL CHARACTERISTICS (condition: Ta=-10~+60 °C, VDD= 2.9 +/- 0.3V)

Parameter	Sym.	Condition		Min	Typ	Max	Unit
CLOCK	Fmain	Main-clock frequency		-	9.83	-	MHz
	Fsub	Sub-clock frequency	RC OSC.	24.6	32.8	41	KHz
Supply current	Idd1	SLEEP mode	VDD=3V, no load	-	-	1	μA
	Idd2	FAST mode	VDD=3V, Fmain=10MHz, no load	-	2000	2500	
Large Pull up resistance	RPU1	SYSTEM RESET, RESET_KEY	Vin=GND	200	400	800	KΩ
Small Pull up resistance	RPU2	SYSTEM RESET, RESET_KEY	Vin=2V	50	100	200	KΩ
Large Pull down resistance	RPD1	TEST	Vin=VDD	250	500	750	KΩ
Small Pull down resistance	RPD2	TEST	Vin=1V	5	10	15	KΩ
Data retention voltage	Vret			1.6	-	-	V
Power ON reset voltage	Vpor			1.4	1.5	1.6	V

X. Demo board operation (For EPL160 IC)



Step1. Power on. (Supply voltage DC3.3V)
Step 2. Press Host MCU board [Reset] key.
Step 3. Press LCD controller board [Reset] key.
Step 4. Turn on LCD power switch. (OFF to ON)
Step 5. Press [Next] key is change next picture.
Step 6. Turn off LCD power switch. (ON to OFF)
Step 7. Power off.

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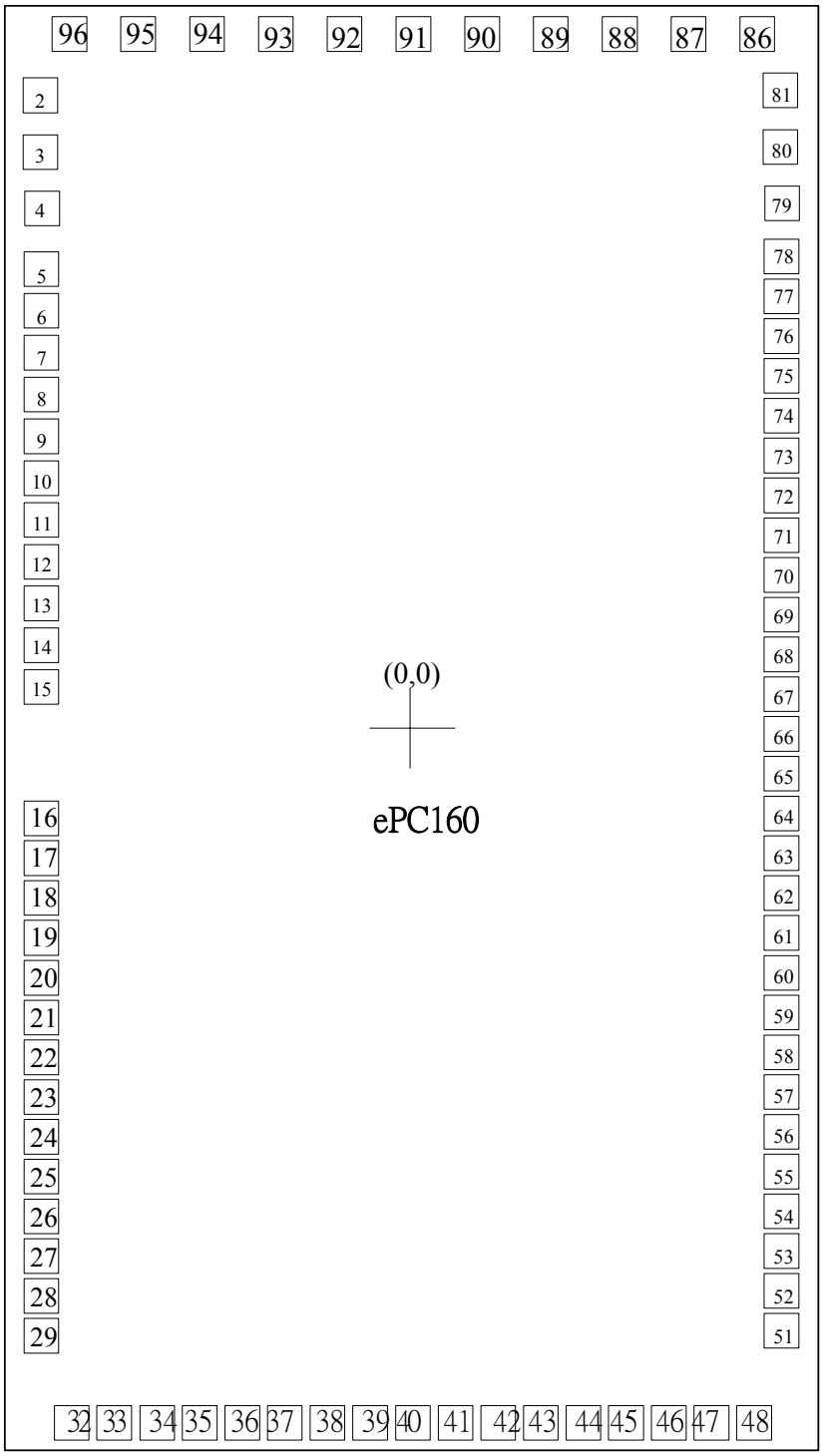
XI. Pad diagram



Chip size : 2350 * 4490 um

Pin NO.	Symbol	X	Y	Pin NO.	Symbol	X	Y
1	NC			51	D0	1026.2	-1797.8
2	NC	-1030.0	1909.0	52	D1	1026.2	-1682.8
3	NC	-1030.0	1710.7	53	D2	1026.2	-1567.8
4	RESET KEY	-1030.0	1522.0	54	D3	1026.2	-1452.8
5	SYS RESET	-1030.0	1262.2	55	NC	1026.2	-1337.8
6	VDD	-1030.0	1142.3	56	NC	1026.2	-1222.8
7	NC	-1030.0	1000.3	57	NC	1026.2	-1107.8
8	(Reserved)	-1030.0	868.2	58	NC	1026.2	-992.8
9	(Reserved)	-1030.0	748.3	59	NC	1026.2	-887.8
10	(Reserved)	-1030.0	628.3	60	NC	1026.2	-762.8
11	(Reserved)	-1030.0	508.3	61	NC	1026.2	-647.8
12	(Reserved)	-1030.0	388.3	62	NC	1026.2	--532.8
13	PLLC	-1030.0	258.3	63	NC	1026.2	-417.9
14	VSS	-1030.0	138.3	64	NC	1026.2	-302.8
15	RC	-1030.0	6.3	65	NC	1026.2	-187.8
16	NC	-1030.0	-304.7	66	NC	1026.2	-72.8
17	TEST	-1030.0	-424.7	67	NC	1026.2	42.2
18	NC	-1030.0	-542.2	68	NC	1026.2	157.2
19	NC	-1030.0	-659.7	69	NC	1026.2	272.2
20	STB	-1030.0	-779.7	70	NC	1026.2	387.2
21	NC	-1030.0	-899.7	71	NC	1026.2	502.2
22	NC	-1030.0	-1019.7	72	NC	1026.2	617.2
23	NC	-1030.0	-1139.7	73	NC	1026.2	732.2
24	NC	-1030.0	-1259.7	74	NC	1026.2	847.2
25	NC	-1030.0	-1379.7	75	NC	1026.2	962.2
26	PWD	-1030.0	-1499.7	76	NC	1026.2	1077.2
27	BUSY	-1030.0	-1617.2	77	NC	1026.2	1192.2
28	SCK	-1030.0	-1732.2	78	NC	1026.2	1307.2
29	NC	-1030.0	-1847.2	79	NC	1026.2	1515.4
30	NC			80	NC	1026.2	1713.7
31	NC			81	NC	1026.2	1902.4
32	SDI	-894.1	-2100.0	82	NC		
33	CMD	-776.6	-2100.0	83	NC		
34	NC	-656.6	-2100.0	84	NC		
35	FR	-536.6	-2100.0	85	NC		
36	DSPOFF	-416.6	-2100.0	86	NC	967.1	2093.5
37	NC	-299.1	-2100.0	87	NC	778.4	2093.5
38	NC	-184.1	-2100.0	88	NC	580.1	2093.5
39	NC	-69.1	-2100.0	89	NC	391.4	2093.5
40	NC	45.9	-2100.0	90	NC	193.1	2093.5
41	NC	160.9	-2100.0	91	NC	4.4	2093.5
42	NC	275.9	-2100.0	92	NC	-193.9	2093.5
43	NC	390.9	-2100.0	93	NC	-382.6	2093.5
44	NC	505.9	-2100.0	94	NC	-580.9	2093.5
45	FLM	620.9	-2100.0	95	NC	-769.6	2093.5
46	LP	735.9	-2100.0	96	NC	-967.9	2093.5
47	XCK	850.9	-2100.0	97	NC		
48	NC	965.9	-2100.0	98	NC		
49	NC			99	NC		
50	NC			100	NC		

Note: Pad 8 ~ Pad 12 is for factory test only. Please do NOT bonding these pads on application circuit.

For PCB layout, IC substrate must be connected to VSS.