Aimtron
圓創科技股份有限公司

AT1736

Preliminary Product Information

LCD Panel Power Supplies with High-Current Operational Amplifiers

Features

- 2.6V to 5.5V Input Supply Range
- 1.2MHz Current-Mode PWM Step-Up Regulator:
  - Fast Transient Response
  - 1.5% High-Accuracy Output Voltage
  - Built-In 17V, 2.5A, 0.16Ω N-Channel MOSFET Current-Limit
  - High Efficiency
- High-Current Operational Amplifiers:
  - ±150mA Output Short-Circuit Current
  - 13V/µs Slew Rate
  - 12MHz, -3dB Bandwidth
  - Rail-to-Rail Inputs/Outputs
- Gate-On and Gate-off Linear Regulator Controllers
- Gate-on Pulse Modulator with Adjustable Delay for Sequence Control
- Latched Fault Protection with Timer

Applications

- LCD Monitor Panel Modules
- TV LCD Panel Modules
- Automotive Displays

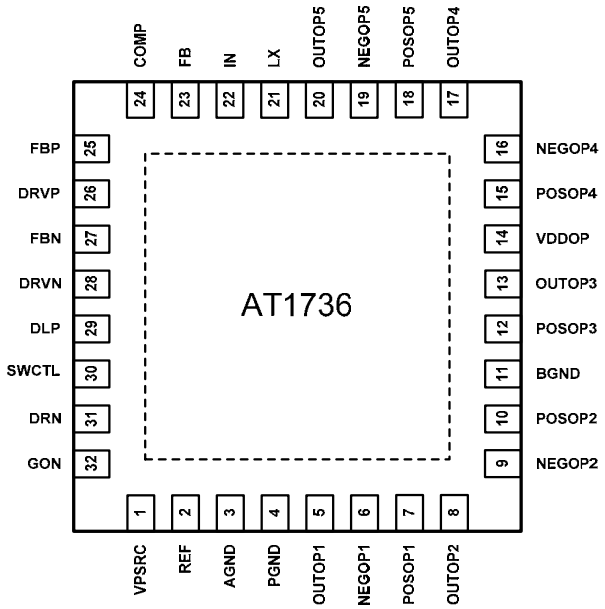
General Description

The AT1736 offers a complete power-supply solution for TFT LCD panels used in LCD monitors and LCD TVs. The AT1736 consists of a high-performance step-up converter, two linear-regulator controllers, five high-current operational amplifiers, and a logic-controlled gate-on pulse modulator.

The step-up DC-DC converter provides the regulated supply voltage for the panel source driver ICs. The two linear regulators provide the regulated positive gate-on and negative gate-off supply voltages from external charge-pumps. The operational amplifier supplies the VCOM & GAMMA buffers with high output current, fast slew rate and wide bandwidth performances for driving capacitive loads. The high-voltage gate-on pulse modulator to control the positive gate-on output voltage waveform.

The AT1736 is available in a 32-pin thin QFN package which is 5mm x 5mm with a maximum thickness of 0.8mm for ultra thin LCD panel design.

Pin Configuration



Aimtron reserves the right without notice to change this circuitry and specifications.

7F, No.9,PARK AVENUE. II, Science-Based Industrial Park, Hsinchu 300,Taiwan, R.O.C.
Tel: 886-3-563-0878 Fax: 886-3-563-0879 WWW: http://www.aimtron.com.tw
10/19/2007 REV:0.5 Email: service@aimtron.com.tw

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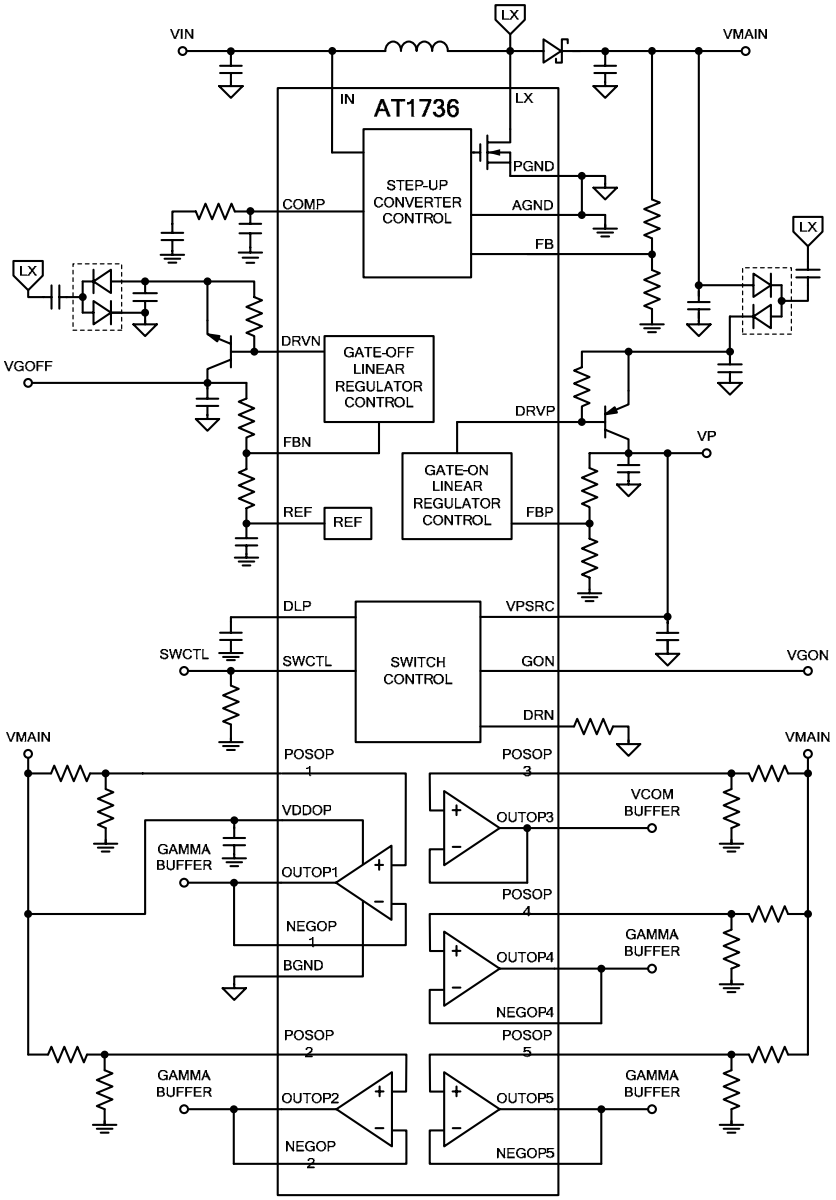
Ordering Information

Part number	Package	Marking
AT1736N_GRE	Thin QFN32, Green	AT1736N

Block Diagram



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Pin Descriptions

Pin No.	Pin Name	Function
1	VPSRC	Gate-on Pulse Modulator Voltage Supply Input. Source of the internal high-voltage P-channel MOSFET connected to GON. Connect a minimum 0.1µF capacitor close to the VPSRC and PGND pins.
2	REF	Reference Output. Connect a 0.22µF capacitor from REF to GND. REF remains on in shutdown.
3	AGND	Analog Ground for the Signal Control of the Regulators.
4	PGND	Power Ground. PGND is the source of the n-channel power MOSFET of step-up converter. Place the input-capacitor ground terminals close to PGND with a wide trace.
5	OUTOP1	Operational Amplifier 1 Output.
6	NEGOP1	Operational Amplifier 1 inverting Input.
7	POSOP1	Operational Amplifier 1 Noninverting Input.
8	OUTOP2	Operational Amplifier 2 Output.
9	NEGOP2	Operational Amplifier 2 inverting Input.
10	POSOP2	Operational Amplifier 2 Noninverting Input.
11	BGND	Analog Ground for Operational Amplifiers.
12	POSOP3	Operational Amplifier 3 Noninverting Input.
13	OUTOP3	Operational Amplifier 3 Output.
14	VDDOP	Operational Amplifier Power Supply Input. Connect a 0.1µF capacitor from VDDOP to BGND.
15	POSOP4	Operational Amplifier 4 Noninverting Input.
16	NEGOP4	Operational Amplifier 4 inverting Input.
17	OUTOP4	Operational Amplifier 4 Output
18	POSOP5	Operational Amplifier 5 Noninverting Input.
19	NEGOP5	Operational Amplifier 5 inverting Input.
20	OUTOP5	Operational Amplifier 5 Output.
21	LX	Drain of Internal N-Channel Power MOSFET of Step-up Converter. Minimize the connecting trace area for the lowest EMI.
22	IN	IC Supply Voltage Input.
23	FB	Step-Up Converter Feedback Input. Connect a resistive voltage-divider to determine the step-up converter output voltage. Place the resistive voltage-divider close to this pin.
24	COMP	Compensation pin of Error-Amplifier of the Step-Up Converter. Connect a compensation network from COMP to AGND.
25	FBP	Positive Gate-On Linear Regulator Feedback Input. Connect a resistive voltage-divider to determine the gate-on linear regulator output voltage. Place the resistive voltage-divider close to this pin.
26	DRVP	Transistor Base Driver of Positive Gate-On Linear-Regulator. Open drain of an internal n-channel MOSFET. Connect DRVP to the base of an external pnp transistor.
27	FBN	Negative Gate-Off Linear-Regulator Feedback Input. Connect a resistive voltage-divider to determine the gate-off linear regulator output voltage. Place the resistive voltage-divider close to this pin.
28	DRVN	Transistor Base Driver of Negative Gate-off Linear Regulator. Open drain of an internal p-channel MOSFET. Connect DRVN to the base of an external npn transistor.
29	DLP	Positive Gate-on Pulse Modulator Delay Input. Connect a capacitor from DLP to GND to set the delay time.
30	SWCTL	Gate-on Pulse Modulator Timing Control Input.
31	DRN	Discharge Switch Input. Connect a resistor to GND to discharge the V_{GON} when SWCTL is low.

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32	GON	Internal High-voltage Gate-on Pulse Modulator Output Terminal for Positive Gate-on Voltage Supply.

Absolute Maximum Ratings (Ta = 25℃)

Parameter	Rated Value		Unit
	Min.	Max.	
IN, FB, FBP, FBN, COMP, REF, SWCTL, DLP	-0.3	+6.0	V
PGND, BGND to AGND	-0.3	+0.3	V
LX, VDDOP	-0.3	+17.0	V
POSOP_, NEGOP_, OUTOP_	-0.3	+17.0	V
DRVN	V_{IN}-30	V_{IN} +0.3	V
DRVP, VPSRC, GON, DRN	-0.3	+30.0	V
DRN to GON	-30.0	+30.0	V
LX Switch Maximum Continuous RMS Output Current	-	1.6	A
OUTOP Maximum Continuous Output Current	-75.0	+75.0	mA
Power Dissipation (Ta≦25℃)	-	1702	mW
Operating Temperature	-35	+85	^{0}C
Storage Temperature	-55	+150	^{0}C
Lead Temperature (soldering, 10s)	-	+260	^{0}C
ESD Susceptibility (MM)	-200	200	V
ESD Susceptibility (HBM)	-2	2	KV

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Devices are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Recommended Operating Conditions

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Operating Supply Range	V_{IN}	2.6	-	5.5	V
Operating Temperature*	T_{OP}	-20	+25	+85	℃
Operating Junction Temperature	T_J	-	-	+150	℃

***Using X5R or X7R capacitors.**

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Electrical Characteristics

(Test circuit is shown as Typical Application Circuit, unless otherwise noted. V_{IN} = 3V, V_{VDDOP} = 8V, PGND = AGND = BGND = 0, I_{REF} = 25µA, Ta= 0℃ to +85℃. Typical values are at Ta=+25℃.)

Parameter	Condition	Values			Unit
		Min.	Typ.	Max.	
IN Operating Supply Range		2.6		5.5	V
IN Undervoltage-Lockout Threshold	V_{IN} rising	2.3	2.5	2.7	V
	Hysteresis		150		mV
IN Quiescent Current	V_{FB} = V_{FBP} = 1.4V, V_{FBN} = 0V, LX not switching		0.8	1.1	mA
	V_{FB} = 1.1V, V_{FBP} = 1.4V, V_{FBN} = 0V, LX switching		6	11	
Duration to Trigger Fault condition			55		ms
REF Output Voltage	-10µA < I_{REF} < 50µA, VIN = 2.6 to 5.5V	1.210	1.233	1.256	V
Step-Up Converter Section					
Output Voltage Range		V_{IN}		16	V
Operating Frequency		1020	1200	1380	kHz
Oscillator Maximum Duty Cycle		84	87	90	%
Feedback Regulation voltage	No load, Ta = +25℃	1.210	1.233	1.256	V
FB Input Bias Current	V_{FB} = 1.4V	-50	1	50	nA
FB Fault Trip Level	V_{FB} falling	0.90	1.00	1.10	V
FB Load Regulation	0 mA < I_{LX} < full load, transient only		-1.6		%
FB Line Regulation	2.6V < Vin < 5.5V		±0.04	±0.15	%/V
FB Transconductance	ΔI_{COMP} = 1.4V	75	160	280	µS
FB Voltage Gain	FB to COMP		600		V/V
LX Switch On-Resistance			160	250	mΩ
LX Leakage Current	V_{LX} = 17V		0.02	40	µA
LX Current Limit	V_{IN} = 3.3V	2.5	3.0	3.5	A
Current-Sense Transconductance		3.0	3.8	5	S
Soft-Start Period t_{SS}			14		ms
Soft-Start Step Size			I_{LIM} / 8		A
Operational Amplifiers Section					
VDDOP Supply Operating Range		4.5		16	V

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VDDOP Supply Current	Buffer configuration, V_{POSOP} = 4V, no load		3.2	4.8	mA
Input Offset Voltage	(V_{NEGOP}, V_{POSOP}) = V_{VDDOP} / 2, T_A = +25°C	-16	0	16	mV
Input Bias Current	(V_{NEGOP}, V_{POSOP}) = V_{VDDOP} / 2	-50	1	50	nA
Common-Mode Input Range	V_{NEGOP}, V_{POSOP}	0		V_{VDDOP}	V
Common-Mode Rejection Ratio	0 ≦ (V_{NEGOP}, V_{POSOP}) < V_{VDDOP}	45			dB
Open-Loop Gain			125		dB
Output Voltage Swing High	I_{OUTOP} = 100µA	V_{VDDOP} -15	V_{VDDOP} - 3		mV
	I_{OUTOP} = 5mA	V_{VDDOP} -150	V_{VDDOP} - 80		mV
Output Voltage Swing Low	I_{OUTOP} = -100µA		2	15	mV
	I_{OUTOP} = -5mA		80	150	
Short-Circuit Current	Short to V_{VDDOP} / 2, sourcing	50	150		mA
	Short to V_{VDDOP} / 2, sinking	50	150		
Output Current	Buffer configuration, V_{POSOP} = 4V, V_{OUTOP} error < ±10mV	±40			mA
Power-Supply Rejection Ratio	6V ≦ V_{VDDOP} ≦ 13.2V, DC (V_{NEGOP}, V_{POSOP}) = V_{VDDOP} / 2	60			dB
Slew Rate			13		V/µs
-3dB Bandwidth	Buffer configuration, R_L = 10kΩ, C_L = 10pF		12		MHz
Gain-Bandwidth Product	Buffer configuration		8		MHz
Gate-On Linear Regulator Controller Section					
FBP Regulation Voltage	I_{DRVP} = 100µA	1.210	1.233	1.256	V
FBP Fault Trip Level	V_{FBP} falling	0.90	1.00	1.10	V
FBP Input Bias Current	V_{FBP} = 1.4V	-50		+50	nA
FBP Effective Load-Regulation Error (Transconductance)	V_{DRVP} = 10V, I_{DRVP} = 50µA to 1mA		-0.7	-1.5	%
FBP Line (IN) Regulation Error	I_{DRVP} = 100µA, 2.6V < V_{IN} < 5.5V		±1.5	±5	mV
DRVP Sink Current	V_{FBP} = 1.1V, V_{DRVP} = 10V	1	5		mA
DRVP Off-Leakage Current	V_{FBP} = 1.4V, V_{DRVP} = 28V		0.01	10	µA
Soft-Start Period			14		ms
Soft-Start Step Size			V_{REF} / 128		V

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Gate-Off Linear Regulator Controller Section					
FBN Regulation Voltage	I_{DRVN} = 100µA	235	250	265	mV
FBN Fault Trip Level	V_{FBN} rising	320	420	520	mV
FBN Input Bias Current	V_{FBN} = 0V	-50		+50	nA
FBN Effective Load-Regulation Error (Transconductance)	V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA		11	25	mV
FBN Line (IN) Regulation Error	I_{DRVN} = 100µA, 2.6V < V_{IN} < 5.5V		±0.7	±5	mV
DRVN Source Current	V_{FBN} = 500mV, V_{DRVN} = -10V	1	4		mA
DRVN Off-Leakage Current	V_{FBN} = 0V, V_{DRVN} = -25V		-0.01	-10	µA
Soft-Start Period			14		ms
Soft-Start Step Size			V_{REF} / 128		V
Gate-on Pulse Modulator Section					
DLP Capacitor Charge Current	During startup, V_{DLP} = 1.0V	4	5	6	µA
DLP Turn-On Threshold		1.210	1.233	1.256	V
DLP Discharge Switch On-Resistance	During UVLO, V_{IN} = 2.2V		20		Ω
SWCTL Input Low Voltage				0.6	V
SWCTL Input High Voltage		2.0			V
SWCTL Input Leakage Current		-1		+1	µA
SWCTL to GON Propagation Delay	Rising & Falling		100		ns
VPSRC Input Voltage Range				30	V
VPSRC Input Current	V_{DLP}=1.5V, SWCTL=high		50	100	µA
	V_{DLP}=1.5V, SWCTL=low		15	30	µA
VPSRC to GON Switch On-Resistance	V_{DLP}=1.5V, SWCTL=high		6	12	Ω
DRN to GON Switch On-Resistance	V_{DLP}=1.5V, SWCTL =low		35	70	Ω

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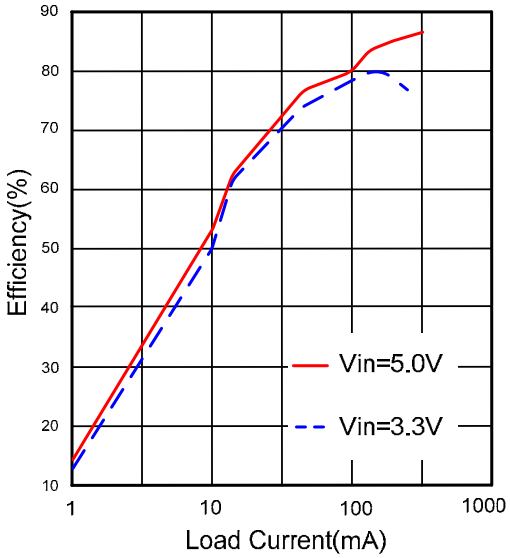
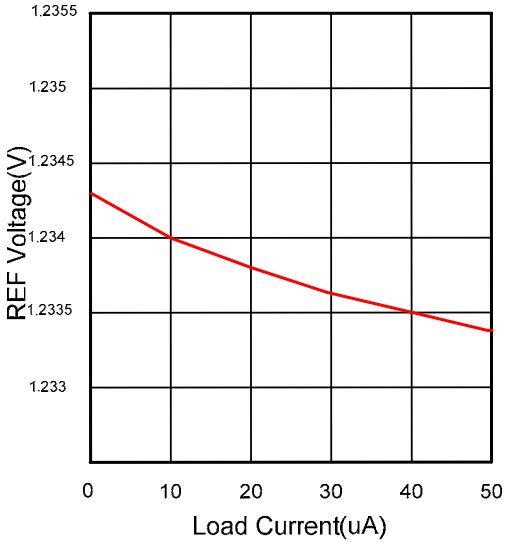
Typical Characteristics：

(V_{IN}=5.0V, V_{MAIN}=13.5V, V_P=23.5V, V_{GOFF}=-8.0V, T_A=+25℃, unless otherwise noted.)

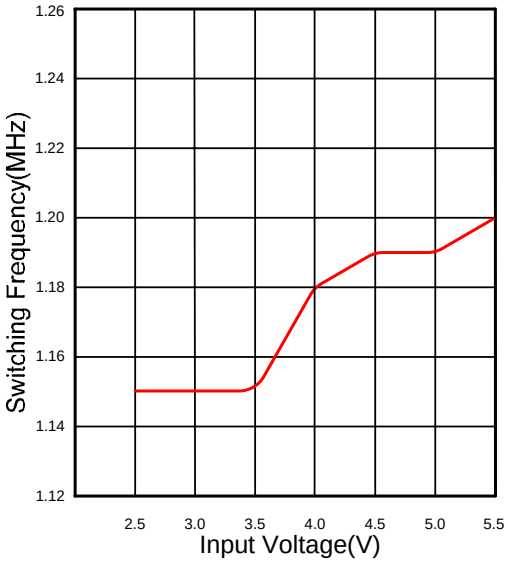
V_{MAIN} Efficiency VS. Load Current



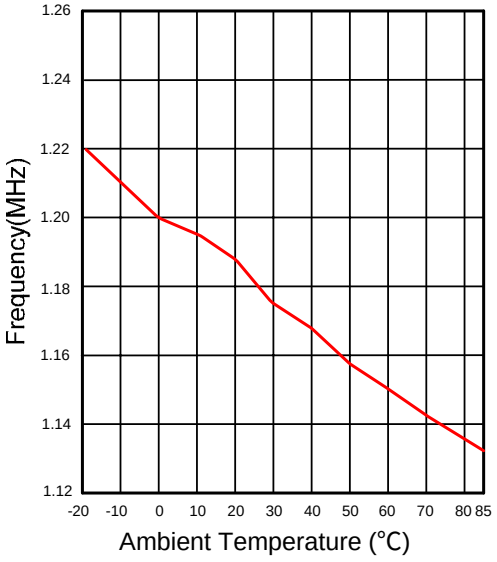
REF Voltage Load Regulation



Switching Frequency VS. Input Voltage



Switching Frequency VS. Ambient Temperature



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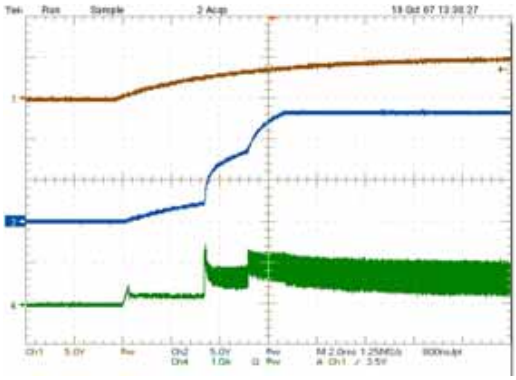
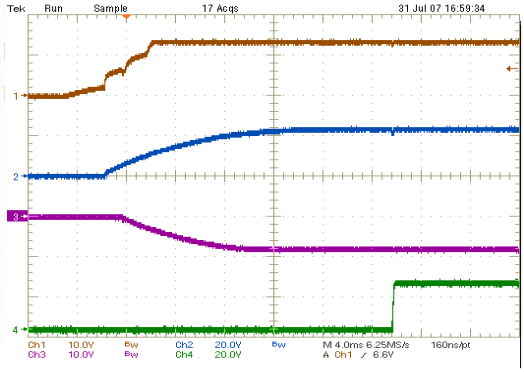
V_{MAIN} Regulator Soft-Start(Heavy Load)



CH1=V_{IN} CH2=V_{MAIN}

CH3=Inductor Current

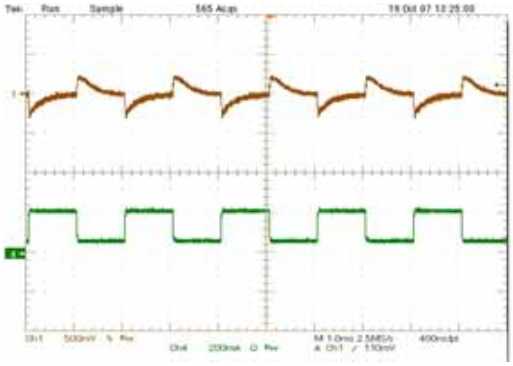
Power-Up Sequence



CH1=V_{MAIN} CH2=VP

CH3=V_{GOFF} CH4=V_{GON}

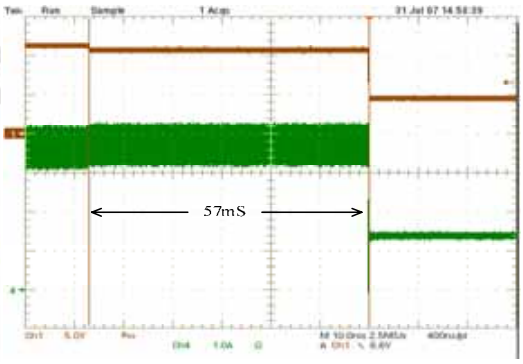
V_{MAIN} Regulator Pulsed VS. Load-Transient Response



CH1=V_{MAIN} , AC-Coupled

CH4=Load Current

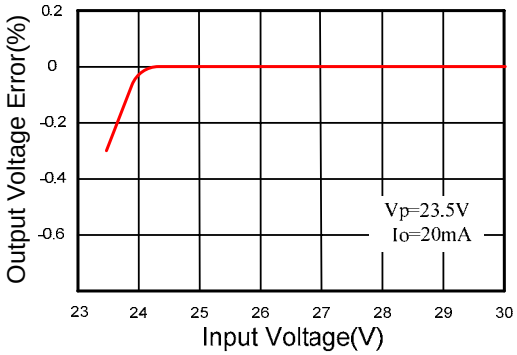
Timer Delay Latch Response To Overload



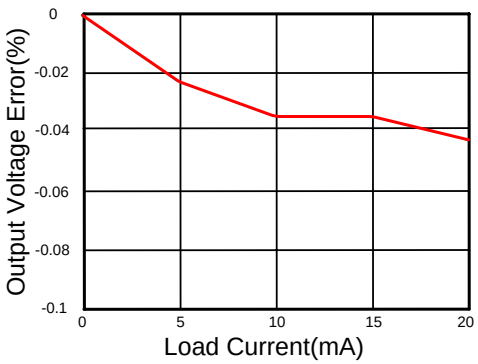
CH1=V_{MAIN}

CH4=Inductor Current

Gate-On Regulator Line Regulation



Gate-On Regulator Load Regulation



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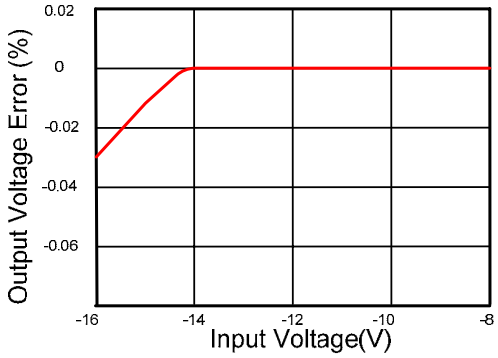
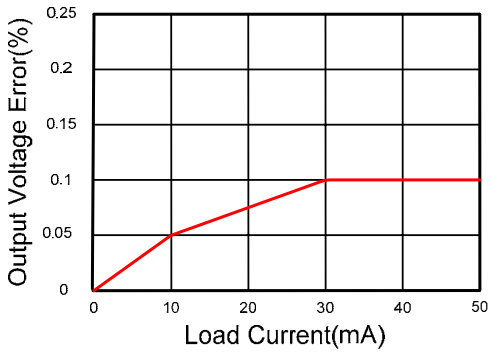
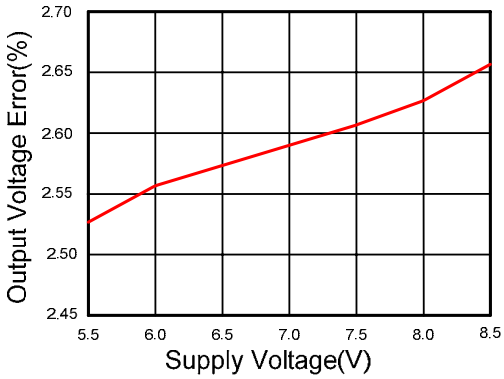
Gate-Off Regulator Line Regulation



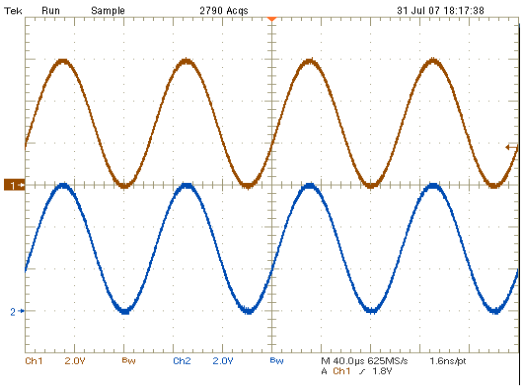
Gate-Off Regulator Line Regulation



Operational - Amplifier
Supply Current VS. Supply Voltage

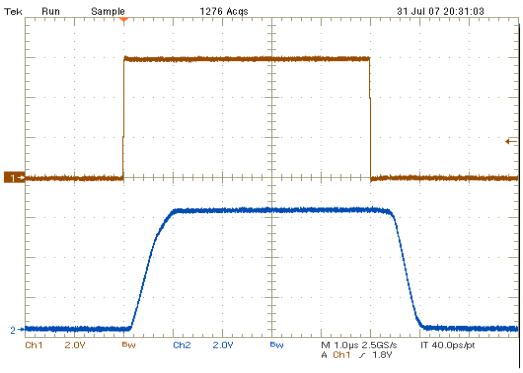


Operational - Amplifier
Rail-To-Rail Input/Output

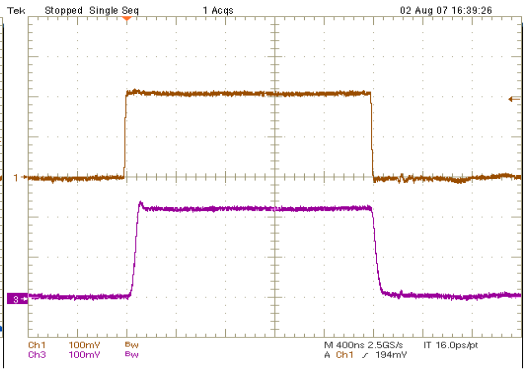


CH1=Input Signal CH2=Output Signal

Operational – Amplifier
Large-Signal Step Response



Operational – Amplifier
Small-Signal Step Response



CH1=Input Signal CH2=Output Signal CH1=Input Signal CH2=Output Signal

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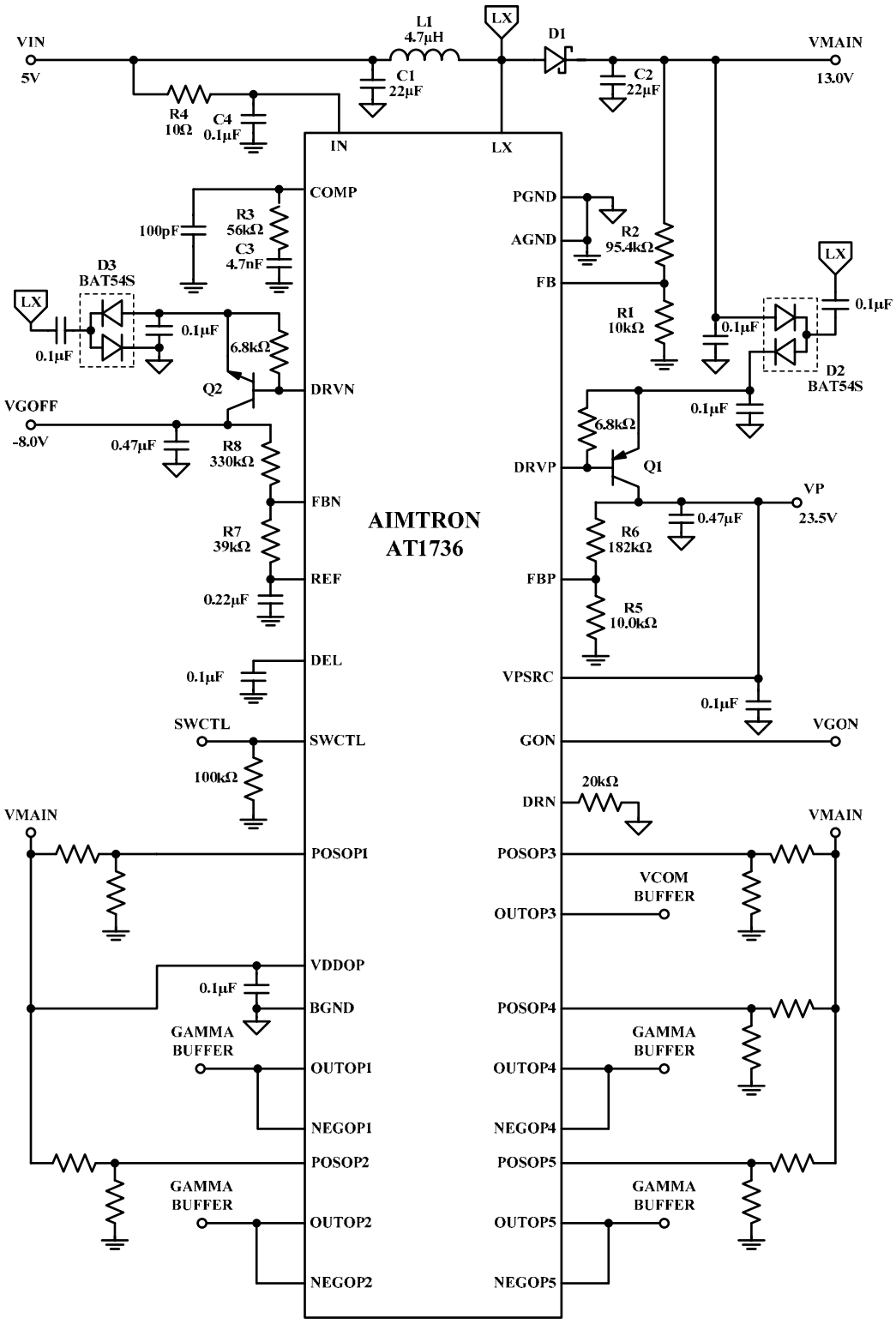
Typical Application Circuit



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Function Description

The AT1736 consists of a high-performance step-up converter, two linear regulator controllers, five high-current operational amplifiers, and a gate-on pulse modulator. The step-up DC-DC converter generates the source-driver supply voltage. The two linear regulator controllers provide the regulated positive gate-on and negative gate-off supply voltages from external charge pumps. The operational amplifiers supply the VCOM and GAMMA buffers with high output current, fast slew rate and wide bandwidth performances for driving capacitive loads. The gate-on pulse modulator controls the positive gate-on voltage waveform for reducing the flicker on TFT LCD panel.

Step-up Converter

The step-up DC-DC converter adopts the PWM current mode control, fixed 1.2MHz switching frequency and an internal 2.4A, 0.16Ω (typical) power MOSFET. Such architecture provides faster line and load transient response for the specific performance of the source-driver supply voltage source. The high switching frequency can minimize the components as the space of thick LCD panel required. The internal soft-start function uses 8 steps digital current limit to restrain the inrush current and output voltage overshoot and also to reduce the pin number of the chip and the external component. The external compensation network provides the flexibility in determining output voltage regulation accuracy and dynamic response.

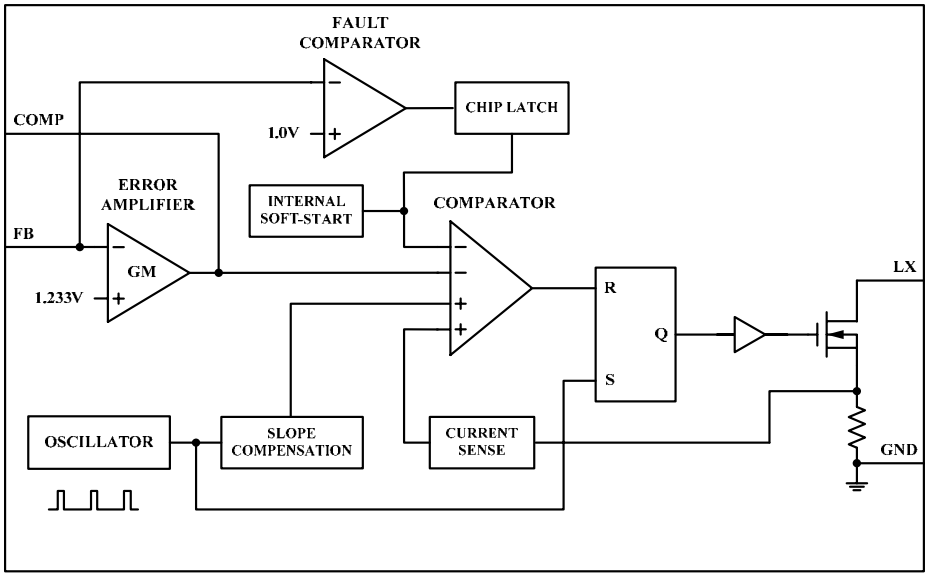

Figure 1. Step-up converter block diagram

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Positive Gate-On Linear Regulator Controller

The positive gate-on linear regulator controller consists of FBP and DRVP pins. Use FBP to determine the positive gate-on output voltage. The DRVP pin is an open-drain n-channel MOSFET to drive an external pnp transistor. A 6.8kΩ resistor connected from base to emitter of the external transistor and a 0.47μF output capacitor are recommended. The driving sink current is at least 1 mA for the design of 20mA output current. The internal soft-start function adopts rising its reference voltage in the 128 steps (7 bits) to restrain the inrush current and output voltage overshoot.

If the applications where the charge-pump output voltage is over 28V, an external NPN transistor needs to be inserted in between the DRVP pin and the based of transistor Q1, or the linear regulator can control the VMAIN and regulate the final charge pump output as shown in Fig. 2.

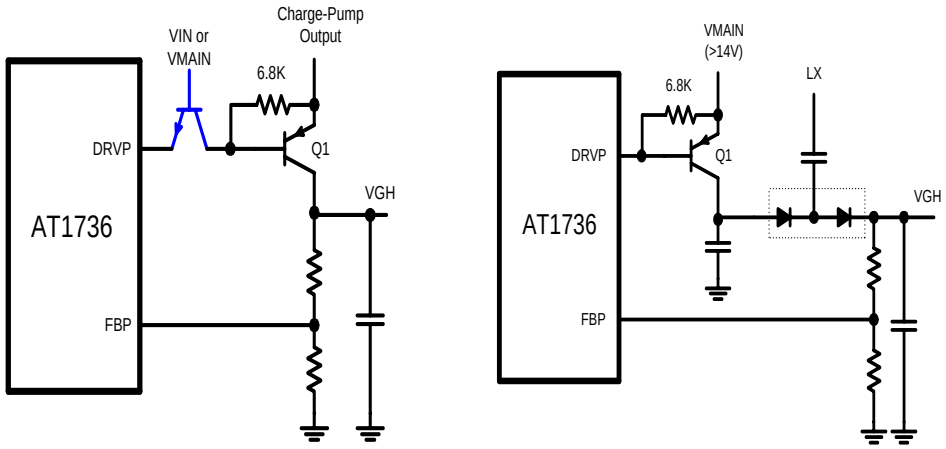

Figure 2. High Charge-Pump output Application Circuit

Negative Gate-Off Linear Regulator Controller

The negative gate-off linear regulator controller consists of FBN and DRVN pins. Use FBN to determine the negative gate-off output voltage. The DRVN pin is an open-drain p-channel MOSFET to drive an external npn transistor. A 6.8kΩ resistor connected from base to emitter of the external transistor and a 0.22μF output capacitor are recommended. The driving source current is at least 1 mA for the design of 20mA output current. The internal soft-start function adopts decreasing its reference voltage from V_{REF} to 250mV in the 128 steps (7 bits) to restrain the inrush current and output voltage overshoot.

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Output Voltage Fault Protection

After soft-start period, if the feedback voltage of the step-up DC-DC converter or any of the linear regulators does not exceed its fault-detection threshold, the AT1736 enables the internal fault timer. If the fault condition exceeds the fault-timer duration (200ms typical), then the AT1736 shuts down all the outputs except the reference. Once the fault condition is removed, cycle the input voltage (below the UVLO falling threshold) to reactivate the chip.

Reference Voltage

The reference output voltage is typical 1.233V and the source ability is at least 50μA. Connecting a 0.22μF bypass ceramic capacitor between REF and GND is recommended.

Gate-On Pulse Modulator

The AT1736 includes a gate-on pulse modulator to control gate-on voltage waveform to reduce the flicker on TFT LCD panel. After the V_{IN} exceeds UVLO, all the soft-start periods are complete, fault conditions do not exist, and the V_{DLP} exceeds the turn-on threshold, the gate-on pulse modulator start to be active and is controlled by SWCTL. There are two high voltage switches Q1 and Q2 connecting to GON. Another terminal of Q1 is connected to positive charge-pump output for the positive high voltage input (VPSRC), and Q2 is connected to DRN with an external series resistor to ground for discharging the positive gate-on voltage. If SWCTL is high, Q1 turns on and Q2 turns off. If SWCTL is low, Q1 turns off and Q2 turns on.

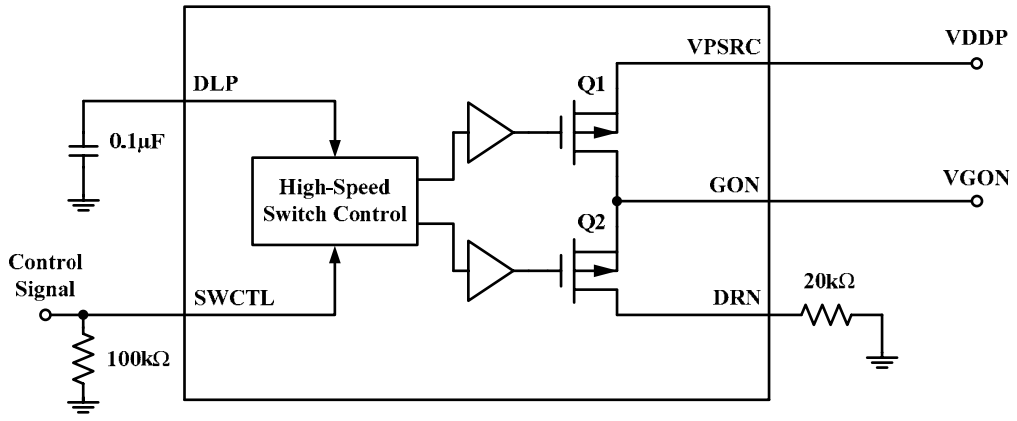

Figure 3. Gate-on pulse modulator

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Power-Up Sequence

The AT1736 goes through start-up sequence after power-up. When V_{IN} exceeds UVLO threshold, the reference voltage starts to rise. After reference voltage reaches regulation, the step-up converter and linear regulators will start up with the soft-start procedure.

Once the FB voltage reaches the reference voltage, the gate-on pulse modulator delay block is also enabled. The gate-on pulse modulator is enabled after the V_{DLP} goes above V_{REF} with a constant charging current (5μA typical). Connect an appropriate capacitor between DLP and GND to obtain the required delay-time.

$$C_{DLP} = T_{DELAY} \times \frac{5.0\mu A}{V_{REF}}$$

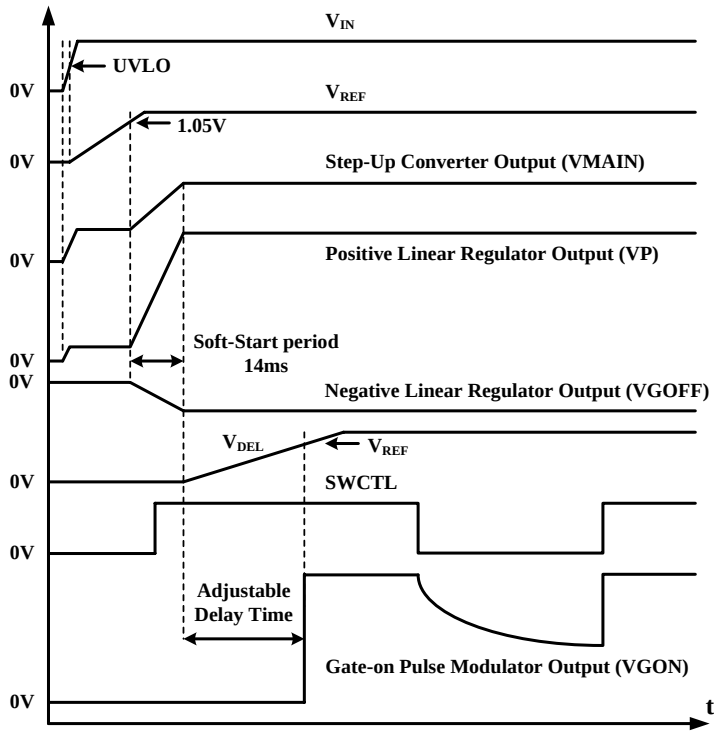

Figure 3. Power-up sequence

Operational Amplifier

These five identical operational amplifiers have the excellent performances as high output current (150mA), fast slew rate (13V/μs), and wide bandwidth (12MHz) to drive the distributed series capacitance and resistance of the TFT LCD backplane.

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Output Voltages Setting

The output voltages of step-up converter and linear regulators are set by each resistive voltage-divider as the Typical Application Circuit shown.

The AT1736 applies a 1.233V feedback reference voltage at FBL pin of linear regulator, and the output voltage setting is according to the following equation:

$$V_{VMAIN} = 1.233 \times \left(1 + \frac{R2}{R1}\right) \text{ (V)}$$

The feedback reference voltage of positive charge-pump V_{FBP} is typical 1.233V. The output voltage is set by the following equation:

$$V_{VP} = 1.233 \times \left(1 + \frac{R6}{R5}\right) \text{ (V)}$$

The feedback reference voltage of negative charge-pump V_{FBN} is typical 250mV, and the reference voltage (V_{REF}) is typical 1.233V. So the output voltage is set by the following equation:

$$V_{VGOFF} = 0.25 - \left(\frac{0.983 \times R8}{R7}\right) \text{ (V)}$$

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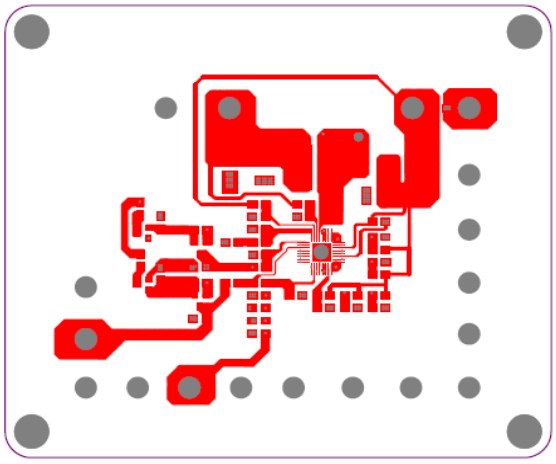
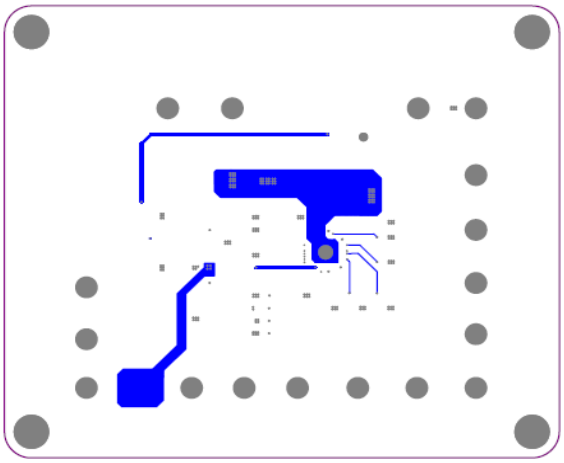
PC Board Layout

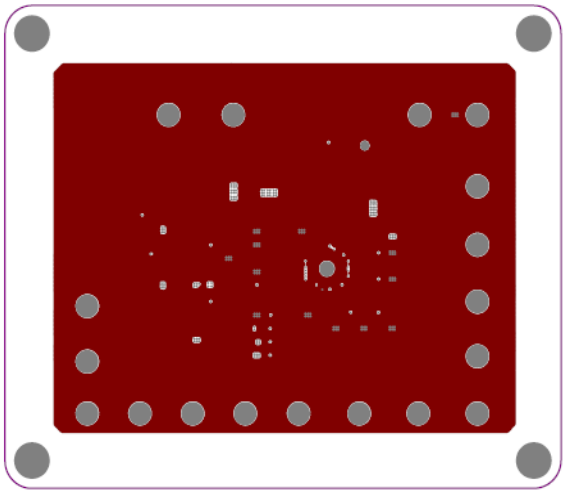
1. The most critical aspect of the layout is the placements of the input bypass capacitors of pin IN, VDDOP, VPSRC and REF. They must be placed as close as possible to the AT1736 to reduce the input ripple voltage and noise coupling.
2. Power loops on the input and output of the converters should be connected with the shortest and widest traces as possible. The long and narrow trace increases the ESR and ESL, and that will induce more effective noise at high frequency easily.
3. The feedback resistors should connect to FB pins as close as possible. And each route connected to output should be away from the switching noise source, such as charge-pump and step-up converter power loops.
4. Separate the power ground and analog signal ground into different planes to prevent the interference, and connect these two parts at the VMAIN output ground.



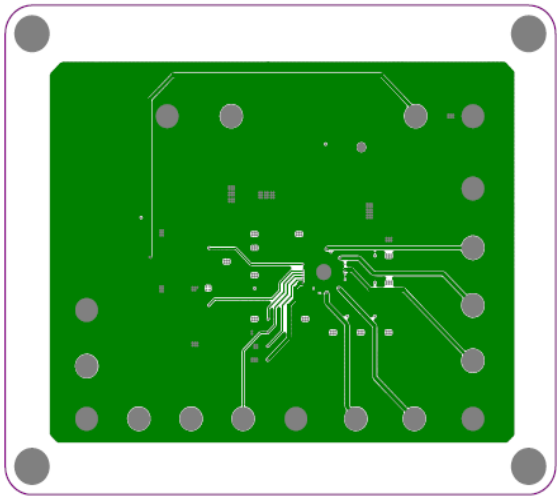
Top-layer



Bottom-layer



Middle ground layer 1



Middle ground layer 2

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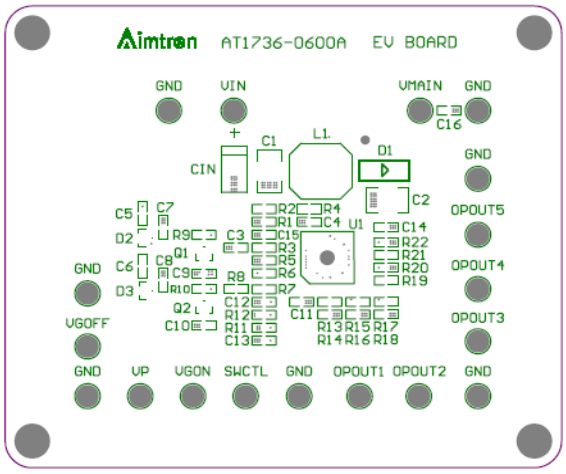

Component side

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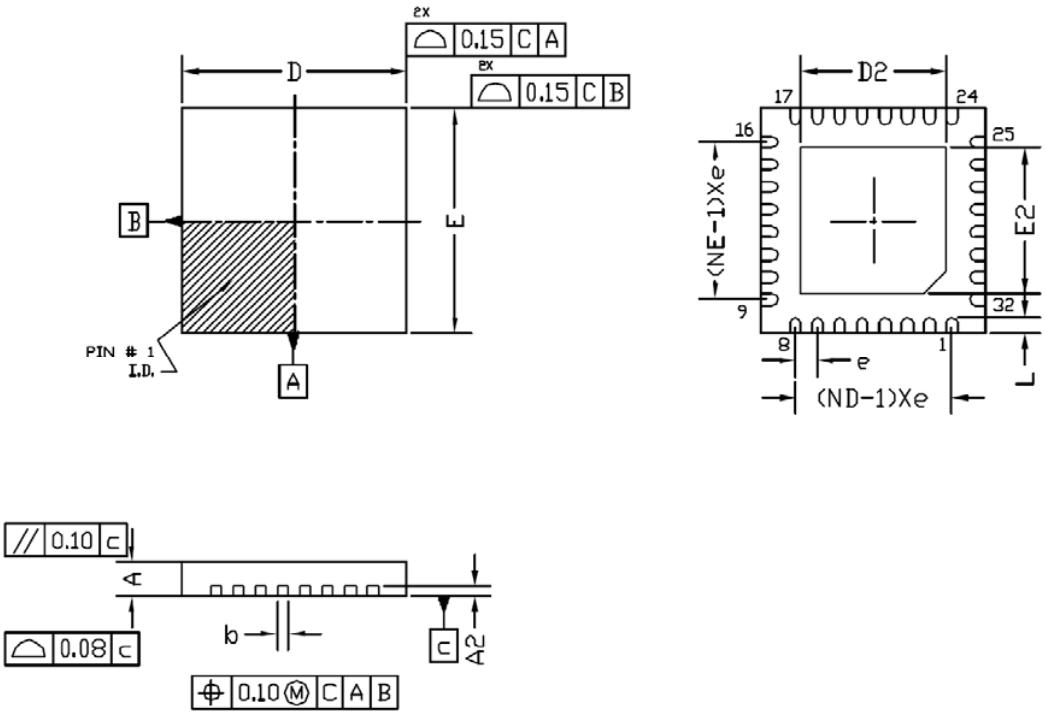
Package Outline: Thin QFN-32



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.027	0.029	0.031
A2	0.200 REF.			0.0078 REF.		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	3.05	3.15	3.25	0.120	0.124	0.128
e	0.50 TYP			0.020 TYP		
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	3.05	3.15	3.25	0.120	0.124	0.128
L	0.30	0.40	0.50	0.012	0.016	0.020

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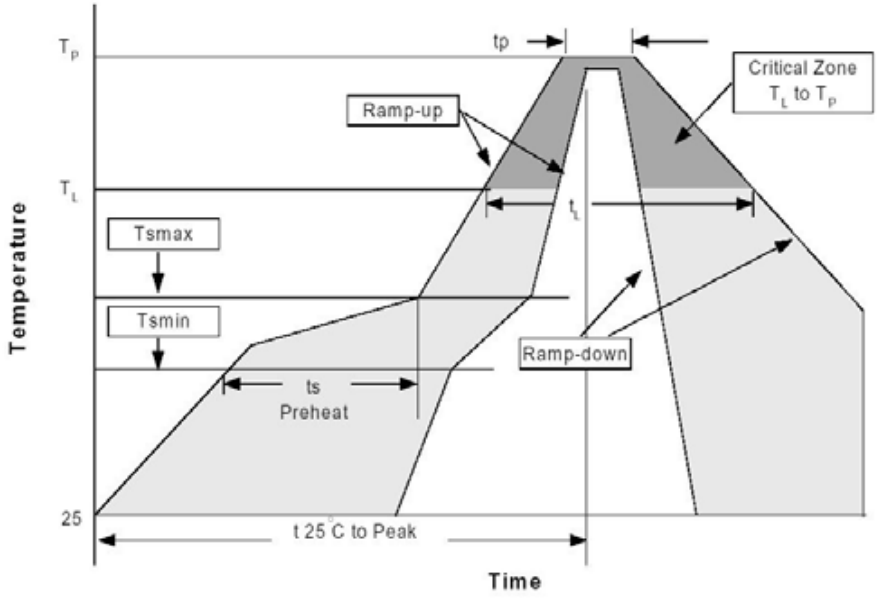
Reflow Profiles



Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm^3	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm^3**	**Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm^3**	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm^3**
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat -Temperature Min(Tsmin) -Temperature Max (Tsmax) -Time (min to max)(ts)	100°C 150°C 60-120 seconds		150°C 200°C 60-180 seconds	
Tsmax to T_L -Ramp-up Rate			3°C/second max.	
Time maintained above: -Temperature (T_L) -Time (t_L)	183°C 60-150 seconds		217°C 60-150 seconds	
Peak Temperature(T_P)	225+0/-5°C	240+0/-5°C	245+0/-5°C	250+0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

***All temperatures refer to topside of the package, measured on the package body surface.**

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