Aimtron
圓創科技股份有限公司

LCD Panel Power Supplies with Low-Cost Linear-Regulator, Charge-Pumps and High-Current OP

Features

- High-Performance Linear Regulator:
  - 1.6% Output Accuracy
  - Works with Small Ceramic Output Capacitors
  - Fast Transient Response
  - Foldback Current Limit
- High-Current Operational Amplifier:
  - 12V/µs Slew Rate
  - 12MHz, -3dB Bandwidth
  - Rail-to-Rail Inputs/Output
- 100mA Negative Charge Pump Regulator
- 50mA Positive Charge Pump Regulator with Adjustable Delay
- Built-In Power-Up Sequence
- Gate-on Pulse Modulator for Sequence & Discharge Control
- Thermal Protection
- Latched Fault Protection with Timer

Applications

- LCD Monitor Panel Modules
- LCD TV Panel Modules

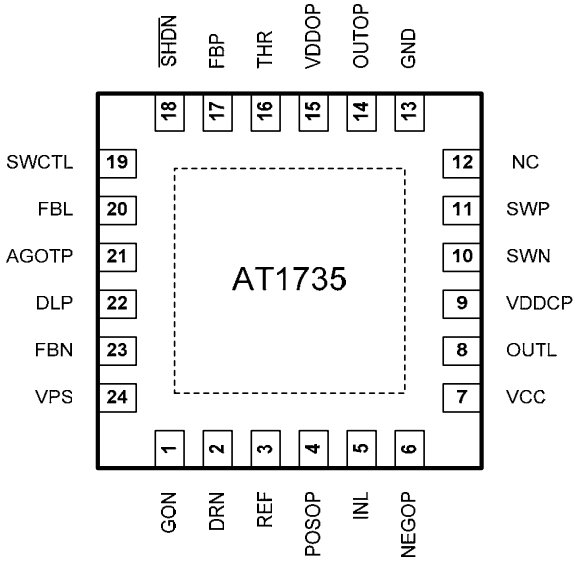
General Description

AT1735 provides a complete linear- regulator power supply solution for TFT LCD panels. AT1735 incorporates a high-performance linear regulator, two low-power charge-pump regulators, a high-current operational amplifier, and logic-controlled gate-on pulse modulator to control the positive charge-pump output sequence and waveform.

The linear regulator generates the source-driver supply voltage from the input voltage directly. The two charge-pump regulators generate the positive gate-on and negative gate-off supply voltages. The operational amplifier supplies the VCOM buffer with high output current, fast slew rate and wide bandwidth performances for driving capacitive loads. The gate-on pulse modulator control (SWCTL) is independent of the $\overline{\text{SHDN}}$ chip enable control.

The AT1735 adopts a 24-pin thin QFN package which is 4mm x 4mm with a maximum thickness of 0.8mm for ultra-thin LCD panel application.

Pin Configuration

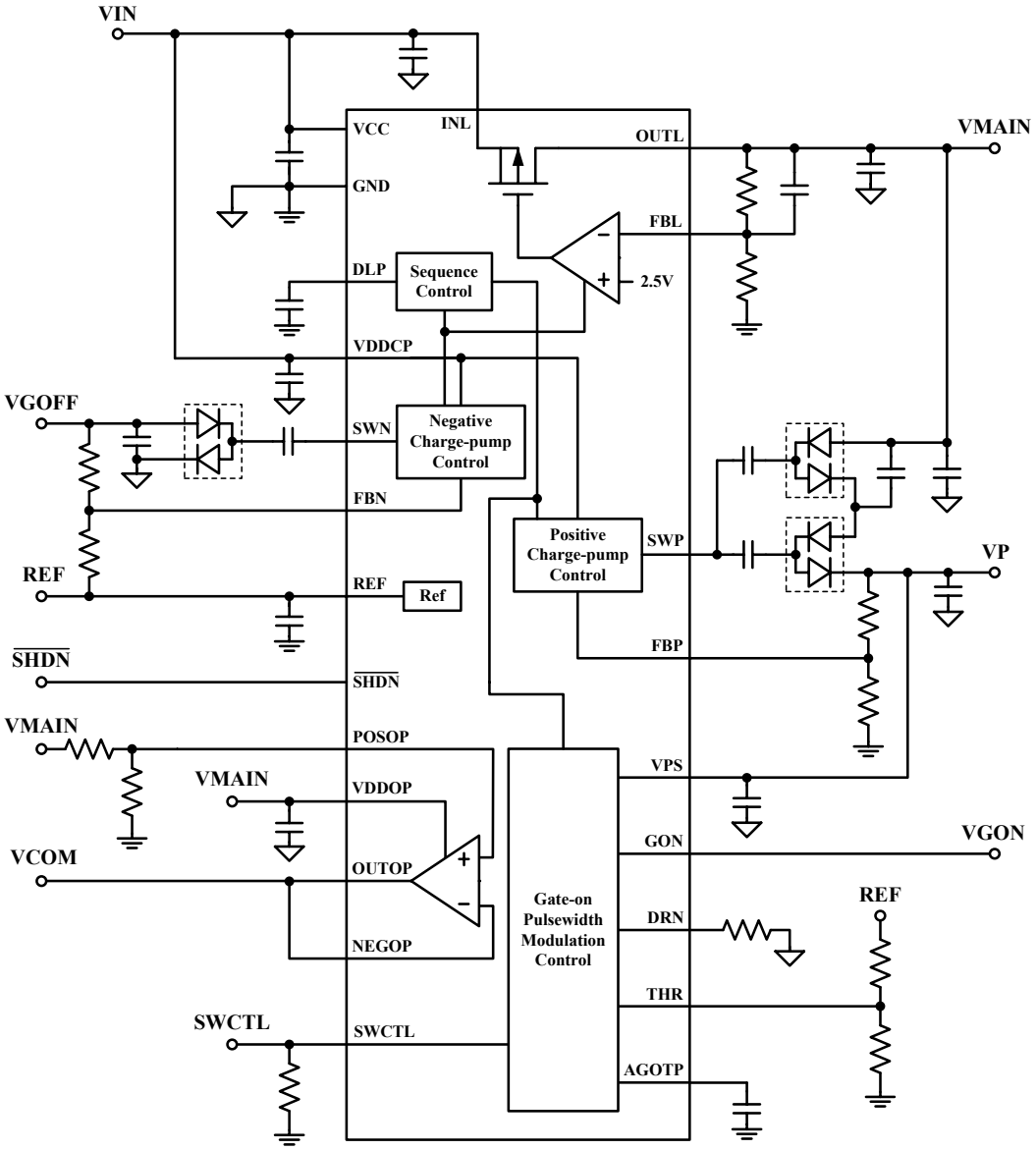


Aimtron reserves the right without notice to change this circuitry and specifications.

Ordering Information

Part number	Package	Marking
AT1735N_GRE	Thin QFN24, Green	AT1735N

Block Diagram



Pin Descriptions

Pin No.	Pin Name	Function
1	GON	Internal High-Voltage MOSFET Switch Output Terminal for Gate-on Voltage Supply.
2	DRN	Discharge Switch Input. Connect a resistor to GND to discharge the V_{GON} when SWCTL is low.
3	REF	Reference Output. Connect a 0.22µF capacitor from REF to GND. REF remains on in shutdown.
4	POSOP	Operational Amplifier Noninverting Input.
5	INL	Linear Regulator Input.
6	NEGOP	Operational Amplifier Inverting Input.
7	VCC	IC Supply Input. Connect VCC to GND with a 0.1µF bypass capacitor.
8	OUTL	Linear Regulator Output.
9	VDDCP	Supply Input for the Charge-Pump Regulators. Connect a 0.1µF bypass capacitor from VDDCP to GND.
10	SWN	Negative Charge-Pump Driver Output. Output high level is VDDCP, and output low level is GND. SWN is internally pulled to VDDCP in shutdown.
11	SWP	Positive Charge-Pump Driver Output. Output high level is VDDCP, and output low level is GND. SWP is internally pulled to GND in shutdown.
12	NC	No Connect.
13	GND	Ground.
14	OUTOP	Operational-Amplifier Output.
15	VDDOP	Operational-Amplifier Supply Input. Connect VDDOP to GND with a 0.1µF bypass capacitor.
16	THR	GON Voltage Low-Level Regulation Set-Point Input. Connect THR to the center of a resistive voltage-divider between REF and GND to set the low-level V_{GON} regulation level. The threshold voltage is $10 \times V_{THR}$.
17	FBP	Positive Charge-Pump Feedback Input. Place the voltage-divider to IC as close as possible.
18	$\overline{SHDN}$	Active-Low Shutdown Control Input. Pull $\overline{SHDN}$ low to turn off all sections of the device except REF. Pull $\overline{SHDN}$ high to enable the device. Cycle $\overline{SHDN}$ to reset the device after a fault.
19	SWCTL	Gate-on Pulse Modulator Timing Control Input.
20	FBL	Linear-Regulator Feedback Input. Place the voltage-divider to IC as close as possible.
21	AGOTP	Adjustable Gate-on Time Pulsewidth Modulator Input. AGOTP is high impedance when it is connected to REF. Connect a capacitor to GND to extend the Gate-on ON time.
22	DLP	Positive Charge-Pump Start-up Delay and Gate-on Pulse Modulator Delay Input. Connect a capacitor from DLP to GND to set the delay time. A 5µA current source charges C_{DLP}.
23	FBN	Negative Charge-Pump Feedback Input. Place the voltage-divider to IC as close as possible.
24	VPS	Gate-on Pulse Modulator Voltage Supply Input. Source of the internal high-voltage P-channel MOSFET connected to GON.

Absolute Maximum Ratings (Ta = 25℃)

Parameter	Rated Value		Unit
	Min.	Max.	
SWCTL, FBL, FBP, FBN, $\overline{SHDN}$, REF, THR	-0.3	+6.0	V
AGOTP, DLP	-0.3	+6.0	V
VCC, INL, OUTL	-0.3	+18.0	V
VDDCP, VDDOP	-0.3	+18.0	V
POSOP, NEGOP, OUTOP	-0.3	+18.0	V
SWP, SWN	-0.3	+18.0	V
VPS, GON, DRN	-0.3	+30.0	V
DRN to GON	-30.0	+30.0	V
OUTOP Maximum Continuous Output Current	-40.0	+75.0	mA
Power Dissipation (Ta≦25℃)	-	1349	mW
Operating Temperature	-35	+85	^{0}C
Storage Temperature	-55	+150	^{0}C
Lead Temperature (Soldering, 10s)	-	+300	^{0}C
ESD Susceptibility (MM)	-200	200	V
ESD Susceptibility (HBM)	-2	2	KV

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Devices are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Recommended Operating Conditions

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{VCC}	8	-	18	V
Operating Temperature*	T_{OP}	-20	+25	+85	°C
Operating Junction Temperature	T_J	-	-	+150	°C

***Using X5R or X7R capacitors.**

Electrical Characteristics

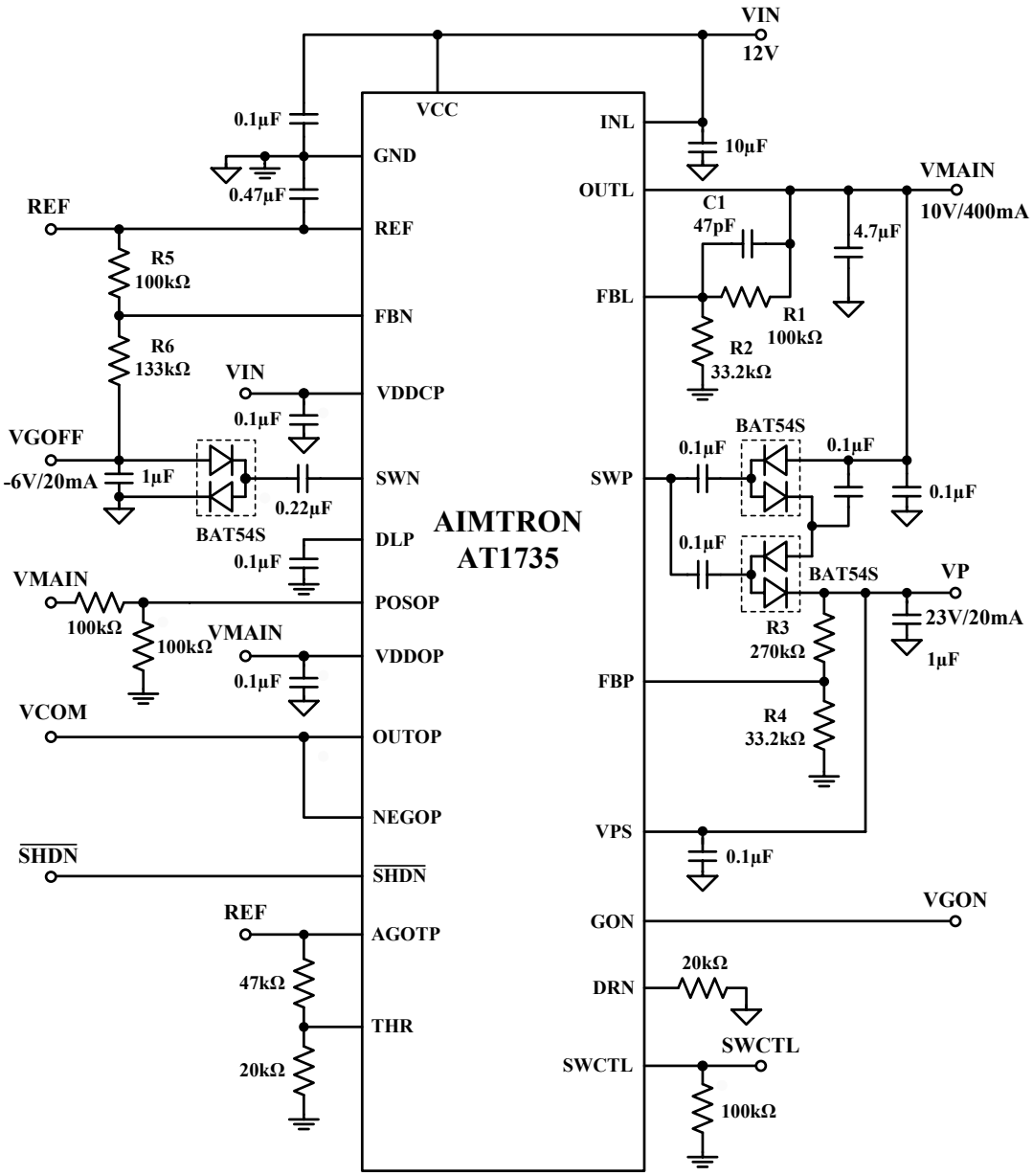
(Test circuit is shown as Typical Application Circuit, unless otherwise noted. VCC = V_{INL} = V_{VDDCP} = 12V, V_{OUTL} = V_{VDDOP} = 10V, V_{VPS} = 23V, Ta=+25°C.)

Parameter	Condition	Values			Unit
		Min.	Typ.	Max.	
VCC Operating Supply Range		8		18	V
VCC Quiescent Current	$\overline{SHDN}$ = GND		0.7	0.9	mA
	$\overline{SHDN}$ = 3.3V			2.5	
Duration to Trigger Fault Condition			44		ms
REF Output Voltage	-10μA < I_{REF} < 1mA* (excluding internal load)	4.9	5.0	5.1	V
VDDCP Input Supply Range		2.7		18	V
Charge-Pump Regulators Operating Frequency		1275	1500	1725	kHz
Thermal Shutdown	Rising temperature, 15°C hysteresis		+160		°C
Linear Regulator Section					
INL Operation Supply Range	V_{OUTL} < V_{INL}	7		18	V
Dropout Voltage	I_{OUTL} = 200mA		200		mV
FBL Regulation Voltage	I_{OUTL} = 50mA	2.46	2.50	2.54	V
FBL Input Bias Current	V_{FBL} = 2.5V			50	nA
FBL Fault Trip Level (UVP)	Falling edge	1.85	2.00	2.15	V
FBL Line-Regulation Error	V_{INL} = VCC = 10.8V~13.2V, V_{OUTL} = 10V, I_{OUTL} = 50mA			15	mV
	V_{INL} = VCC = 11V~20V, V_{OUTL} = 10V, I_{OUTL} = 50mA		10		
Bandwidth	Guaranteed by design	1000			kHz
Maximum OUTL Current	V_{FBL} = 2.4V	500			mA
OUTL Soft-Start Period			2.73		ms
OUTL Load Regulation	VCC = 12V, 5mA < I_{OUTL} < 500mA			2	%
Operational Amplifier Section					
VDDOP Supply Operating Range		4.5		16	V
VDDOP Supply Current	Buffer configuration, V_{POSOP} = 4V, no load		1.0	1.5	mA
Input Offset Voltage	(V_{NEGOP}, V_{POSOP}) = V_{VDDOP} / 2, TA = +25°C	-16	0	16	mV
Input Bias Current	(V_{NEGOP}, V_{POSOP}) = V_{VDDOP} / 2	-50	+1	+50	nA
Common-Mode Input Range	V_{NEGOP}, V_{POSOP}	0		V_{VDDOP}	V

Common-Mode Rejection Ratio	0 ≦(V_{NEGOP}, V_{POSOP}) < V_{VDDOP}	50	90		dB
Open-Loop Gain			125		dB
Output Voltage Swing High	I_{OUTOP} = 100µA	V_{VDDOP} -15	V_{VDDOP} - 8		mV
	I_{OUTOP} = 5mA	V_{VDDOP} -150	V_{VDDOP} - 110		
Output Voltage Swing Low	I_{OUTOP} = -100µA		20	35	mV
	I_{OUTOP} = -5mA		200	250	
Short-Circuit Current	Short to V_{VDDOP} / 2, sourcing	50	125		mA
	Short to V_{VDDOP} / 2, sinking	50	66		
Output Current	Buffer configuration, V_{POSOP} = 4V, V_{OUTOP} error < ±10mV	-40		+80	mA
Power-Supply Rejection Ratio	6V ≦V_{VDDOP} ≦13.2V, DC (V_{NEGOP}, V_{POSOP}) = V_{VDDOP} / 2	60	100		dB
Slew Rate			12		V/µs
-3dB Bandwidth	Buffer configuration, R_L = 10kΩ, C_L = 10pF		12		MHz
Gain-Bandwidth Product	Buffer configuration, R_L = 10kΩ, C_L = 10pF		8		MHz
Positive Charge-Pump Regulator Section					
FBP Regulation Voltage	I_{GON} = 10mA	2.425	2.500	2.575	V
FBP Line-Regulation Error	V_{OUTL} (V_{VDDCP}) = 10.8V~13.2V, V_{GON} = 23V, I_{GON} = 20mA			25	mV
FBP Input Bias Current	V_{FBP} = 2.5V	-50		+50	nA
SWP P-Channel On-Resistance			15	30	Ω
SWP N-Channel On-Resistance	V_{FBP} = 2.4V		6	12	Ω
	V_{FBP} = 2.6V	20			kΩ
FBP Fault Trip Level (UVP)	Falling edge	1.85	2.00	2.15	V
Positive Charge-Pump Soft-Start Period			2.73		ms
Negative Charge-Pump Regulator Section					
FBN Regulation Voltage	I_{GOFF} = -10mA	200	250	300	mV
FBN Line-Regulation Error	V_{OUTL} (V_{VDDCP}) = 10.8V~13.2V, V_{GOFF} = -6V, I_{GOFF} = -50mA			25	mV
FBN Input Bias Current	V_{FBN} = 250mV	-50		+50	nA
SWN P-Channel On-Resistance			3	6	Ω
SWN N-Channel On-Resistance	V_{FBN} = 350mV		1.5	3	Ω
	V_{FBN} = 150mV	20			kΩ
FBN Fault Trip Level	Rising edge		700		mV
Negative Charge-Pump Soft-Start Period			2.73		ms
Sequence Control Section					

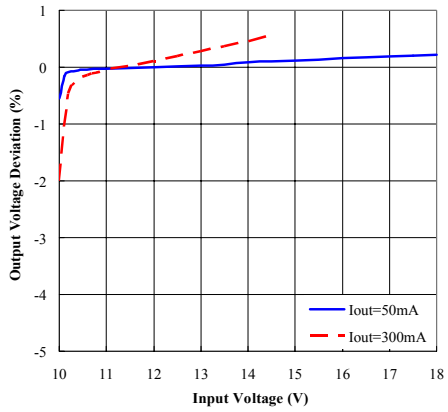
$\overline{SHDN}$ Input Low Voltage				0.8	V
$\overline{SHDN}$ Input High Voltage		1.4			V
$\overline{SHDN}$ Input Current				2.5	µA
DLP Capacitor Charge Current	During startup, V_{DLP} = 1.0V	3.8	5	6.2	µA
DLP Turn-On Threshold		2.375	2.5	2.625	V
Pin Discharge Switch On-Resistance	$\overline{SHDN}$ = low or fault tripped; DLP, FBP, FBN to GND		60		Ω
	$\overline{SHDN}$ = low or fault tripped; OUTL, OUTOP to GND)		1.3		kΩ
	SWCTL=high, V_{AGOPT} = V_{REF} /2 ; AGOTP to GND		1.3		kΩ
Gate-on Pulse Modulator Section					
SWCTL Input Low Voltage				1.0	V
SWCTL Input High Voltage		1.4			V
SWCTL Input Leakage Current		-1		+1	µA
SWCTL to GON Rising Propagation Delay	V_{AGOPT} = V_{REF}, 1.5nF from GON to GND, V_{SWCTL} = 0V to 3V step, no load on GON, measured from V_{SWCTL} = 1.5V to GON = 20%		50		ns
SWCTL to GON Falling Propagation Delay	V_{AGOPT} = V_{REF}, 1.5nF from GON to GND, V_{SWCTL} = 3V to 0V step, DRN falling, no load on DRN and GON, measured from V_{SWCTL} = 1.5V to GON = 80%		50		ns
VPS Input Voltage Range				30	V
VPS Input Current	V_{AGOPT}= V_{REF}, V_{DLP}= V_{REF}, SWCTL=high		80		µA
DRN Input Current	V_{AGOPT}= V_{REF}, V_{DRN}=8V, V_{DLP}= V_{REF}, SWCTL= low		80	120	µA
VPS to GON Switch On-Resistance	V_{AGOPT}= V_{REF}, V_{DLP}= V_{REF}, SWCTL=high		15	30	Ω
DRN to GON Switch On-Resistance	V_{AGOPT}= V_{REF}, V_{DLP}= V_{REF}, SWCTL =low		30		Ω
AGOTP Capacitor Charge-Current			50		µA
AGOTP Voltage Threshold for Enabling DRN Switch Control		2.3	2.5	2.7	V
AGOTP Current-Source Stop Voltage Threshold	V_{AGOTP} rising edge	3.3	3.5	3.7	V
THR to GON Voltage Gain			10		V/V
GON Falling Slew Rate			13.5		V/µs

Typical Application Circuit

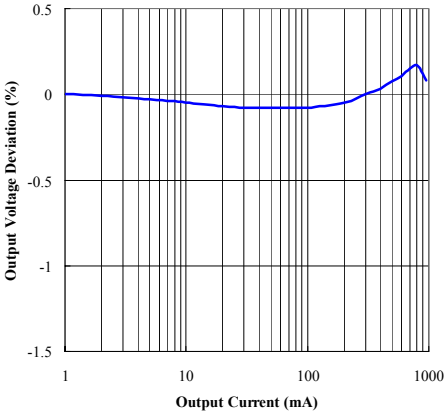


Typical Characteristics

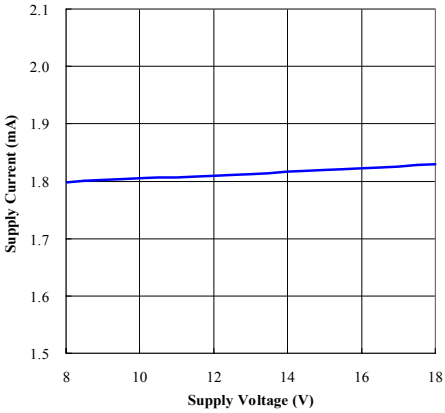
Linear Regulator Line Regulation



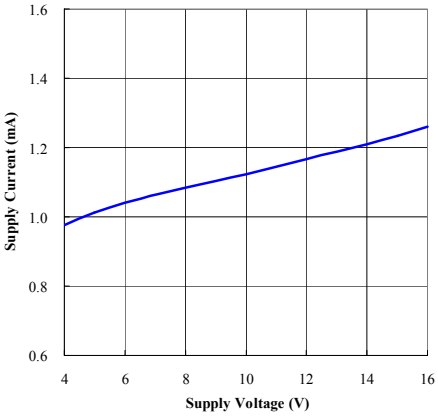
Linear Regulator Load Regulation



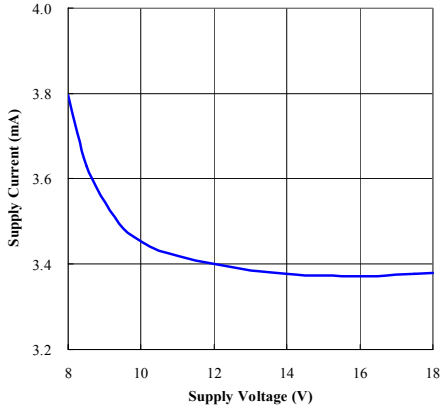
VCC No-load Supply Current vs. Supply Voltage



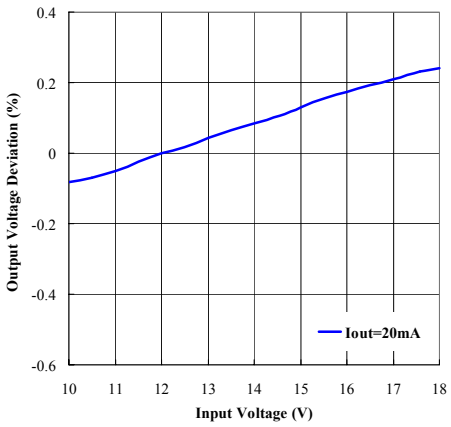
VDDOP No-load Supply Current vs. Supply Voltage



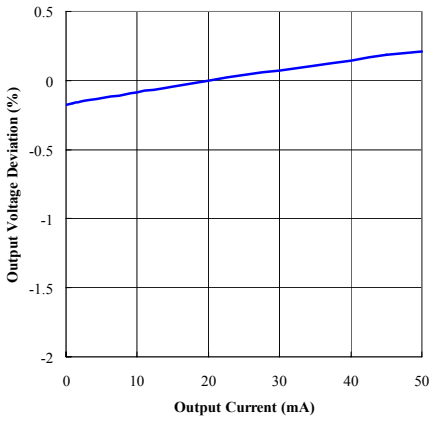
VDDCP No-load Supply Current vs. Supply Voltage



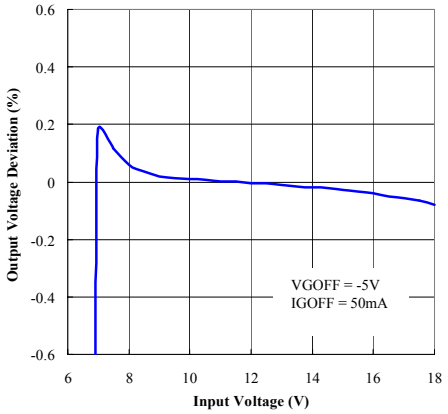
Positive Charge-pump Line Regulation



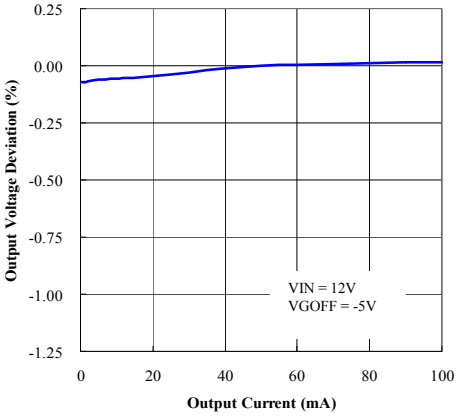
Positive Charge-pump Load Regulation



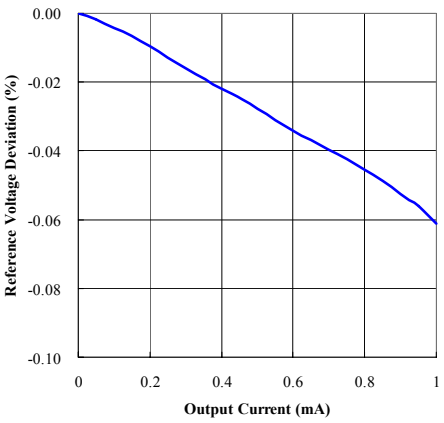
Negative Charge-pump Line Regulation



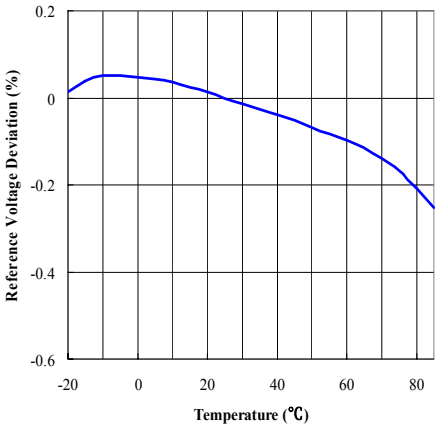
Negative Charge-pump Load Regulation



Reference Load Regulation



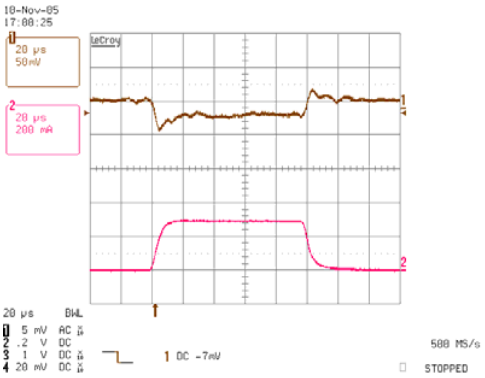
Reference Voltage vs. Temperature



(Test circuit is shown as Typical Application Circuit, unless otherwise noted. VCC = V_{INL} = V_{VDDCP} =

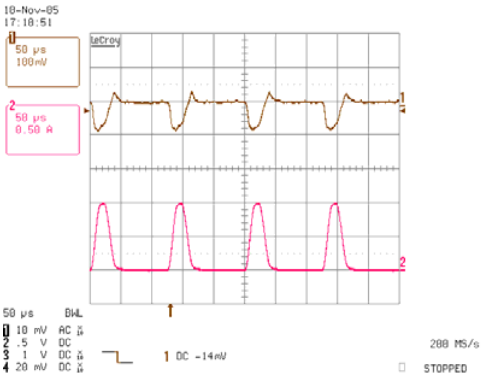
12V, V_{OUTL} = V_{VDDOP} = 10V, V_{VPS} = 23V, Ta=+25℃.)

Load Transient Response



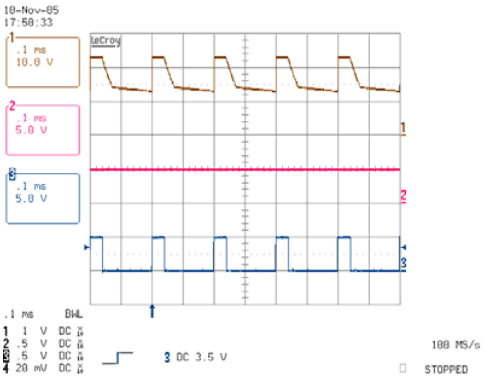
CH1: V_{OUTL}
CH2: I_{OUTL} = 0 to 300mA

Load Transient Response



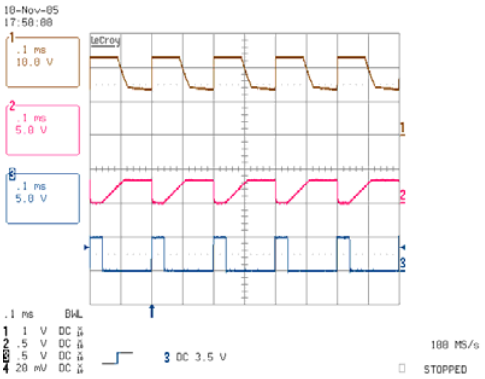
CH1: V_{OUTL}
CH2: I_{OUTL} = 0 to 1A

VGON Pulsewidth Modulation Control



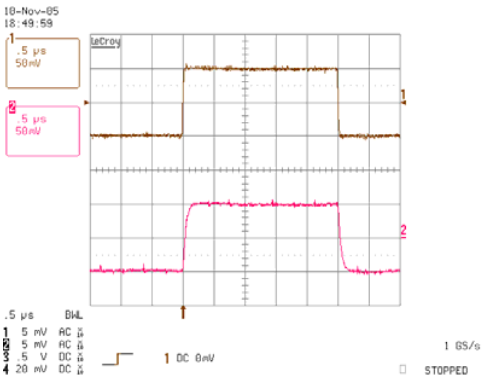
CH1: VGON CH3: SWCTL
CH2: AGOTP

VGON Pulsewidth Modulation Control



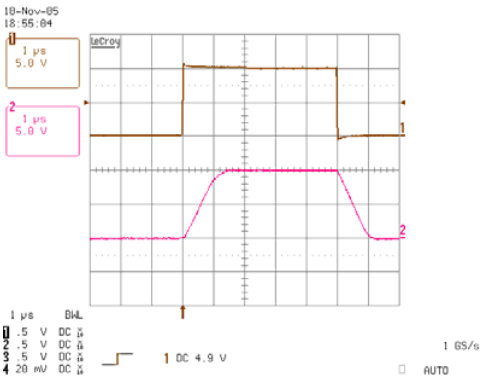
CH1: VGON CH3: SWCTL
CH2: AGOTP

OP Amp Small-signal Response



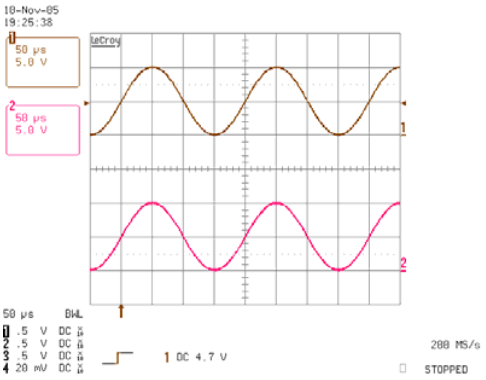
CH1: V_{POSOP}
CH2: V_{OUTOP}

OP Amp Large-signal Response



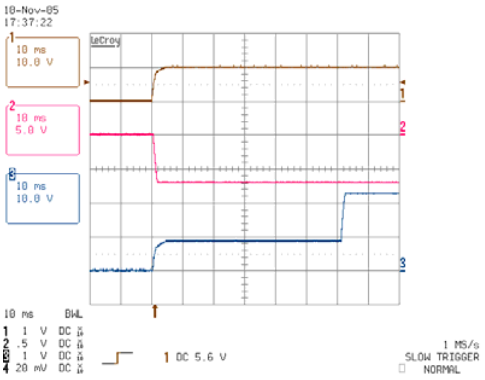
CH1: V_{POSOP}
CH2: V_{OUTOP}

OP Amp Input & Output



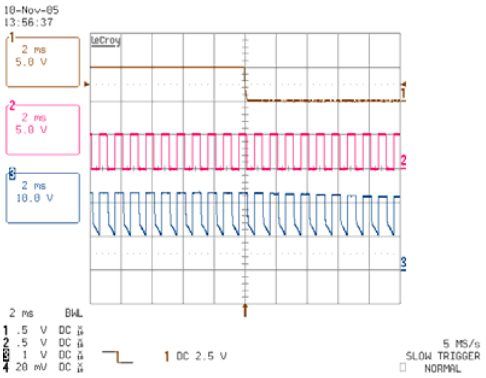
CH1: V_{POSOP}
CH2: V_{OUTOP}

Power–up Sequence



CH1: VMAIN CH3: VP
CH2: VGOFF

VGON Control



CH1: $\overline{SHDN}$ CH3: VGON
CH2: SWCTL

Function Description

The AT1735 consists of a high-performance linear regulator, two low- power charge-pump regulators, a high-current operational amplifier, and a gate-on pulse modulator to control the positive charge-pump output sequence and waveform.

The linear regulator generates the source-driver supply voltage from the input voltage directly. The two charge-pump regulators generate the positive gate-on and negative gate-off supply voltages. The operational amplifier supplies the VCOM buffer with high output current, fast slew rate and wide bandwidth performances for driving capacitive loads. The gate-on pulse modulator control, SWCTL, is independent of the $\overline{\text{SHDN}}$ chip enable control in AT1735.

Linear Regulator

The linear regulator of AT1735 uses an internal P-channel MOSFET to supply load currents up to 500mA. The internal reference voltage of linear regulator is 2.5V, connect an external resistive voltage-divider (R1 & R2 as the Typical Application Circuit shown) to set the output voltage as requirement. The linear regulator includes an OCP function to protect the internal transistor against over loads and short circuits.

The operation input voltage range of the linear regulator is from 8V to 18V. The output voltage range of the linear regulator (OUTL) is up to 18V.

The linear regulator can driver at least 500mA output current continuously. The maximum application device power dissipation should not exceed the package-dissipation limit listed in the Absolute Maximum Ratings section.

After reference voltage reaches regulation and $\overline{\text{SHDN}}$ is logic high, the linear regulator is enabled and starts to go through the soft-start procedure. The soft-start function is to ramp up its internal reference voltage from 0 to 2.5V in 128 steps. During the soft-start period, the output voltage fault protection function is disabled.

The internal current limit of linear-regulator is approximately 1.2A. The linear regulator output voltage starts to droop when the load current exceeds limit value.

Operational Amplifier

The operational amplifier is with the excellent performances as high output current (150mA), fast slew rate (12V/μs), and wide bandwidth (12MHz) to drive the distributed series capacitance and resistance of the TFT LCD backplane.

Negative Charge-Pump Regulator

Negative charge-pump regulator contains internal P-channel and N-channel MOSFETs to perform the power transfer. The constant switching frequency of charge-pump regulator is 1.5MHz. The charge-pump inverts the supply voltage (VMAIN) and provides a regulated negative output voltage. Figure 1 shows charge-pump block diagram. During the first half-cycle, the P-channel MOSFET turns on and flying capacitor C_{CPN} charges to VMAIN minus a diode drop. During the second half-cycle, the P-channel MOSFET turns off, and the N-channel MOSFET turns on, level shifting C_{CPN}. This connects C_{CPN} in parallel with the reservoir capacitor C_{NEG}. The amount of charge transferred to the output is controlled by the variable N-channel on-resistance.

Positive Charge-Pump Regulator

Positive charge-pump regulator also contains internal P-channel and N-channel MOSFETs to perform the power transfer. The internal MOSFETs switch at a constant 1.5MHz. The charge-pump inverts the doubles supply voltage (VMAIN) and provides a regulated positive output voltage. During the first half-cycle, the N-channel MOSFET turns on and flying capacitor C_{CPP} charges to VMAIN minus a diode drop. During the second half-cycle, the N-channel MOSFET turns off, and the P-channel MOSFET turns on, level shifting C_{CPP} by VMAIN volts. This connects C_{CPP} in parallel with the reservoir capacitor C_{POS}. The amount of charge transferred to the output is controlled by the variable N-channel on-resistance.

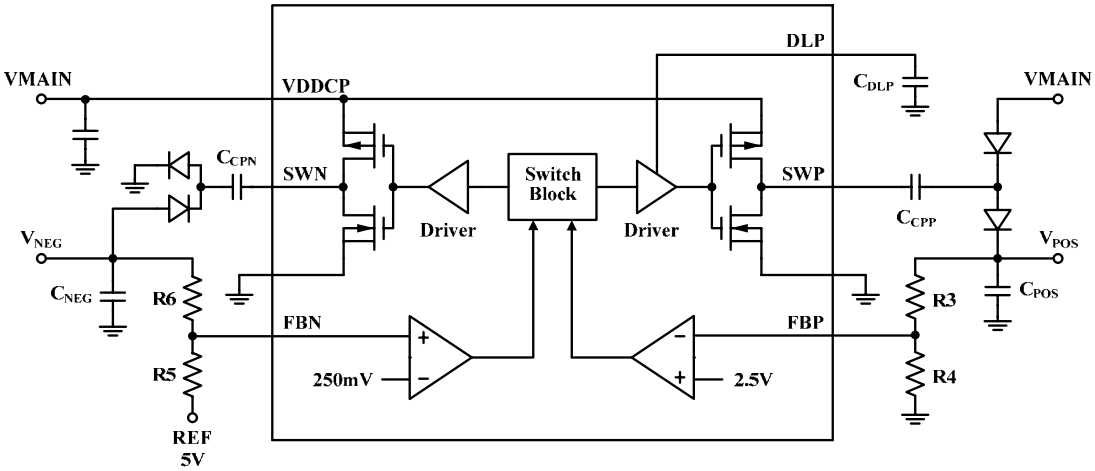


Figure 1. Charge-Pump Regulator Function Block

Output Voltage Fault Protection

After soft-start period, if feedback voltage of the linear regulator or any of the charge-pump regulator outputs does not exceed its fault-detection threshold, the AT1735 enables the internal fault timer. If any fault condition exceeds the fault-timer duration (44ms typical), the AT1735 shuts down all the outputs except the reference. Once the fault condition is removed, toggle the $\overline{SHDN}$ signal or cycle the input voltage to reactivate the chip.

Reference Voltage

The reference output voltage is typical 5V and the source ability is up to 1mA. Connecting a 0.22μF bypass ceramic capacitor between REF and GND is recommended.

Gate-On Pulse Modulator

The AT1735 includes a gate-on pulse modulator to control gate-on voltage waveform by SWCTL and AGOPT signals to reduce the flicker on TFT LCD panel.

There are two high voltage switches Q1 and Q2 connecting to GON. Another terminal of Q1 is connected to positive charge-pump output for the positive high voltage input, and Q2 is connected with a series resistor to ground for discharging the positive gate-on voltage. These two switches are controlled by DLP, SWCTL, AGOTP and THR. The switches start to be active after the V_{DLP} reaches $V_{REF}/2$. The operation that Q1 turns on and Q2 turns off is controlled by the condition SWCTL is logic high or V_{AGOTP} is lower than 2.5V. When V_{AGOTP} is higher than 2.5V, the Q1 turns off and the Q2 turns on. Once the $V_{GON}/10$ is lower than the V_{THR}, both the two switches turn off.

The control operations can be set to two difference modes as Fig 3 shown. Mode 1, connect AGOTP to REF. The high voltage period of VGON is identical to the SWCTL signal. Mode 2, connect a capacitor from AGOTP to ground. A constant current source (50μA typical) starts to charge this capacitor linearly when SWCTL is logic low. The VGON remains connecting to high input voltage VP as the V_{AGOTP} is lower than 2.5V.

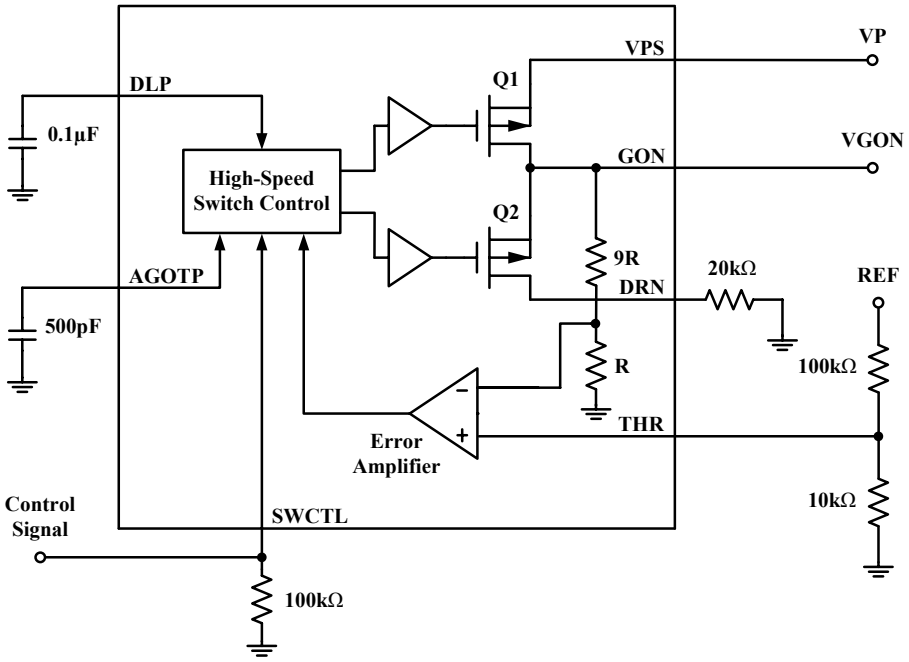


Figure 2. Gate-On Pulse Modulator Block Diagram

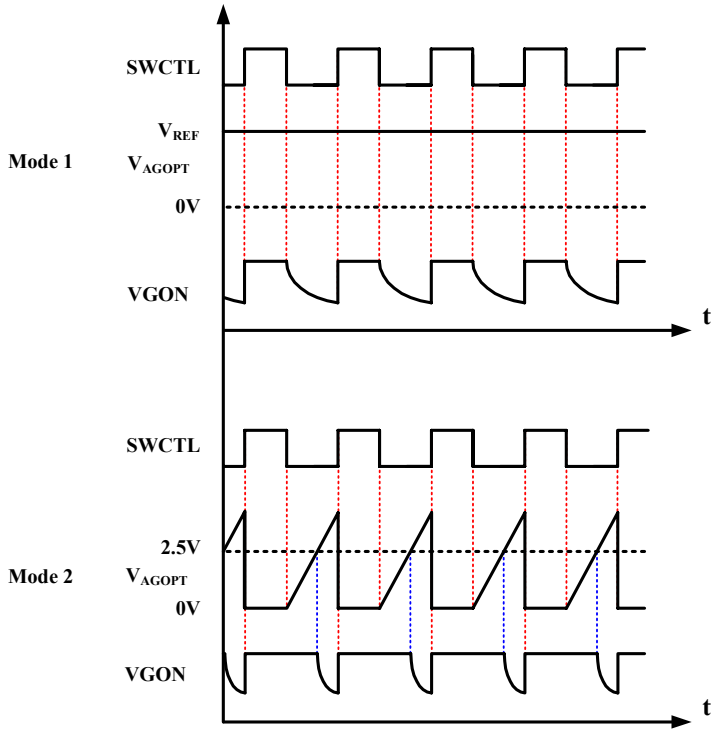


Figure 3. Gate-On Pulse Modulator Timing

Power-Up Sequence

When the AT1735 is powered up, the REF voltage rises with the input power. After the REF voltage is regulated and $\overline{SHDN}$ is logic high, the linear regulator, OPA and the negative charge-pump regulator are enabled and enter the soft-start period.

A capacitor connecting from DLP pin to GND supplies positive charge-pump regulator start-up delay. When the REF is regulated and $\overline{SHDN}$ is logic high, a 5.0uA current source charges C_{DLP}. When V_{DLP} goes above 2.5V, the positive charge pump regulator starts up and begins its soft-start period.

During the soft-start period, all the output voltage fault protection functions are disabled.

Select C_{DLP} using the following equation:

$$C_{DLP} = T_{DELAY} \times \frac{5.0uA}{V_{REF}/2}$$

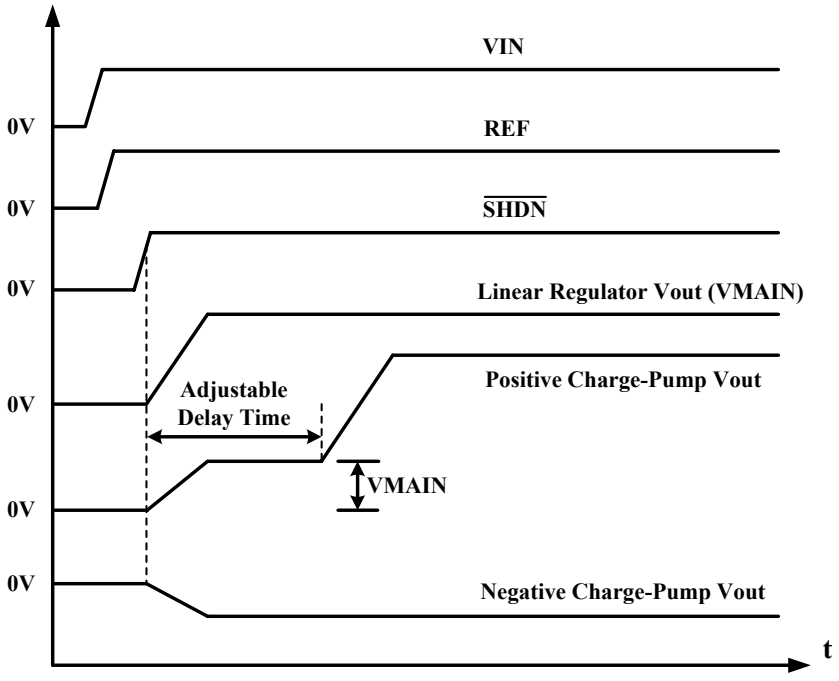


Figure 4. Power-Up Sequence

Output Voltages Setting

The output voltages of linear regulator and charge-pump converters are set by each resistive voltage-divider as Typical Application Circuit shown. The AT1735 applies a 2.5V feedback reference voltage at FBL pin of linear regulator, and the output voltage setting is according to the following equation:

$$V_{VMAIN} = 2.5 \times \left(1 + \frac{R1}{R2}\right) \ (V)$$

The feedback reference voltage of positive charge-pump V_{FBP} is typical 2.5V. The output voltage is set by the following equation:

$$V_{VP} = 2.5 \times \left(1 + \frac{R3}{R4}\right) \ (V)$$

The feedback reference voltage of negative charge-pump V_{FBN} is typical 250mV, and the reference voltage (V_{REF}) is typical 5V. So the output voltage is set by the following equation:

$$V_{VGOFF} = 0.25 - \left(\frac{4.75 \times R6}{R5}\right) \ (V)$$

External Transistor for Higher Current

The linear regulator's power dissipation can be calculated in the following equation:

$$P_D = (V_{INL} - V_{OUTL}) \times I_{OUTL}$$

For some applications, the load current may be much higher than the regulator's guaranteed output current for the AT1735. It can be connect an external PNP transistor to solve this issue as shown in Figure 5.

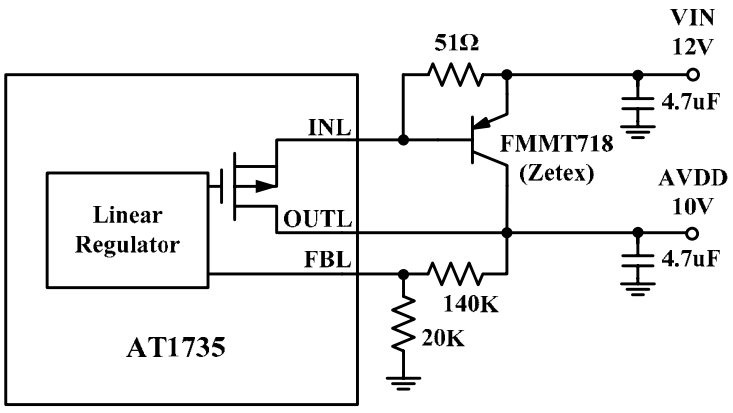
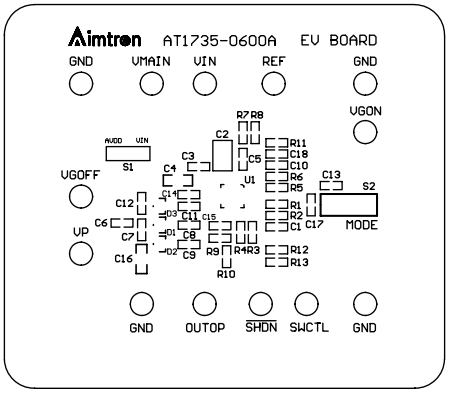


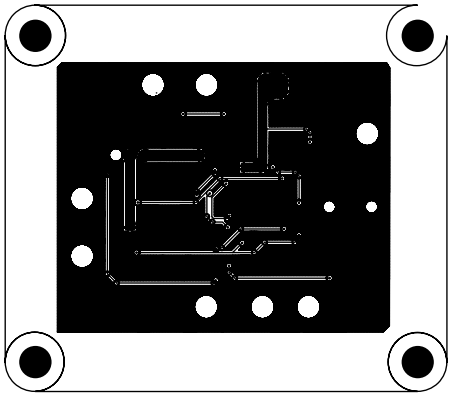
Figure 5. High-Current Linear Regulator

PC Board Layout

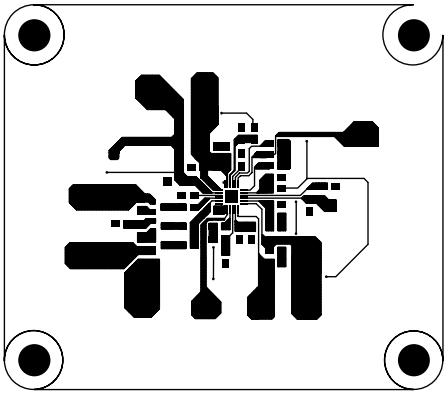
1. The most critical aspect of the layout is the placements of the input bypass capacitors of pin VCC, INL, VDDCP, VDDOP, VPS and REF. They must be placed as close as possible to the AT1735 to reduce the input ripple voltage and noise coupling.
2. Power loops on the input and output of the converters should be connected with the shortest and widest traces as possible. The long and narrow trace increases the ESR and ESL, and that will induce more effective noise at high frequency easily.
3. The feedback resistors should connect to FB pins as close as possible. And each route connected to output should be away from the switching noise source, such as charge-pump power loops.
4. Connecting all the ground-side of components at the backside ground-plane may effectively reduce the occurrence of unnecessary loop.



Component side

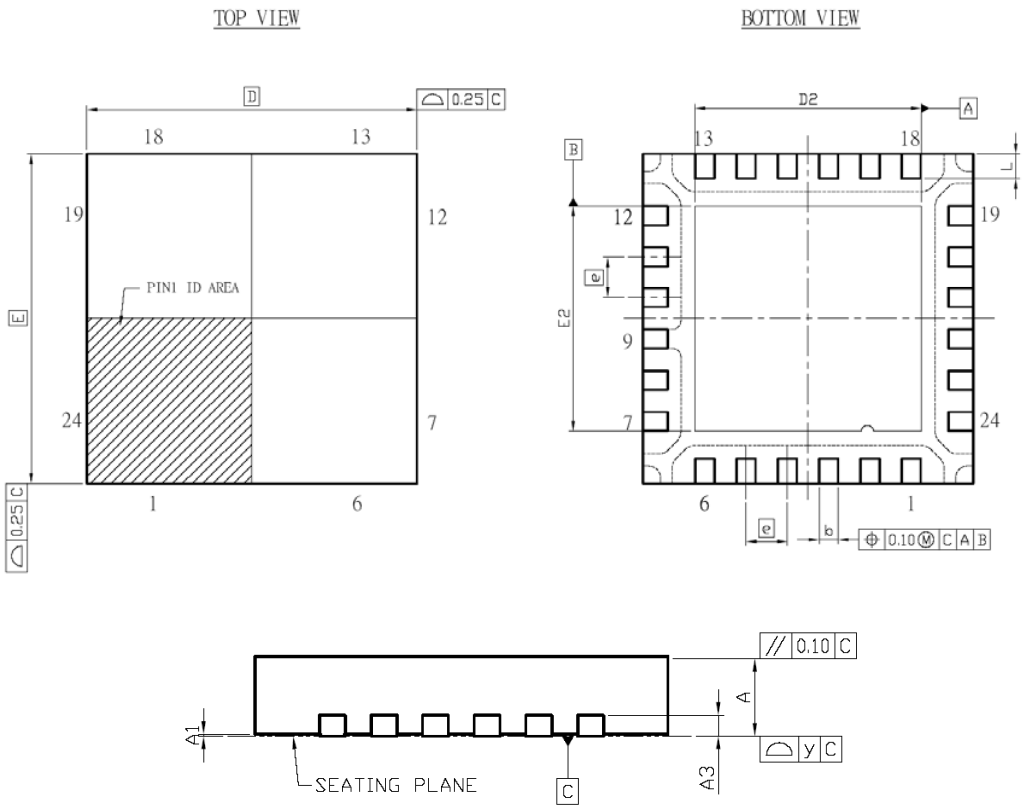


Bottom-layer



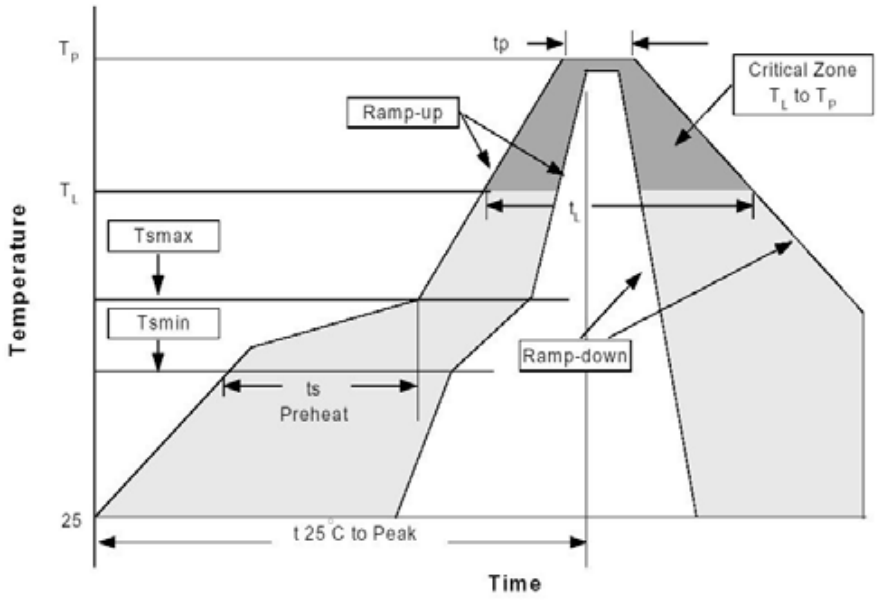
Top-layer

Package Outline: Thin QFN-24



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			8 REF		
b	0.18	0.25	0.30	7.09	9.84	11.81
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	2.66	2.74	2.82	104.7	107.9	111.0
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	2.66	2.74	2.82	104.7	107.9	111.0
e	0.50 BSC			19.7 BSC		
L	0.22	0.30	0.38	8.8	11.8	14.8
y	0.08			3.15		
R	0.10 BSC			4.0 BSC		

Reflow Profiles



Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm³	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm³**	**Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm³**	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm³**
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat -Temperature Min(Tsmin) -Temperature Max (Tsmax) -Time (min to max)(ts)	100°C 150°C 60-120 seconds		150°C 200°C 60-180 seconds	
Tsmax to T_L -Ramp-up Rate			3°C/second max.	
Time maintained above: -Temperature (T_L) -Time (t_L)	183°C 60-150 seconds		217°C 60-150 seconds	
Peak Temperature(T_P)	225+0/-5°C	240+0/-5°C	245+0/-5°C	250+0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

***All temperatures refer to topside of the package, measured on the package body surface.**