Aimtron
圓創科技股份有限公司

AT1738

Preliminary Product Information

LCD Panel Step-up Converter with Analog Multi-Function Outputs

Features

- 2.6V to 5.5V Input Supply Range
- 640KHz/1.2MHz Current-Mode PWM Step-Up Regulator:
  - Fast Transient Response
  - 1.0% High-Accuracy Output Voltage
  - Built-In 18V, 2.0A, 0.2Ω N-Channel MOSFET
  - Programmable Soft-Start
  - Current-Limit
  - Latched Fault Protection with Timer
  - High Efficiency
- Gate-On Charge Pump Regulator Controller with Latched Fault Protection with Timer
- High-Performance Linear Regulator:
  - 1.5% Output Accuracy
  - Works with Small Ceramic Output Capacitors
  - Fast Transient Response
  - Foldback Current Limit
- High-Current Operational Amplifier:
  - ±150mA Output Short-Circuit Current
  - 13V/μs Slew Rate
  - 12MHz, -3dB Bandwidth
  - Rail-to-Rail Input/Output
- Gate-on Pulse Modulator with Adjustable Delay for Sequence Control
- Voltage Detector with Adjustable Delay

Applications

- LCD Monitor Panel Modules
- NB LCD Panel Modules
- Automotive Displays

General Description

The AT1738 offers a complete power-supply solution for TFT LCD panels used in LCD monitors and NB LCD panels. The AT1738 consists of a high-performance step-up converter, a low-power charge-pump regulator, a high-performance linear regulator, an operational amplifier, a voltage detector and a logic-controlled gate-on pulse modulator.

The step-up DC-DC converter provides the regulated supply voltage for the panel source driver ICs. The charge-pump regulator generates the positive gate-on supply voltage. The operational amplifier supplies the VCOM buffer with high output current, fast slew rate and wide bandwidth performances for driving capacitive loads.

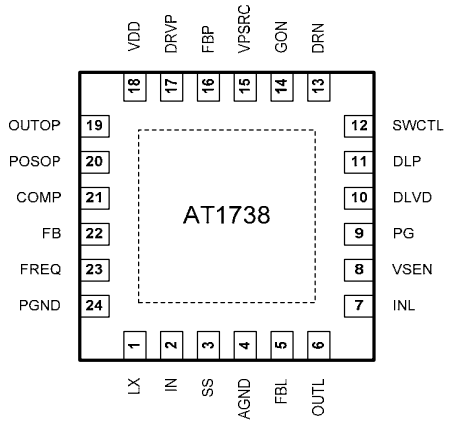
The high-voltage gate-on pulse modulator to control the positive gate-on output voltage waveform for reducing the flicker on TFT LCD panel.

The high-performance linear regulator uses an internal P-channel MOSFET to supply load currents up to 350mA. It provides the regulated supply voltage for the TCON IC.

The voltage detector with adjustable detected voltage-point and delay-time monitors the input supply voltage to prevent the improper shutdown of the system power application.

The AT1738 is available in a 24-pin thin QFN package which is 4mm x 4mm with a maximum thickness of 0.8mm for ultra-thin LCD panel design.

Pin Configuration



Aimtron reserves the right without notice to change this circuitry and specifications.

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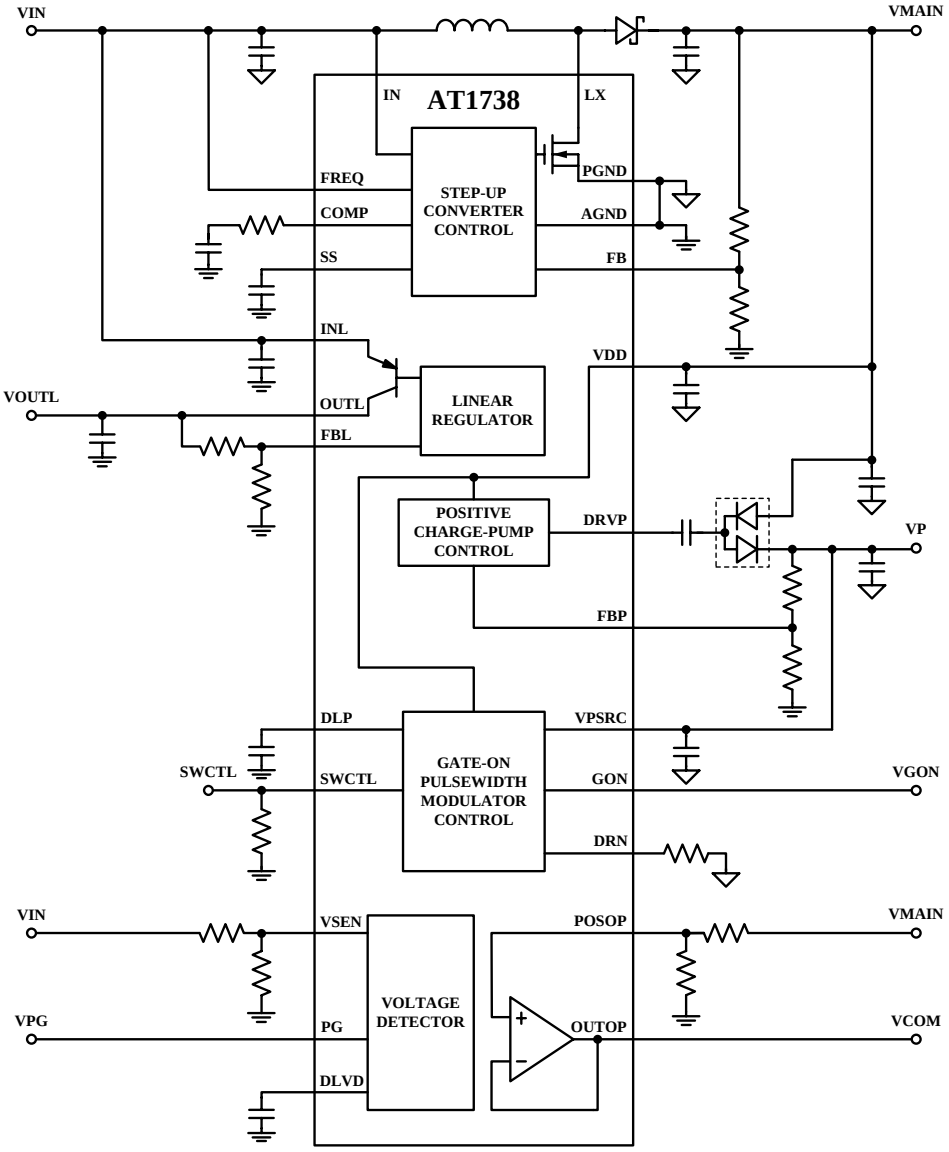
Ordering Information

Part number	Package	Marking
AT1738N_GRE	Thin QFN24, Green	AT1738N

Block Diagram



Pin Descriptions

Pin No.	Pin Name	Function
1	LX	Drain of Internal N-Channel Power MOSFET of Step-Up Converter. Minimize the connecting trace area for the lowest EMI.
2	IN	IC Supply Voltage Input.
3	SS	Soft-Start Setting Pin of Step-Up Converter. Connect a capacitor from SS to AGND to set the soft-start period.
4	AGND	Analog Ground for the Signal Control.
5	FBL	Linear-Regulator Feedback Input. Place the voltage-divider to IC as close as possible.
6	OUTL	Linear Regulator Output.
7	INL	Linear Regulator Input.
8	VSEN	Sense Input of Voltage Detector.
9	PG	Power-Good Signal Output of Voltage Detector.
10	DLVD	Voltage Detector Power-Good Signal Delay Input. Connect a capacitor from DLVD to GND to set the delay time.
11	DLP	Positive Gate-On Pulse Modulator Delay Input. Connect a capacitor from DLP to GND to set the delay time.
12	SWCTL	Gate-On Pulse Modulator Timing Control Input.
13	DRN	Discharge Switch Input. Connect a resistor to GND to discharge the VGON when SWCTL is low.
14	GON	Internal High-Voltage Gate-On Pulse Modulator Output Terminal for Positive Gate-On Driver Voltage Supply.
15	VPSRC	Gate-On Pulse Modulator Voltage Supply Input. Source of the internal high-voltage P-channel MOSFET connected to GON. Connect a minimum 0.1μF capacitor close to the VPSRC and PGND pins.
16	FBP	Positive Charge-Pump Feedback Input. Place the voltage-divider to IC as close as possible.
17	DRVP	Positive Charge-Pump Driver Output. Output high level is VDD, and output low level is GND. SWP is internally pulled to GND in shutdown.
18	VDD	Power Supply Input for Gate-On Pulse Modulator Driver, Positive Charge-Pump Driver and Operational Amplifier. Connect a 0.1μF capacitor from VDD to PGND.
19	OUTOP	Operational Amplifier Output.
20	POSOP	Operational Amplifier Noninverting Input.
21	COMP	Compensation Pin of Step-Up Converter Error-Amplifier. Connect a compensation network from COMP to AGND.
22	FB	Step-Up Converter Feedback Input. Connect a resistive voltage-divider to determine the step-up converter output voltage. Place the resistive voltage-divider close to this pin.
23	FREQ	Frequency Selection Pin of Step-Up Converter. Connect to logic high for 1.2MHz operation, and connect to logic low for 640KHz operation. This pin is with an internal 4μA pull-low constant current.
24	PGND	Power Ground. PGND is the source of the n-channel power MOSFET of step-up converter. Place the input-capacitor ground terminals close to PGND with a wide trace.
Exposed Pad	AGND	Analog Ground. Exposed pad should solder to analog ground plane for the optimal power dissipation.

Absolute Maximum Ratings (Ta = 25℃)

Parameter	Rated Value		Unit
	Min.	Max.	
IN, FB, SS, COMP, FREQ, INL, OUTL, FBL, FBP, VSEN, PG, DLVD, SWCTL, DLP	-0.3	+6.0	V
PGND to AGND	-0.3	+0.3	V
LX, DRVP	-0.3	+16.0	V
VDD, POSOP, OUTOP	-0.3	+16.0	V
VPSRC, GON, DRN	-0.3	+30.0	V
LX Switch Maximum Continuous RMS Output Current	-	2.0	A
OUTOP Maximum Continuous Output Current	-75.0	+75.0	mA
Power Dissipation (Ta≦25℃)	-	1349	mW
Operating Temperature	-30	+85	°C
Storage Temperature	-55	+150	°C
Lead Temperature (soldering, 10s)	-	+260	°C
ESD Susceptibility (MM)	-200	200	V
ESD Susceptibility (HBM)	-2	2	KV

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Devices are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Recommended Operating Conditions

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{IN}	2.6	-	5.5	V
Operating Junction Temperature	T_J	-30	-	+125	°C

***Using X5R or X7R capacitors.**

Electrical Characteristics

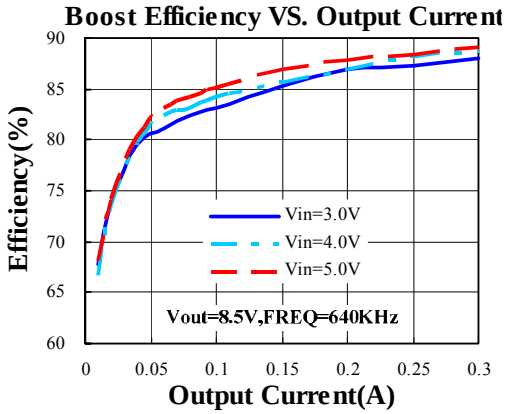
(Test circuit is shown as Typical Application Circuit. V_{IN} = 3.3V, V_{VDD} = 8.5V, PGND = AGND = 0, Ta= 0℃ to +85℃. Typical values are at Ta=+25℃, unless otherwise noted.)

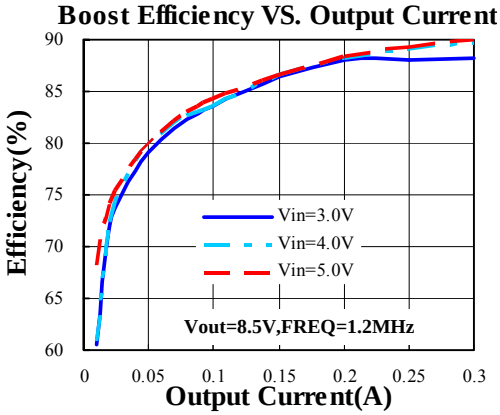
Parameter	Condition	Values			Unit
		Min.	Typ.	Max.	
IN Supply Range		2.5		5.5	V
IN Undervoltage-Lockout Threshold	V_{IN} rising	2.1	2.2	2.3	V
	Hysteresis		200		mV
IN Quiescent Current	V_{FB} = 1.4V, LX not switching		0.4	1.1	mA
	V_{FB} = 1.2 V, LX switching		5	7	
	V_{FB} = 0.5 V, shutdown current		0.3	0.5	mA
Main Step-Up Regulator Section					
Output Voltage Range		V_{IN}		16	V
Operating Frequency (f_{OSC})	FREQ=high	1000	1200	1400	kHz
	FREQ=low		640		
FREQ Input Low Voltage				0.6	V
FREQ Input High Voltage		1.5			V
FREQ Pull-Down Current	V_{FREQ}=1.0V		4		µA
Oscillator Maximum Duty Cycle		86	90	94	%
Feedback Regulation voltage	No load, Ta=+25℃	1.228	1.240	1.252	V
FB Input Bias Current	V_{FB}=1.5V	-40	1	40	nA
FB Load Regulation	0 mA<I_{LX}< full load, transient only		-1.6		%
FB Line Regulation	2.5V < Vin < 5.5V		0.1		%/V
FB Transconductance		75	160	280	µS
FB Voltage Gain	FB to COMP		700		V/V
FB Fault Trip Level	V_{FB} falling		1.0		V
Duration to Trigger Fault condition			160		ms
LX Switch On-Resistance			200	400	mΩ
LX Leakage Current	V_{LX}=18V		0.02	40	µA
LX Current Limit	V_{IN}=3.3V		2.0		A
Current-Sense Transconductance			0.5		S
Soft-Start Charge Current		2	4	6	µA
Operational Amplifier Section					
OP Supply Operating Range		4.5		16	V
OP Supply Current	Buffer configuration, V_{POSOP} = 4V, no load		1.5	1.7	mA
Input Offset Voltage	(V_{OUTOP}, V_{POSOP}) = V_{VDD} / 2, T_A = +25℃	-17	0	17	mV
Input Bias Current	(V_{OUTOP}, V_{POSOP}) = V_{VDD} / 2	-50	1	50	nA
Output Voltage Swing High	I_{OUTOP} = 100µA	V_{VDD} -15	V_{VDD} - 3		mV
	I_{OUTOP} = 5mA	V_{VDDOP} -150	V_{VDDOP} - 80		

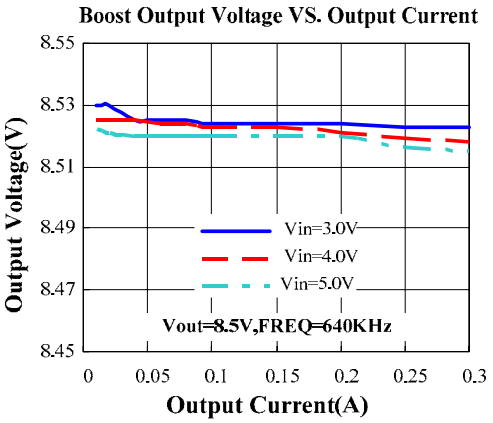
Output Voltage Swing Low	I_{OUTOP} = -100µA		2	15	mV
	I_{OUTOP} = -5mA		70	150	
Short-Circuit Current	Short to V_{VDDOP} / 2, sourcing	100	150	180	mA
	Short to V_{VDDOP} / 2, sinking	100	150	180	
Output Current	Buffer configuration, V_{POSOP} = 4V, V_{OUTOP} error < ±10mV	±40			mA
Slew Rate			13		V/µs
-3dB Bandwidth	Buffer configuration, R_L = 10kΩ, C_L = 10pF		12		MHz
Gain-Bandwidth Product	Buffer configuration, R_L = 10kΩ, C_L = 10pF		8		MHz
Linear Regulator Section					
INL Operation Supply Range	$V_{OUTL} < V_{INL}$	2.5		5.5	V
Quiescent Current			60		µA
Dropout Voltage	I_{OUTL} = 350mA		300	500	mV
FBL Regulation Voltage	I_{OUTL} = 50mA	1.224	1.240	1.256	V
FBL Input Bias Current	V_{FBL} = 2.5V			50	nA
FBL Line-Regulation Error	V_{INL} = 2.8V~5.5V, V_{OUTL} = 2.5V, I_{OUTL} = 100mA		0.1	0.3	%/V
OUTL Load Regulation	Iout=1mA to 300mA		0.2	0.5	%
Current Limit	V_{FBL} = 1.2V		500		mA
Positive Charge-Pump Regulator Section					
FBP Regulation Voltage	I_{VP} = 10mA	1.216	1.240	1.264	V
FBP Line-Regulation Error	V_{MAIN} (V_{VDD}) = 10.8V~13.2V, V_{VP} = 18V, I_{GON} = 20mA		0.5	0.8	%/V
Operating Frequency			0.5* f_{OSC}		Hz
FBP Input Bias Current	V_{FBP} = 1.24V	-50		+50	nA
SWP P-Channel On-Resistance			15	30	Ω
SWP N-Channel On-Resistance	V_{FBP} = 1.2V		6	12	Ω
	V_{FBP} = 1.5V	20			kΩ
FBP Fault Trip Level (UVP)	Falling edge		1.0		V
Duration to Trigger Fault condition			160		ms
Gate-On Voltage Pulse Modulation Switches Section					
DLP Capacitor Charge Current	During startup, V_{DLP} = 1.0V	18	20	22	µA
DLP Turn-On Threshold		1.216	1.240	1.264	V
DLP Discharge Switch On-Resistance	During UVLO, V_{IN} = 2.2V		35		Ω
SWCTL Input Low Voltage				0.6	V
SWCTL Input High Voltage		2.0			V
SWCTL Input Leakage Current		-1		+1	µA
SWCTL to GON Propagation Delay	Rising & Falling		100		ns
VPSRC Input Voltage Range				30	V
VPSRC Input Current	V_{DLP}=1.5V, SWCTL=low		50	100	µA
	V_{DLP}=1.5V, SWCTL=high		15	30	µA

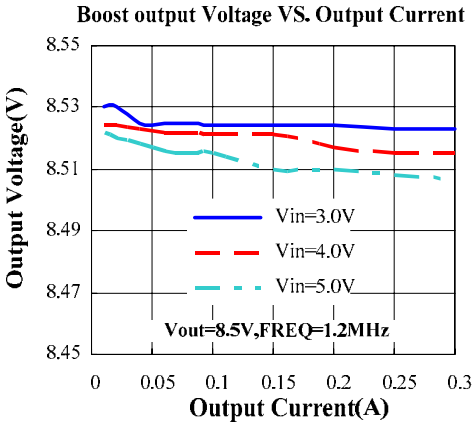
VPSRC to GON Switch On-Resistance	V_{DLP}=1.5V, SWCTL=low		10	20	Ω
DRN to GON Switch On-Resistance	V_{DLP}=1.5V, SWCTL =high		35	70	Ω
Voltage Detector Section					
V_{IN} Minimum Operation Voltage		2.1	2.2	2.3	V
Detect Threshold Voltage			1.04		V
Detect Threshold Voltage Accuracy		-1.0		1.0	%
Adjustable Delay Time-Constant	$K = T_{DELAY\_VD} / C_{DLVD}$		120k		Ω

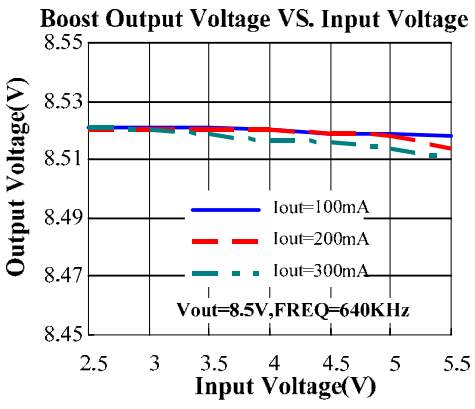
Typical Operating Characteristics

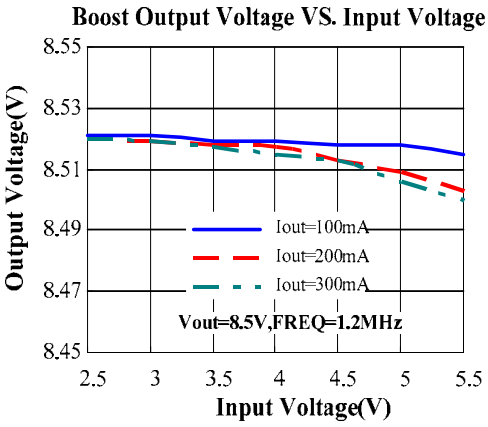




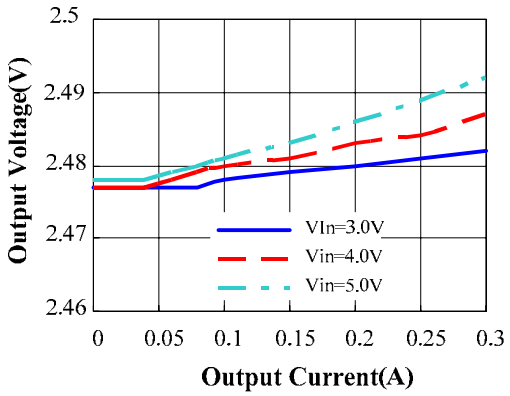




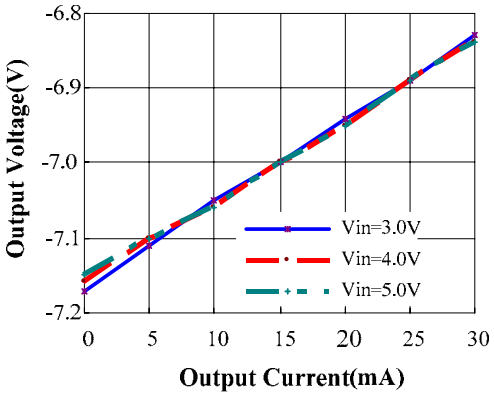




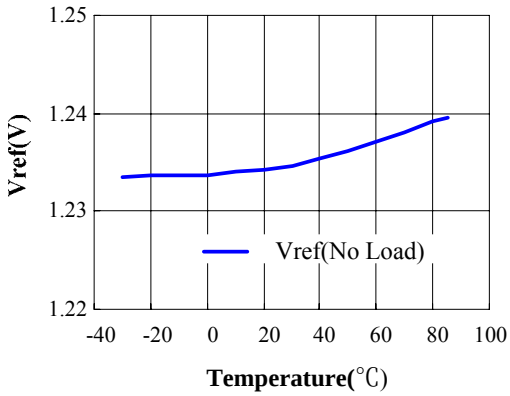
LDO Output Voltage VS. Output Current



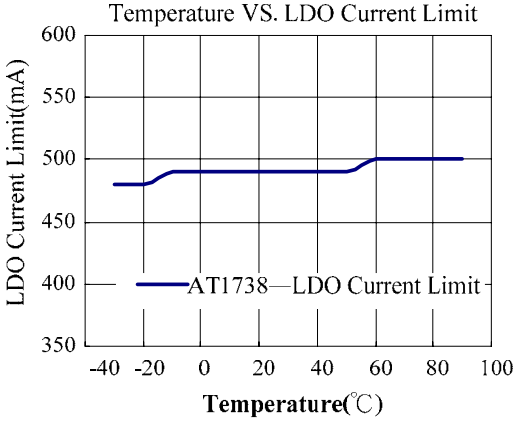
VGL Output Voltage VS. Output Current



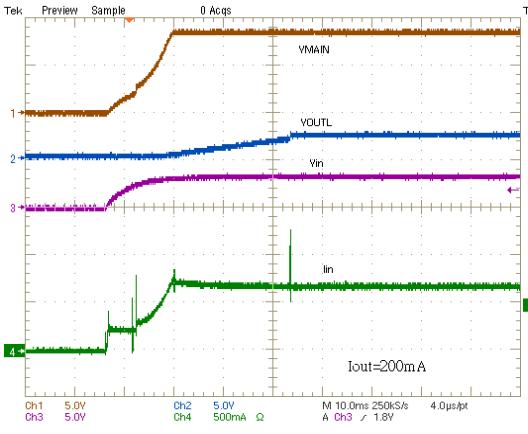
Boost Vref VS. Temperature



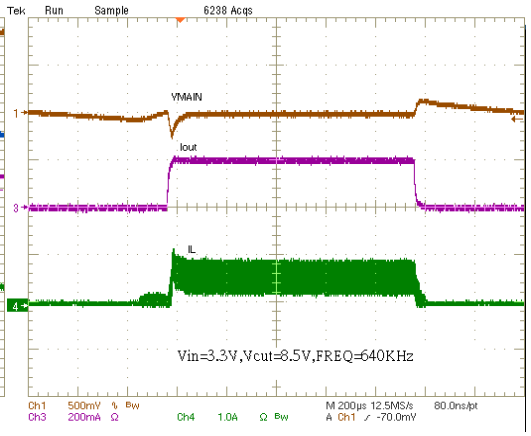
Temperature VS. LDO Current Limit



Boost Start Up



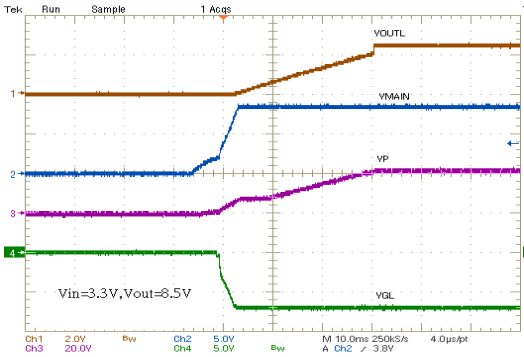
Boost Load Transient Response



CH1：VMAIN　CH2：VOUTL　CH1：VMAIN(AC)　CH3：IMAIN

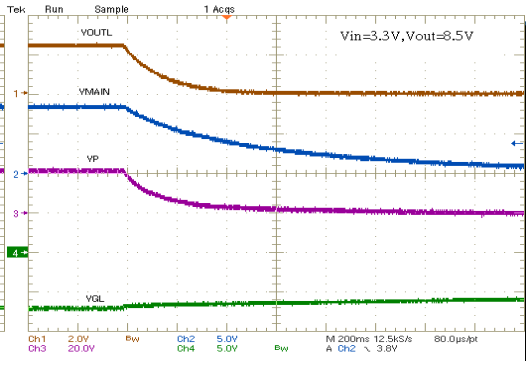
CH3：Vin　CH4：Iin　CH4：IL

Power On Sequence With VGL



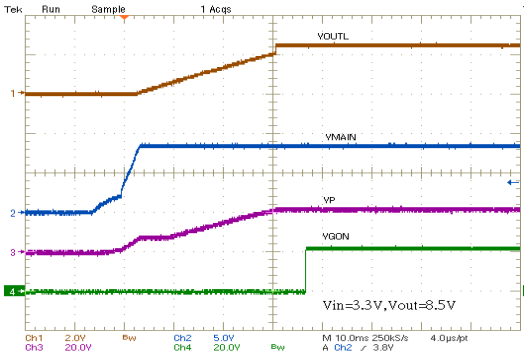
CH1：VOUTL CH2：VMAIN
CH3：VP CH4：VGL

Power Off Sequence With VGL



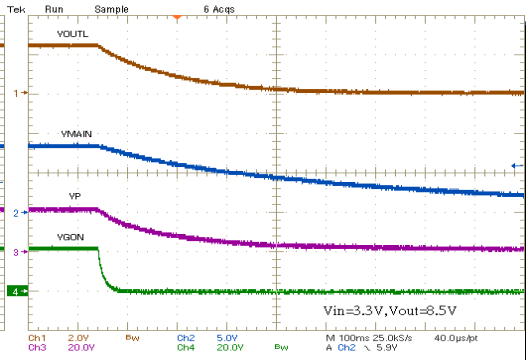
CH1：VOUTL CH2：VMAIN
CH3：VP CH4：VGL

Power On Sequence With VGON



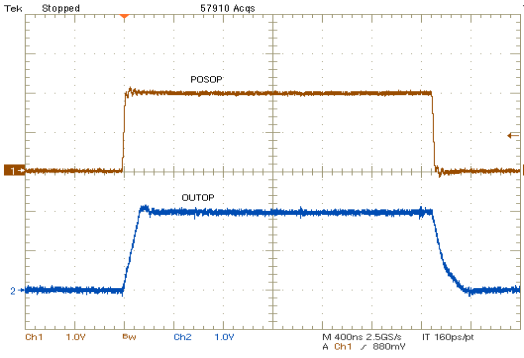
CH1：VOUTL CH2：VMAIN
CH3：VP CH4：VGON

Power Off Sequence With VGON



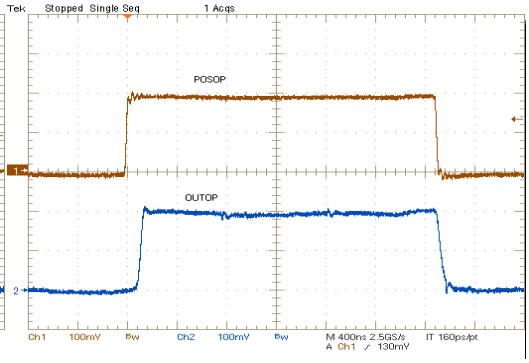
CH1：VOUTL CH2：VMAIN
CH3：VP CH4：VGON

OPA Large Signal Step Response



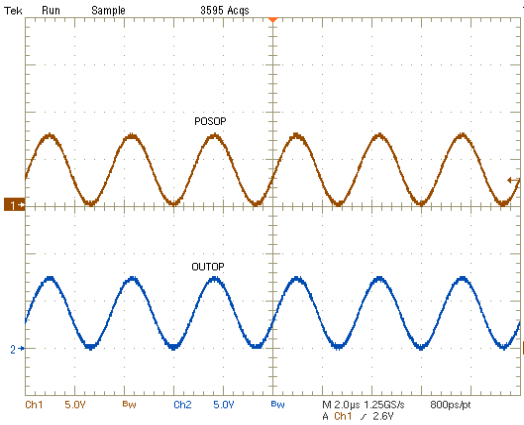
CH1：POSOP CH2：OUTOP

OPA Small Signal Step Response



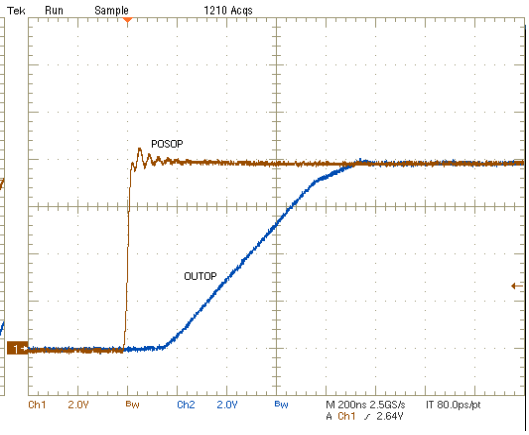
CH1：POSOP CH2：OUTOP

OPA Rail to Rail Input/Output



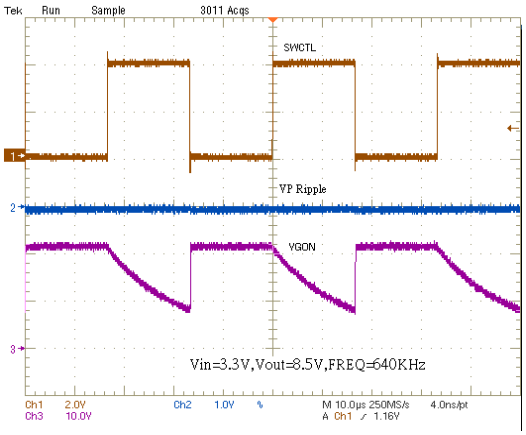
CH1：POSOP CH2：OUTOP

OPA Slew Rate



CH1：POSOP CH2：OUTOP

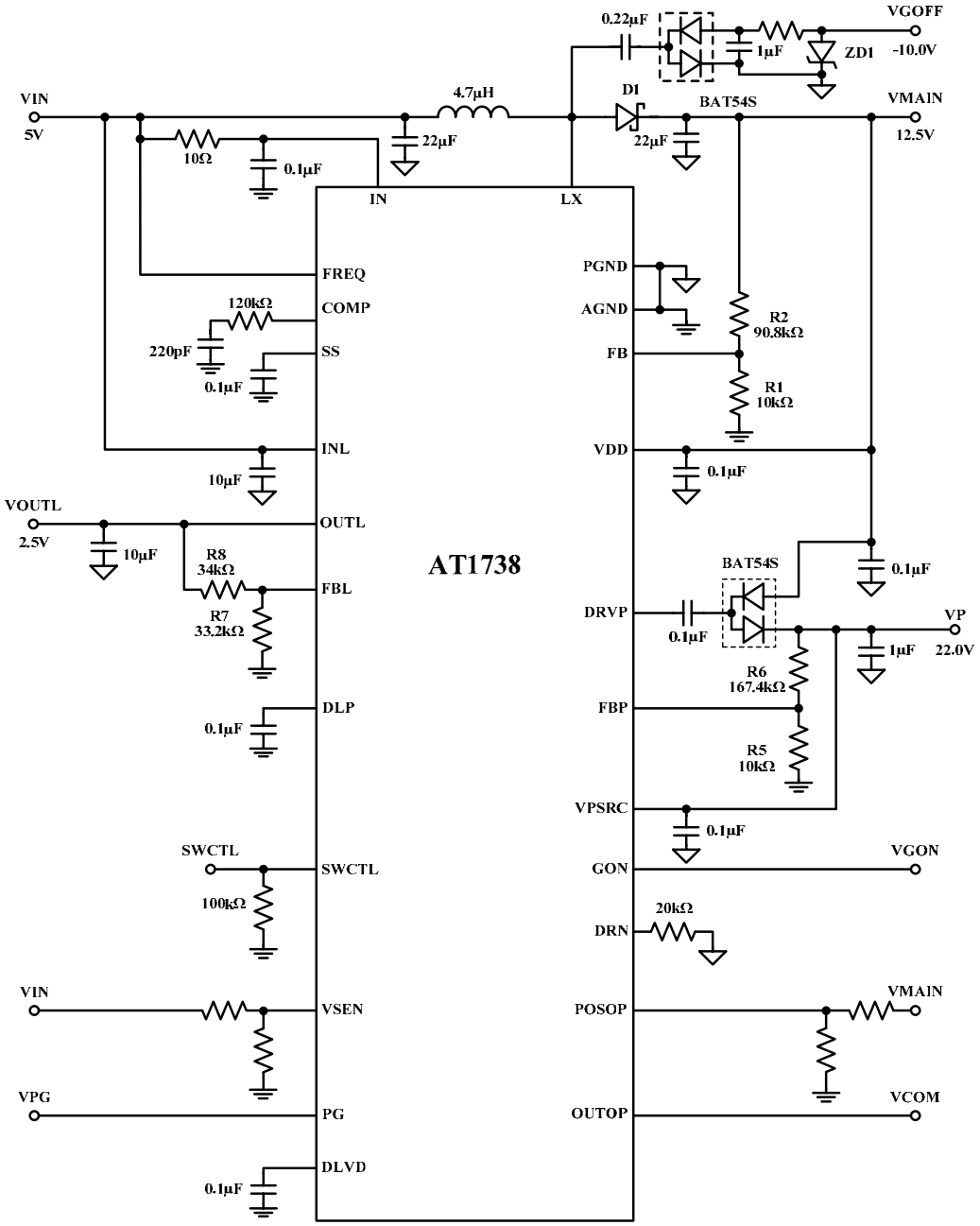
VGON With SWCTL



CH1：SWCTL CH2：VP Ripple

CH3：VGON

Typical Application Circuit



Function Description

The AT1738 offers a complete power-supply solution for TFT LCD panels used in LCD monitors and NB LCD panels. The AT1738 consists of a high-performance step-up converter, a low-power charge-pump regulator, a high-performance linear regulator, an operational amplifier, a voltage detector and a logic-controlled gate-on pulse modulator.

Step-up Converter

The step-up DC-DC converter adopts the PWM current mode control, fixed selectable 640k/1.2MHz switching frequency and an internal 2.0A, 0.2Ω (typical) power MOSFET. Such architecture provides faster line and load transient responses for the specific performance of the source-driver supply voltage source. The high switching frequency can minimize the components as the space of thick LCD panel required. The programmable soft-start function restrains the inrush current and output voltage overshoot with an external capacitor. The external compensation network provides the flexibility in determining output voltage regulation accuracy and dynamic response. The switching frequency can be selected by user to operate at either 640 kHz or 1.2MHz. Connect FREQ to logic high for 1.2MHz operation, and connect to logic low for 640 KHz operation. FREQ has an internal pull-low for the 640 kHz operation if leaving FREQ unconnected.

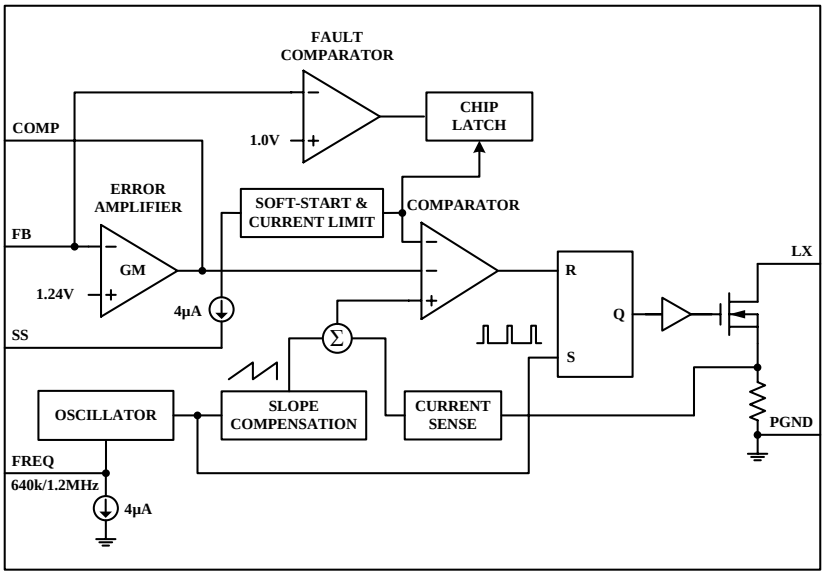


Figure 1. Step-up converter block diagram

Positive Charge-Pump Regulator

Positive charge-pump regulator also contains internal P-channel and N-channel MOSFETs to perform the power transfer. The internal MOSFETs switch at a constant 0.5* f_{OSC} Hz. The charge-pump inverts the doubles supply voltage (VMAIN) and provides a regulated positive output voltage. During the first half-cycle, the N-channel MOSFET turns on and flying capacitor C_{CPP} charges to VMAIN minus a diode drop. During the second half-cycle, the N-channel MOSFET turns off, and the P-channel MOSFET turns on, level shifting C_{CPP} by VMAIN volts. This connects C_{CPP} in parallel with the reservoir capacitor C_{POS}. The amount of charge transferred to the output is controlled by the variable N-channel on-resistance.

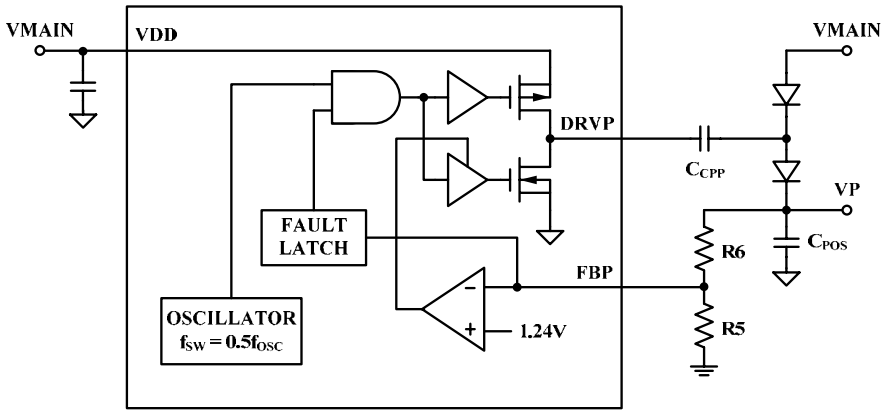


Figure 2. Charge-Pump Regulator Function Block

Soft-Start

The step-up converter and positive charge-pump regulator uses an external capacitor to perform the soft-start function. When VIN exceeds UVLO threshold, the internal reference voltage of the step-up converter starts to rise. After reference voltage reaches regulation, the step-up converter and positive charge-pump regulator start the soft-start process. The soft-start capacitor is immediately charged at a constant current of 4μA (typical). During this time, the SS voltage directly controls the peak inductor current of the step-up converter and the feedback reference voltage of the positive charge-pump regulator. The soft-start period is complete when V_{SS} exceeds 1.24V. When VIN falls below UVLO threshold, the soft-start capacitor is discharged to ground.

$$T_{SS} = C_{SS} \times \frac{1.24V}{4.0\mu A} \quad (sec)$$

Linear Regulator

The linear regulator uses an internal P-channel MOSFET to supply load currents up to 350mA. The internal reference voltage of linear regulator is 1.24V, connect an external resistive voltage-divider (R7 & R8 as the Typical Application Circuit shown) to set the output voltage as requirement. The linear regulator can driver at least 350mA output current continuously. The maximum application device power dissipation should not exceed the package dissipation limit listed in the Absolute Maximum Ratings section. The linear regulator includes an OCP function to protect the internal transistor against over loads and short circuits The internal current limit of linear-regulator is approximately 500mA. Once the load current exceeds limit value, the linear regulator output voltage starts to droop.

Operational Amplifier

The operational amplifier is with the excellent performances as high output current (150mA), fast slew rate (13V/μs), and wide bandwidth (12MHz) to drive the distributed series capacitance and resistance of the TFT LCD backplane.

Voltage Detector

The voltage detector with adjustable detected voltage-point and delay-time monitors the input supply voltage to prevent the improper shutdown of the system power application. Connect a capacitor from DLVD to GND to set the required delay time.

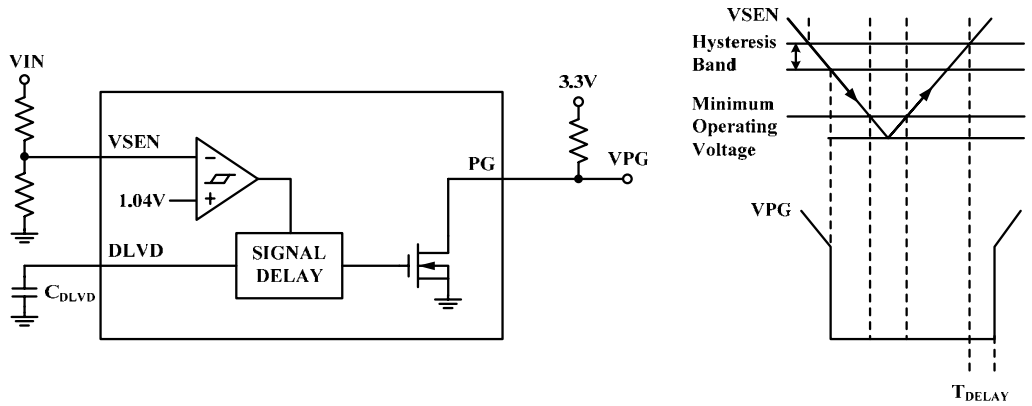


Figure 3. Voltage Detector Function Block and Timing Chart

$$T_{DELAY\_VD} = C_{DLVD} \times 120k \quad (sec)$$

Gate-On Pulse Modulator

The AT1738 includes a gate-on pulse modulator to control gate-on voltage waveform to reduce the flicker on TFT LCD panel. After the VIN exceeds UVLO, once the soft-start periods are complete, fault conditions do not exist, and the VDLP exceeds the turn-on threshold, then the gate-on pulse modulator starts to be active and is controlled by SWCTL. There are two high voltage switches Q1 and Q2 connecting to GON. Another terminal of Q1 is connected to positive charge-pump output for the positive high voltage input (VPSRC), and Q2 is connected to DRN with an external series resistor to ground for discharging the positive gate-on voltage. If SWCTL is high, Q1 turns off and Q2 turns on. If SWCTL is low, Q1 turns on and Q2 turns off.

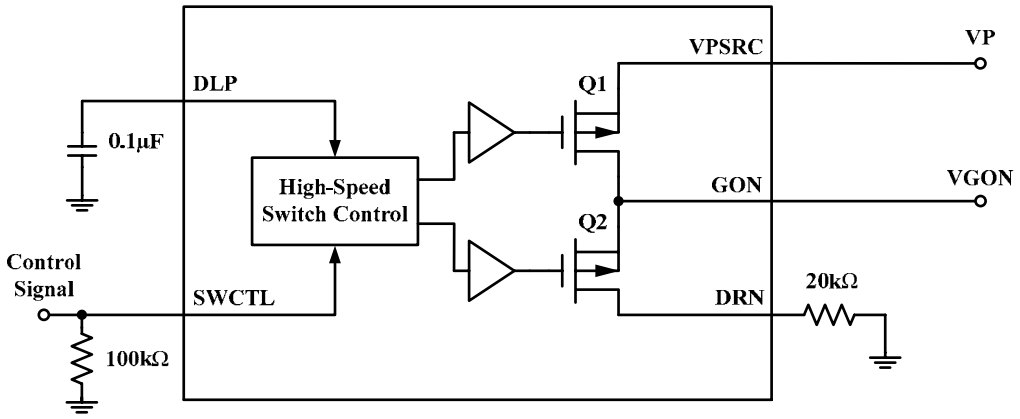


Figure 4. Gate-on pulse modulator

Output Voltage Fault Protection

After soft-start period, if feedback voltage of the step-up DC-DC converter or gate-on charge-pump regulator does not exceed its fault-detection threshold, the AT1738 enables the internal fault timer. If any fault condition exceeds the fault-timer duration (160ms typical), the AT1738 shuts down the step-up converter, gate-on charge-pump regulator, operational amplifier and gate-on pulse modulator. Once the fault condition is removed, cycle the input voltage to reactivate the chip.

Power-Up Sequence

The AT1738 goes through start-up sequence after power-up. When VIN exceeds UVLO threshold, the internal reference voltage starts to rise. After reference voltage reaches regulation, the step-up converter and linear regulators will start up with the soft-start process.

Once the FB voltage reaches the reference voltage, the gate-on pulse modulator delay block is also enabled. The gate-on pulse modulator is enabled after the V_{DLP} goes above V_{REF} with a constant charging current (20μA typical). Connect an appropriate capacitor between DLP and GND to obtain the required delay-time.

$$T_{DELAY\_SW} = C_{DLP} \times \frac{1.24V}{20.0\mu A} \quad (sec)$$

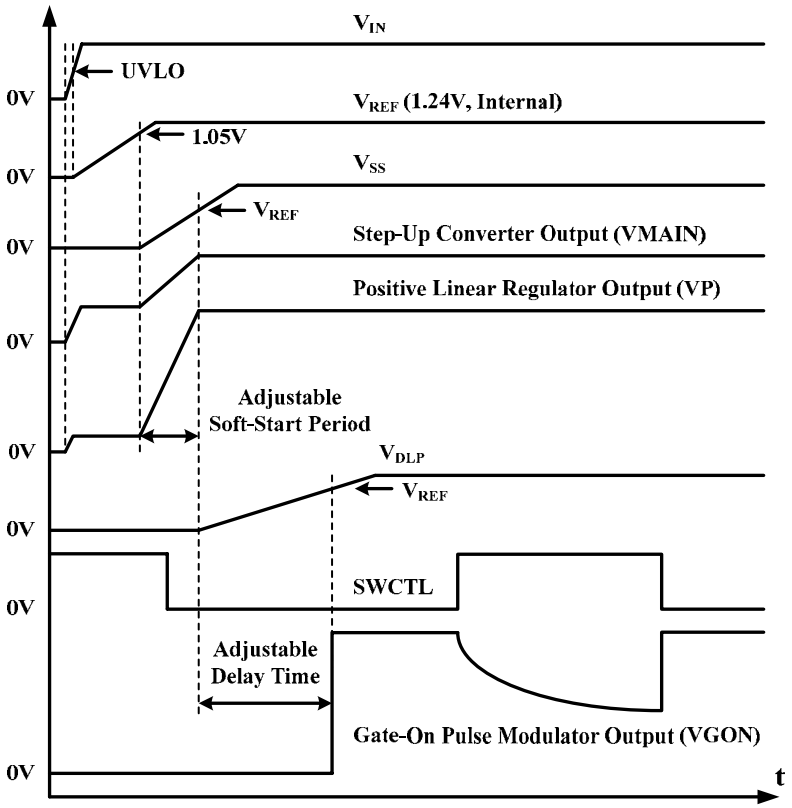


Figure 5. Power-up sequence

Output Voltages Setting

The output voltages of step-up converter, positive charge-pump regulator and linear regulators are set by each resistive voltage-divider as the Typical Application Circuit shown.

The AT1738 applies a 1.240V feedback reference voltage at FB pin of step-up converter, and the output voltage setting is according to the following equation:

$$VMAIN = 1.24 \times \frac{(R1 + R2)}{R1} \quad (V)$$

The feedback reference voltage of positive charge-pump regulator, V_{FBP}, is typical 1.240V. The output voltage is set by the following equation:

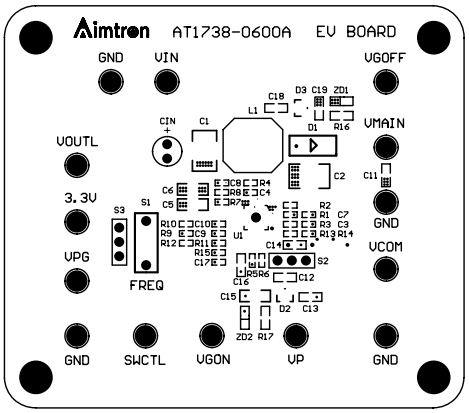
$$VP = 1.24 \times \frac{(R5 + R6)}{R5} \quad (V)$$

The feedback reference voltage of linear regulator, V_{FBL}, is typical 1.240V. The output voltage is set by the following equation:

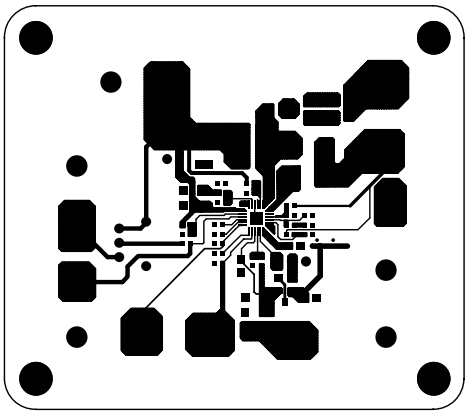
$$VOUTL = 1.24 \times \frac{(R7 + R8)}{R7} \quad (V)$$

PC Board Layout

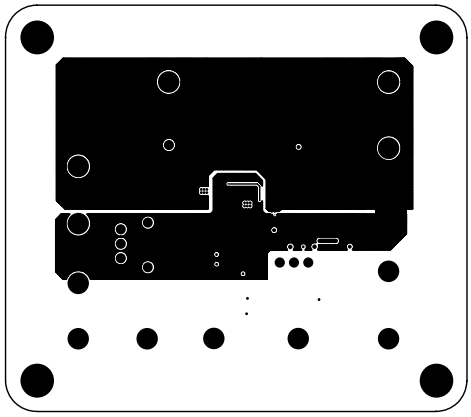
1. The most critical aspect of the layout is the placements of the input bypass capacitors of pin IN, INL, VDD and VPSRC. They must be placed as close as possible to the AT1738 to reduce the input ripple voltage and noise coupling.
2. Power loops on the input and output of the converters should be connected with the shortest and widest traces as possible. The long and narrow trace increases the ESR and ESL, and that will induce more effective noise at high frequency easily.
3. The feedback resistors should connect to FB pins as close as possible. And each route connected to output should be away from the switching noise source, such as charge-pump power loops.
4. Connecting all the ground-side of components at the backside ground-plane may effectively reduce the occurrence of unnecessary loop.



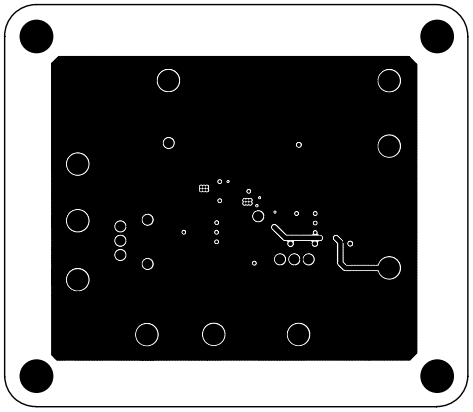
Component side



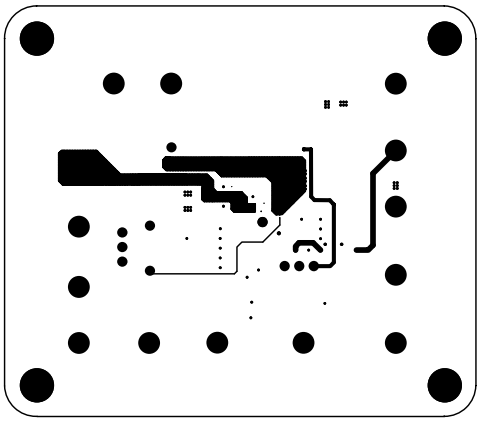
Top-layer



Middle ground layer 1

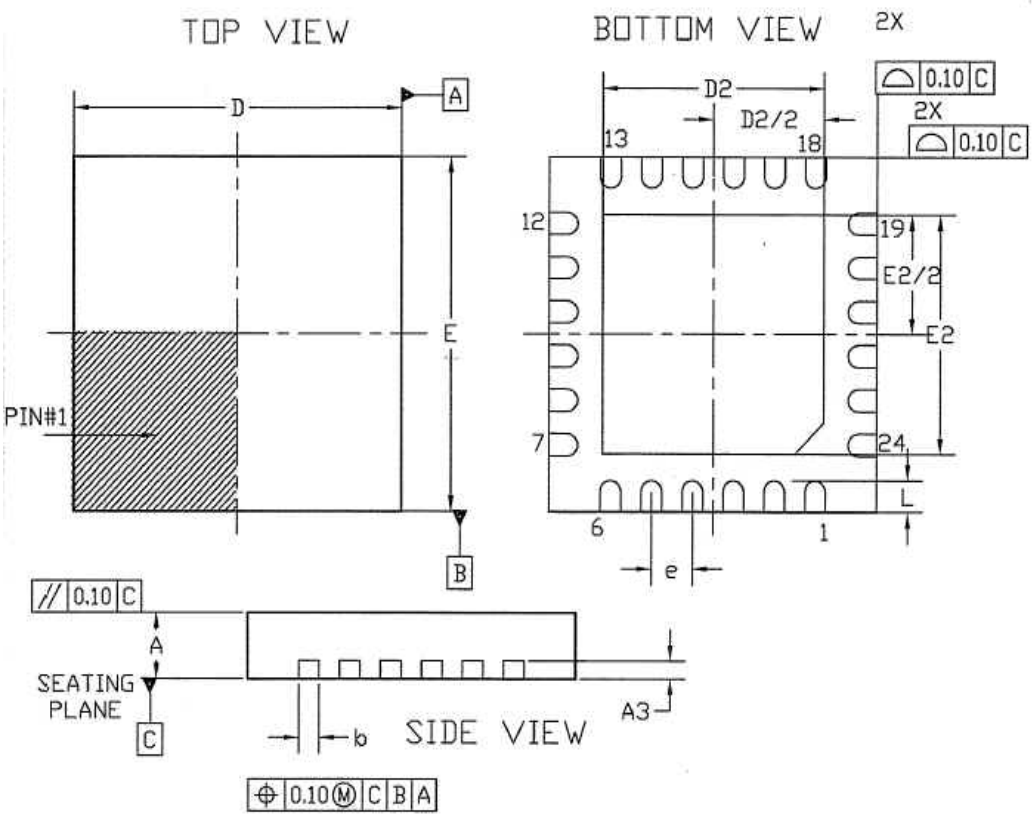


Middle ground layer 2



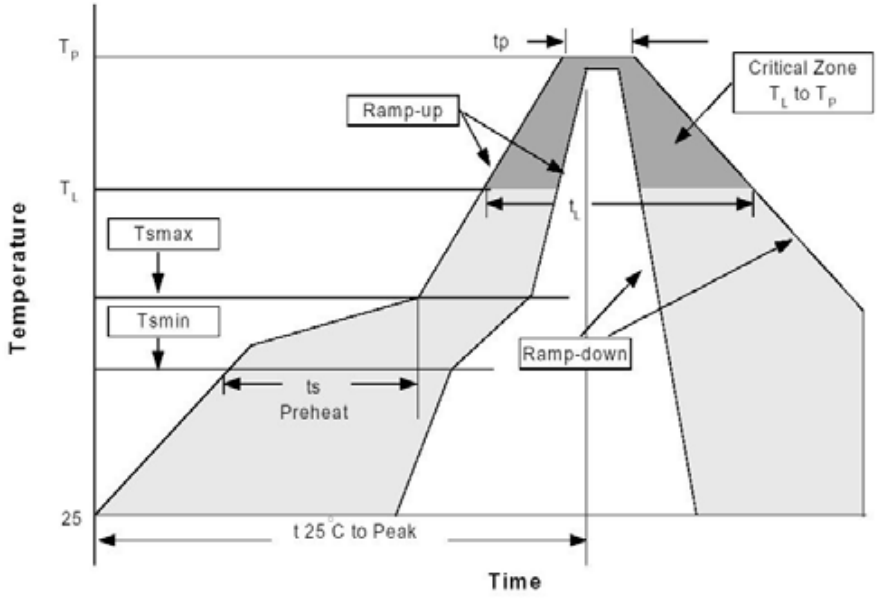
Bottom-layer

Package Outline: Thin QFN-24



SYMBOL	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.027	0.029	0.031
A3	0.195	0.203	0.211	0.0077	0.008	0.0083
b	0.18	0.23	0.30	0.007	0.009	0.012
D	3.925	4.0	4.075	0.154	0.157	0.160
D2	2.50	2.65	2.80	0.098	0.104	0.110
E	3.925	4.0	4.075	0.154	0.157	0.160
E2	2.50	2.65	2.80	0.098	0.104	0.110
e	0.50 BSC			0.02 BSC		
L	0.30	0.35	0.40	0.012	0.014	0.016

Reflow Profiles



Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm^3	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm^3**	**Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm^3**	**Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm^3**
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat -Temperature Min(Tsmin) -Temperature Max (Tsmax) -Time (min to max)(ts)	 100°C 150°C 60-120 seconds		 150°C 200°C 60-180 seconds	
Tsmax to T_L -Ramp-up Rate			3°C/second max.	
Time maintained above: -Temperature (T_L) -Time (t_L)	 183°C 60-150 seconds		 217°C 60-150 seconds	
Peak Temperature(T_P)	225+0/-5°C	240+0/-5°C	245+0/-5°C	250+0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

***All temperatures refer to topside of the package, measured on the package body surface.**