Aimtron
圓創科技股份有限公司

# 2A/18V/300KHz Step-Down Voltage Regulator

## Feature

- 4.75V to 18V Supply Voltage Operating Range.
- 300KHz Fixed Switching Frequency.
- Voltage-Mode PWM Step-Down Regulator.
- Built-in Power MOSFET, Rds(on)≒100mΩ.
- 2A Output Current, Up to 91.9% Efficiency
- Shutdown Current less than 25uA.
- Built-in Soft-Start.
- Cycle-by-Cycle Current-Limit Protection.
- Short Circuitry Protection.
- Under-Voltage Lockout Protection.
- Output Voltage Adjustable up to 16V.
- SOP-8 Package.

## Application

- Distributed Power Systems
- Battery Charger.
- Palmtop Computers, PDAs.
- DSL Modems

## Description

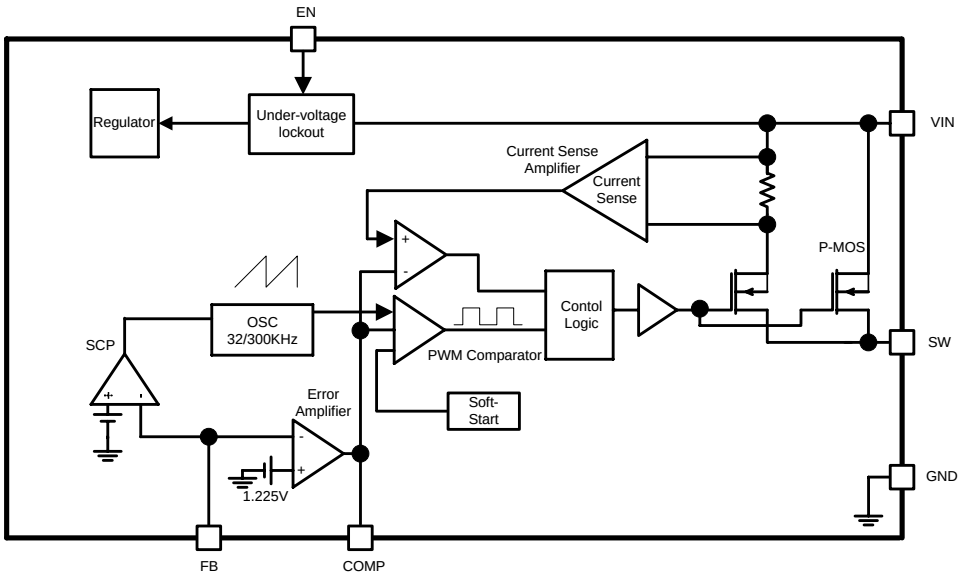
AT1792 is a voltage-mode PWM step-down DC-DC converter capable of driving up to 2A loads over a wide input supply range with excellent line and load regulation characteristics. High efficiency is obtained through the use of a low Rds(on) P-channel power switch.

It uses a fixed switching frequency up to 300KHz thus allowing smaller sized components. The output voltage level is user-programmable via an external resistive voltage divider. The built-in soft-start can reduce inrush current on the input source at turn on.

The device also has built-in cycle-by-cycle current-limit, under-voltage lockout and an ON/OFF logic-control that can power down the regulator to a shutdown mode. In shutdown mode the regulator draws less than 20uA of supply current. When a short circuit is detected on the output , the device immediately change switching frequency to 32 KHz and duty cycle is limited to 5% to protect IC from damage.

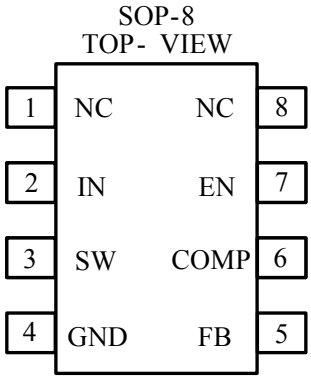
AT1792 is available in SOP-8 package.

## Block Diagram




**Aimtron reserves the right without notice to change this circuitry and specifications.**

## Pin Configuration




## Ordering Information

| Part number | Package | Marking |
|---|---|---|
| AT1792S_GRE | SOP-8, Green | AT1792S, Date Code with one bottom line |

**▲▲▲▲▲ : Date Code**

**For more marking information, contact our sales representative directly*

## Pin Descriptions

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 1 | N/C | | No Connect |
| 2 | IN | P | Power Input. IN supplies power to the IC and Step-down converter switch. IN must be bypassed with a ceramic 0.1uF capacitor. |
| 3 | SW | O | Power Switching Output. |
| 4 | GND | P | Ground. |
| 5 | FB | I | Feedback Input. Connect a resistive divider from switching output to FB to ground. |
| 6 | COMP | O | Error Amplifier Output. A series RC network connected to this pin compensates AT1792. |
| 7 | EN | I | Enable input. EN is a digital input that turns the regulator on/off. Drive EN high to turn on the regulator, drive it low to turn it off. |
| 8 | N/C | | No Connect |

## Absolute Maximum Ratings [*1]

| Parameter | | Rated Value | unit |
|---|---|---|---|
| IN voltage | | -0.3 to 19 | V |
| EN voltage | | -0.3 to 5 | V |
| SW voltage | | -1 to IN+1 | V |
| FB, COMP voltage | | -0.3 to 6 | V |
| Thermal Resistance of Junction-to-Ambient [*2] | | 105 | °C/W |
| Power Consumption | | 620 | mW |
| Junction Temperature | | 150 | °C |
| Lead Temperature(Soldering 10sec) | | 260 | °C |
| Storage Temperature | | -65~+150 | °C |
| ESD Susceptibility [*3] | HBM | 2 | KV |
| | MM | 200 | V |

**1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

**2. Measured on approximately 1" square of 1 oz. copper FR4 board.**

**3. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.**

## Recommended Operation Conditions

| Parameter | Symbol | Values | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Power supply voltage | IN | 4.75 | 12 | 18 | V |
| Operating temperature | Top | -20 | +25 | +85 | ℃ |

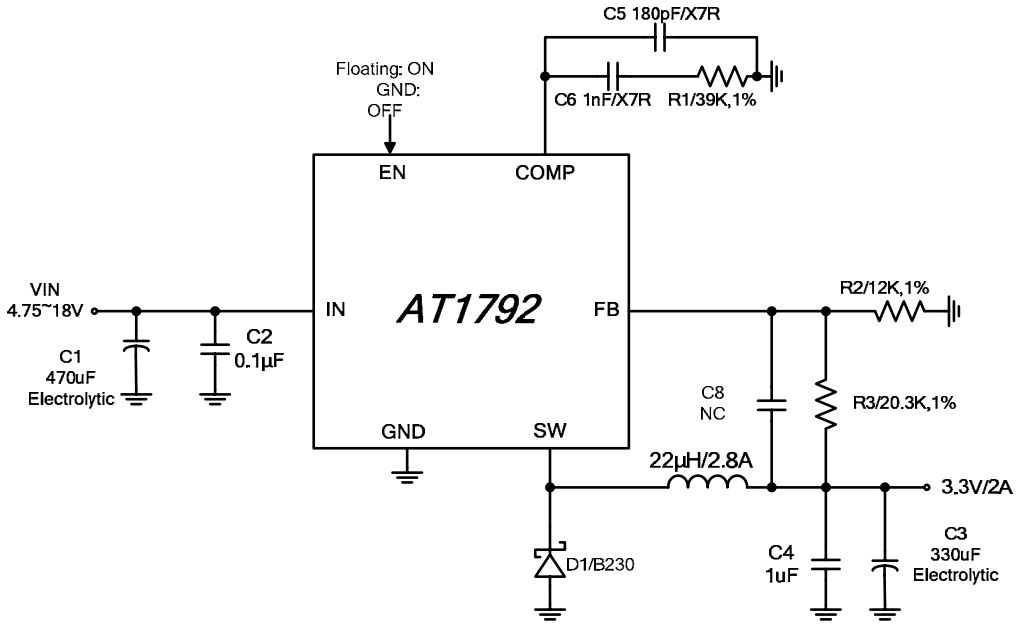
## Electrical Characteristics

(IN=12V, EN=5V, $T_A$=+25℃, unless otherwise noted)

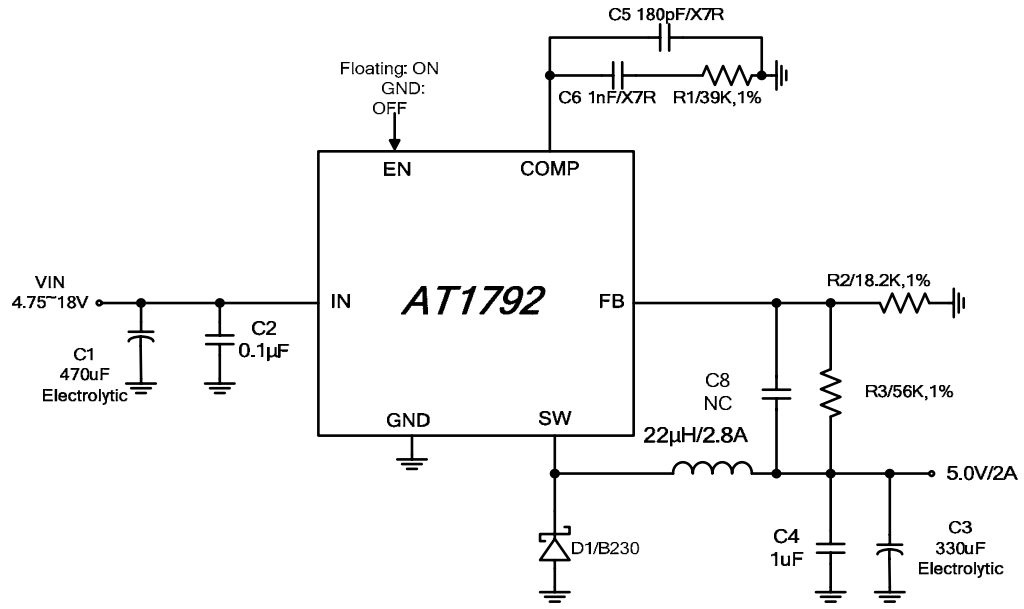
| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input operating voltage | IN | | 4.75 | 12 | 18 | V |
| Input under-voltage lockout threshold | $V_{UVLO}$ | IN Rising | 3.8 | 4.2 | 4.6 | V |
| UVLO hysteresis | | | - | 700 | - | mV |
| Quiescent Current | Iin | $V_{FB}$=1.5V | - | 3.5 | - | mA |
| Shutdown Current | $I_{SHDN}$ | EN =GND | - | 25 | 50 | uA |
| Oscillator Frequency | $f_{SW}$ | Ta=+25°C | - | 300 | 330 | KHz |
| Short-Circuit Frequency | | FB=0V | - | 32 | - | KHz |
| Feedback Regulation voltage | $V_{FB}$ | $T_A$=+25°C | 1.206 | 1.225 | 1.244 | V |
| | | $T_A$ =-20°C~+85°C | 1.176 | 1.225 | 1.274 | V |
| FB Input Bias Current | $I_{FB}$ | $V_{FB}$=1.225V | -50 | - | 50 | nA |
| Current limit*1 | | Min. On-time>0.5μs $T_A$ =+25°C | 2.5 | 3.0 | - | A |
| Maximum Duty Cycle | $D_{MAIN}$ | FB=1.0V | - | - | 100 | % |
| Minimum Duty Cycle | $D_{MIIN}$ | FB=1.5V | 0 | - | - | % |
| SW Switch On-Resistance | $R_{SW-DS(ON)}$ | $I_{SW}$=2A | - | 100 | - | mΩ |
| SW Leakage Current | $I_{SW}$ | IN=13.5V,$V_{SW}$=GND , EN=0V | - | 0.1 | 20 | μA |
| Load Regulation | | 0 A<$I_{SW}$< 2.0A | | 0.2 | | % |
| Line Regulation | | 4.75V < IN<18V | - | 1.0 | - | %/V |
| Error Amplifier Trans-conductance | | | 200 | 300 | 400 | μA/V |
| Soft-Start Time | | | - | 10 | - | ms |
| EN Threshold Voltage | | Hysteresis 150mV | - | 1.5 | - | V |
| EN Pull Up Current | | EN=0V | 2 | -- | - | μA |

*1. Increase current limit 0.015A/°C

## Typical Application Circuit



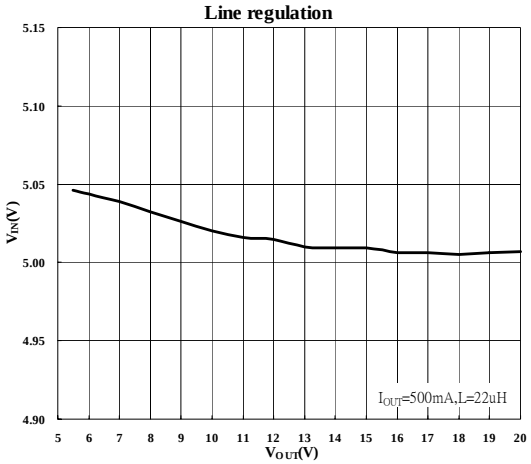

*C2 must be closed to the IC

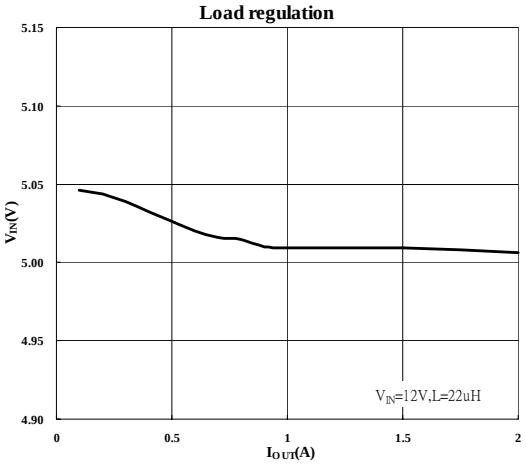


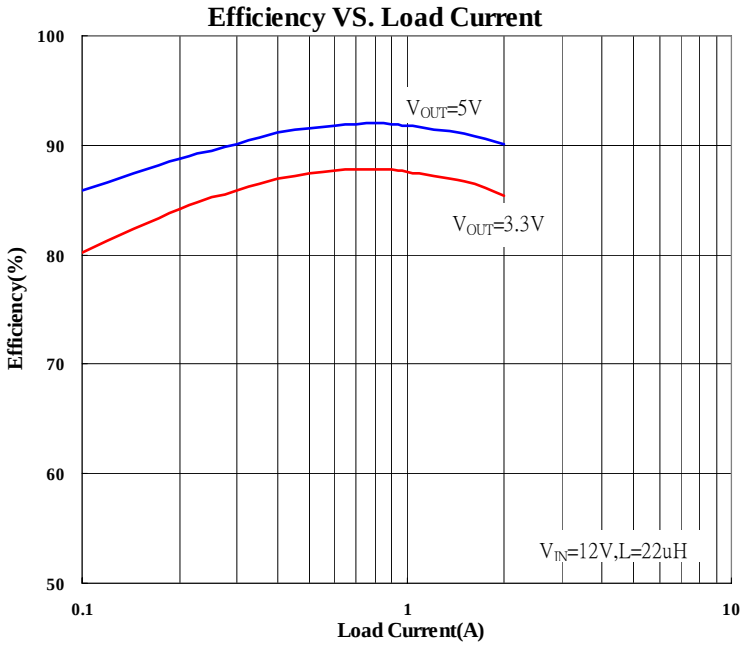

*C2 must be closed to the IC

| $V_{IN}$ | $C_1$ |
|---|---|
| 4.75V~15V | 220µF |
| 15V~18V | 470µF |

## Typical characteristics



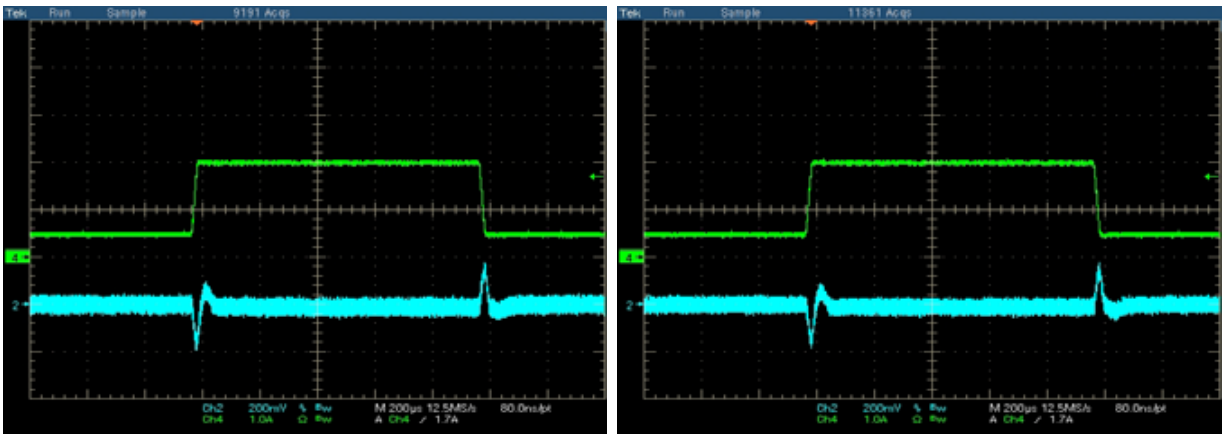



## Typical characteristics

**Load Transient Response**

$V_{IN}$=12V, $V_{OUT}$=5.0V, L=22uH, $I_{OUT}$=500mA to 2A

C4=0.1μF C4=1μF

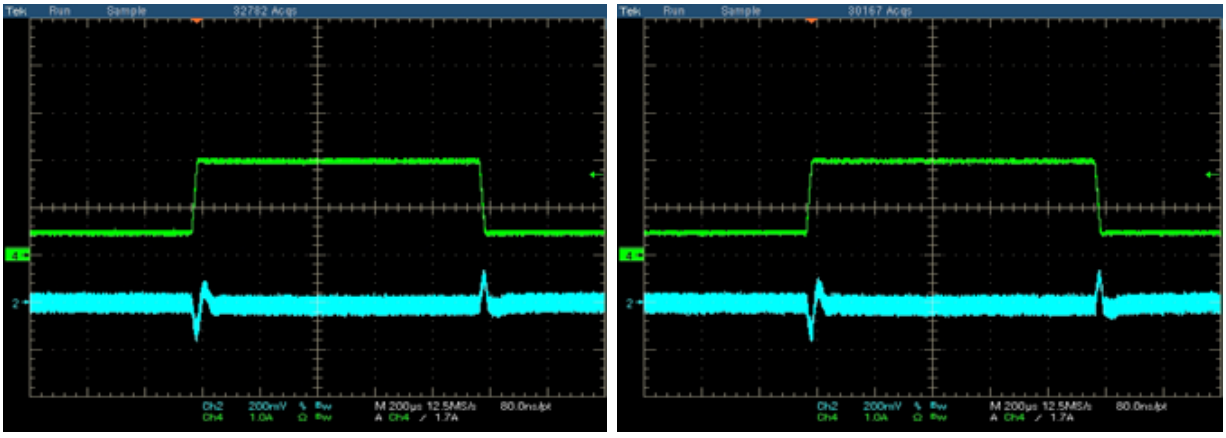


CH2:$V_{OUT}$(AC), CH4:$I_{OUT}$, Time:200μs/div

**Load Transient Response**

$V_{IN}$=18V, $V_{OUT}$=5.0V, L=22uH, $I_{OUT}$=500mA to 2A

C4=0.1μF C4=1μF



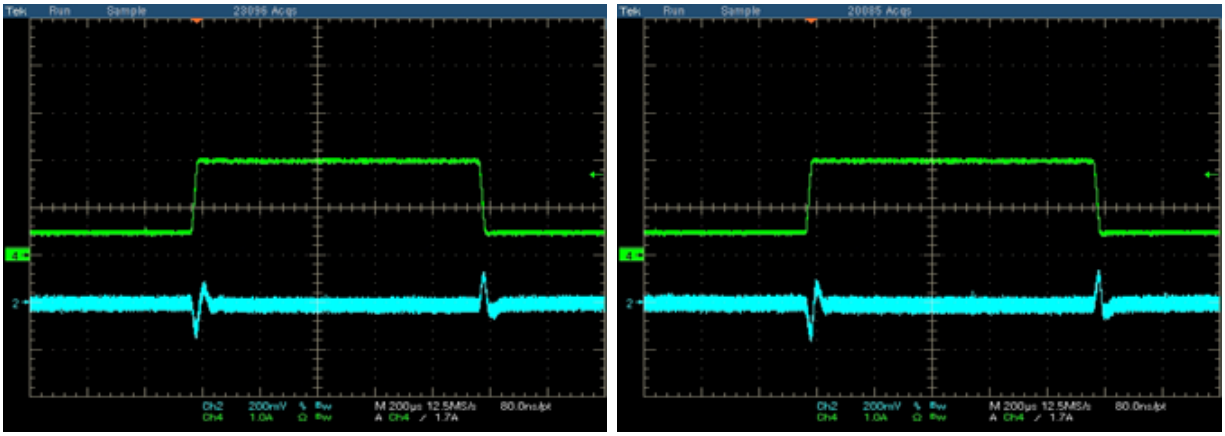
CH2:$V_{OUT}$(AC), CH4:$I_{OUT}$, Time:200μs/div

## Typical characteristics

**Load Transient Response**

$V_{IN}$=12V, $V_{OUT}$=3.3V, L=22uH, $I_{OUT}$=500mA to 2A

C4=0.1µF C4=1µF

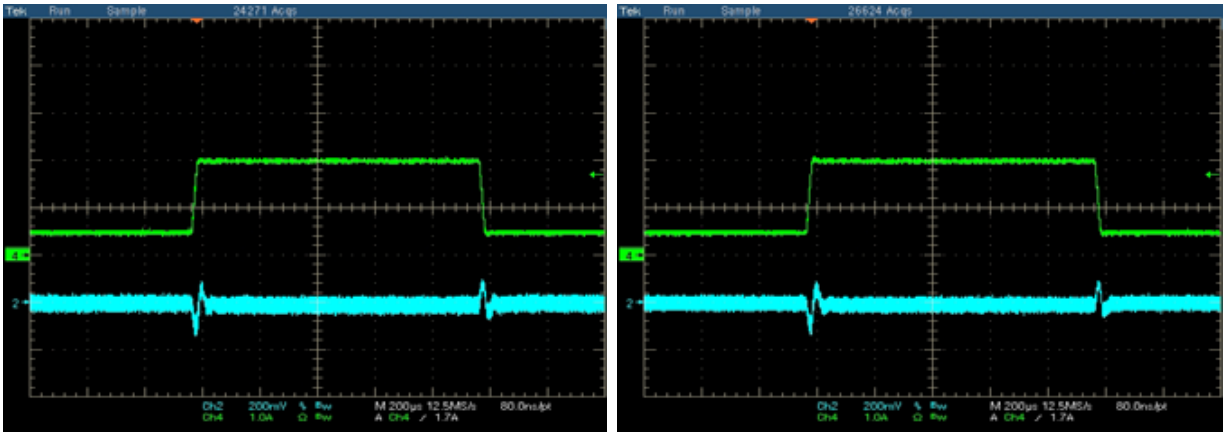


CH2:$V_{OUT}$(AC), CH4:$I_{OUT}$, Time:200µs/div

**Load Transient Response**

$V_{IN}$=18V, $V_{OUT}$=3.3V, L=22uH, $I_{OUT}$=500mA to 2A

C4=0.1µF C4=1µF



CH2:$V_{OUT}$(AC), CH4:$I_{OUT}$, Time:200µs/div

## General Description

The AT1792 features a PWM step-down converter operating with a fixed switching frequency of 300 KHz and uses internal power MOSFET to provide maximum efficiency. The output voltage of the converter can be set as low as 1.225V with external resistive divider. When trans-conductance signal is higher than saw-tooth wave, then PWM comparator will produce ON-time signal to set internal flip-flop, which turns on the switching power MOSFET. The external inductor current ramps up linearly, storing energy in a magnetic field. Once peak current of flowing through switching power MOSFET over current-limited threshold or trans-conductance signal level is lower than saw-tooth wave, the switching power MOSFET will turns off, the flip-flop resets, and external schottky diode turns on. This forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and load. To add higher flexibility to the selection of external component values, the device uses external loop compensation.

### Enable Control

Digital logic of EN provides an electrical ON/OFF control of the power supply. Connecting this pin to ground or to any voltage less than 1.0V will completely turn OFF the regulator. In this state, current drain from the input supply is only 25μA, the internal reference, error amplifier, comparators, and biasing circuitry turn off . When EN control is not required that it should be left open circuited.

### Soft-Start

AT1792 is built-in soft-start function. When power up, after input voltage is above the under-voltage lockout threshold, then soft-start allows a gradual increase of COMP voltage to get to a steady state operating point. Therefore, reducing input surge currents. During this time, the COMP voltage increases and the output duty cycle is allowed to increase from zero to the value required for regulation. The maximum load current is available after the soft-start cycle is completed. When EN pin is taken low, the soft-start capacitor is discharge to ground.

### Short-Circuit Protection

If feedback voltage of the regulator falls below 0.85V, the oscillator clock switched operating frequency to 32KHz and duty cycle is limited to 5% to reduce input power delivered to output. If the short circuitry is not removed, the protection circuitry will activate sustainability. When short-circuit problem is to eliminate, oscillator clock will switch back to 300KHz automatically.

**Cycle-by-Cycle Over-Current Protection**

The AT1792 provides cycle-by-cycle over-current protection. Current limit is accomplished using a separate dedicated comparator. If the current sense amplifier output voltage is larger than current-limited threshold level, it will be immediately turned off power MOS. The current-limit feature protects against a hard short or over current fault at the output.

**Applications Information**

External components of step-down converter can be designed by performing simple calculations. It must be to follow regulation by the output voltage and the maximum load current, as well as maximum and minimum input voltages. Begin by selecting an inductor value, then choose the diode and capacitors.

**Inductor**

Inductor selection depends on input voltage, output voltage, maximum current, switching frequency and availability of inductor values. The following buck circuit equations are useful in choosing the inductor values based on the application. Choose an inductor that does not saturate under the maximum rating load conditions. The magnitude of inductance is selected to maintain a peak to peak ripple current of 30% of the maximum load current.

The peak inductor current is given by:

$$I_{Lpeak} = I_{LAVG} + \frac{\Delta I_L}{2}$$

$$I_{LAVG} = \frac{I_{in}}{D}$$

$$D = \frac{V_O}{V_{in}}$$

D is the MOSFET turn on ratio

where:

$\triangle I_L$ is the inductor peak-to-peak current ripple and is decided by:

$$\Delta I_L = \frac{V_{in} - V_O}{L} \times \frac{D}{f_{OSC}} \Rightarrow L = \frac{(V_{in} - V_O) \times D}{\Delta I_L \times f_{OSC}}$$

$f_{OSC}$ is the switching frequency.

The inductor should be chosen to be able to handle this current and inductor saturation current rating should be greater than $I_{PEAK}$.

**Diode selection**

When the power switch turns off, the current through the inductor continues to flow. The path for this current is through the diode connected between the switch output and ground. This forward biased diode must has a minimum voltage drop and recovery times. Schottky diode is recommended and it should be able to handle those current. As usual, the reverse voltage rating of the diode should be at least 1.3 times greater than the maximum input voltage, and current rating is greater than the maximum load current.

**Feedback Resistor Network**

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 100kΩ is recommended. The buck converter output voltage is determined by the following relationship:

$$V_O = V_{REF} \times \left(1 + \frac{R_3}{R_2}\right)$$

where $V_{REF}$ =1.225V as specified.

**Input capacitor**

An input capacitor helps to provide additional current to the power supply as well as smooth input voltage variations in high current switching regulators. When selecting an input capacitor, a low ESR capacitor is required to keep the noise at the IC to a minimum. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose an input capacitor with maximum voltage rating is 1.3 times greater than the maximum input voltage, and RMS current rating is equal to one-half of the maximum dc load current. It may be necessary in some designs to add a small valued ceramic type capacitor in parallel with the input capacitor to prevent any ring.

**Output Capacitor**

The output capacitor acts to smooth the dc output voltage and also provides energy storage. Selection of an output capacitor, with an associated equivalent series resistance (ESR), impacts both the amount of output ripple voltage and stability of the control loop. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple is estimated to be:

$$\Delta V_{ripple} = \frac{(1-D) \times V_O}{8 \times L \times C_{OUT} \times f_{OSC}^2}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging or discharging of the output capacitor.

In the case of low-ESR electrolytic capacitors, Output ripple voltage drop caused by the switching current through the ESR of the output capacitor. The output ripple is estimated as:

$V_{RIPPLE} \cong \Delta I_L \times R_{ESR}$

Impacting frequency stability of the overall control loop, the output capacitance, in conjunction with the inductor, creates a double pole inside the feedback loop. In addition the capacitance and the ESR value create a zero. These frequency response effects together with the internal frequency compensation circuitry of AT1792 modify the gain and phase shift of the closed loop system.

**Compensation**

The step-down loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is connected to the output of the internal trans-conductance error amplifier. The compensation capacitor adjusts the low frequency gain , and the series resistor value adjusts the high frequency gain. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system. The system has 2 poles and one zero of importance, 2 poles consist of compensation capacitor and output capacitor. One zero is produced by the compensation capacitor and the compensation resistor.

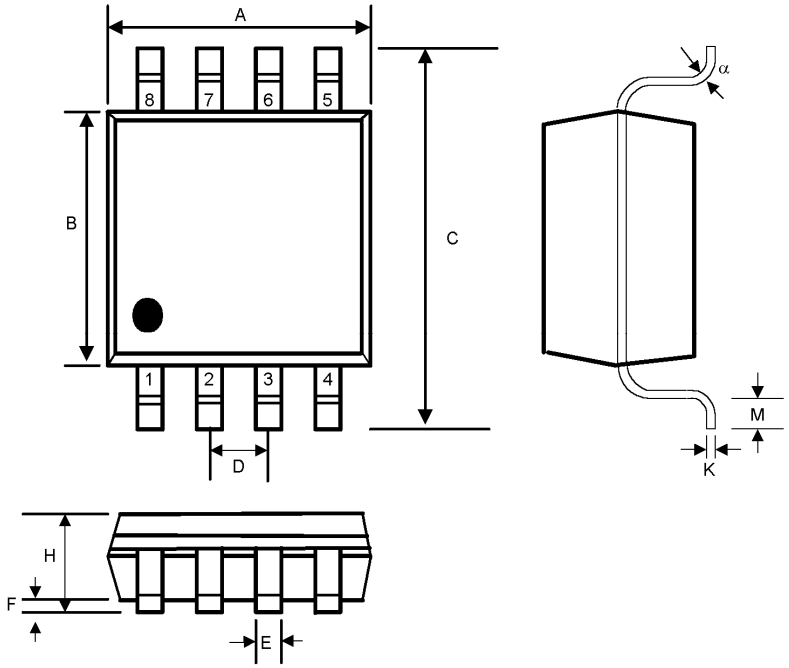
If electrolytic capacitor with relatively high ESR is used, the zero due to the capacitance and ESR of the output capacitor can be compensated by a third pole set by the compensation resistor and another compensation capacitor connected form COMP pin to ground.

**PCB layout guidelines**

Careful printed circuit layout is extremely important to avoid causing parasitical capacitance and line inductance. The following layout guidelines are recommended to achieve optimum performance.

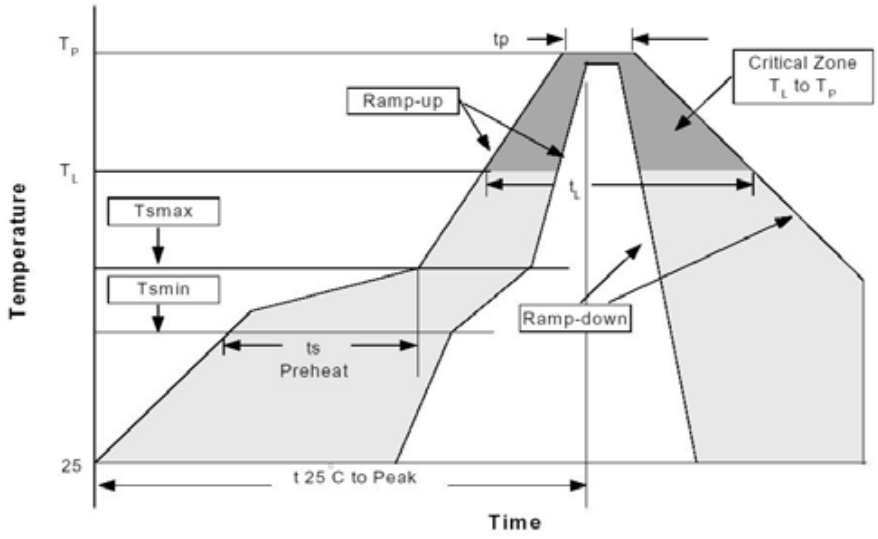
- Please the buck converter diode and inductor close to the SW pin and no via.
- Please ceramic bypass capacitors near the input pin.
- Locate all feedback resistive dividers as close to their respective feedback pins as possible.
- Use wide traces and trace length is short as possible.

**Outline 8-pin SOP**




| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.188 | 0.197 | 4.80 | 5.00 | - |
| B | 0.149 | 0.158 | 3.80 | 4.00 | - |
| C | 0.228 | 0.244 | 5.80 | 6.20 | - |
| D | 0.050 BSC | | 1.27 BSC | | - |
| E | 0.013 | 0.020 | 0.33 | 0.51 | - |
| F | 0.004 | 0.010 | 0.10 | 0.25 | - |
| H | 0.053 | 0.069 | 1.35 | 1.75 | - |
| J | 0.011 | 0.019 | 0.28 | 0.48 | |
| K | 0.007 | 0.010 | 0.19 | 0.25 | |
| M | 0.016 | 0.050 | 0.40 | 1.27 | |
| e1 | $45^{O}$ | | $45^{O}$ | | |
| $\alpha$ | $0^{0}$ | $8^{0}$ | $0^{0}$ | $8^{0}$ | - |

## Reflow Profiles




| Profile Feature | Sn-Pb Eutectic Assembly | | Pb-Free Assembly | |
|---|---|---|---|---|
| | Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm$^3$ | Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm$^3$ | Large Body Pkg. thickness ≥2.5mm or Pkg. volume ≥350mm$^3$ | Small Body Pkg. thickness <2.5mm or Pkg. volume <350mm$^3$ |
| Average ramp-up rate ($T_L$ to $T_P$) | 3°C/second max. | | 3°C/second max. | |
| Preheat<br>-Temperature Min(Tsmin)<br>-Temperature Max (Tsmax)<br>-Time (min to max)(ts) | <br>100°C<br>150°C<br>60-120 seconds | | <br>150°C<br>200°C<br>60-180 seconds | |
| Tsmax to $T_L$<br>-Ramp-up Rate | | | 3°C/second max. | |
| Time maintained above:<br>-Temperature ($T_L$)<br>-Time ($t_L$) | <br>183°C<br>60-150 seconds | | <br>217°C<br>60-150 seconds | |
| Peak Temperature($T_P$) | 225+0/-5°C | 240+0/-5°C | 245+0/-5°C | 250+0/-5°C |
| Time within 5°C of actual Peak Temperature ($t_P$) | 10-30 seconds | 10-30 seconds | 10-30 seconds | 20-40 seconds |
| Ramp-down Rate | 6°C/second max. | | 6°C/second max. | |
| Time 25°C to Peak Temperature | 6 minutes max. | | 8 minutes max. | |

***All temperatures refer to topside of the package, measured on the package body surface.**