TOSHIBA

TENTATIVE   TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

128-MBIT (16M × 8 BITS/8M x 16BITS) CMOS NAND E^{2}PROM

DESCRIPTION

The TC58DxM72x1xxxx is a 128-Mbit (138,412,032) bit NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^{2}PROM) organized as 528 bytes/264 words × 32 pages × 1024 blocks. The device uses dual power supplies (2.7 V to 3.6 V for V$_{CC}$ and 1.65 V to 1.95 V for V$_{CCQ}$). The device has a 528-byte/264-words static register which allows program and read data to be transferred between the register and the memory cell array in 528-byte/256-words increments. The Erase operation is implemented in a single block unit (16 Kbytes + 512 bytes: 528 bytes × 32 pages/8k words + 256 words:264 words × 32 pages).

The TC58DxM72x1xxxx is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.
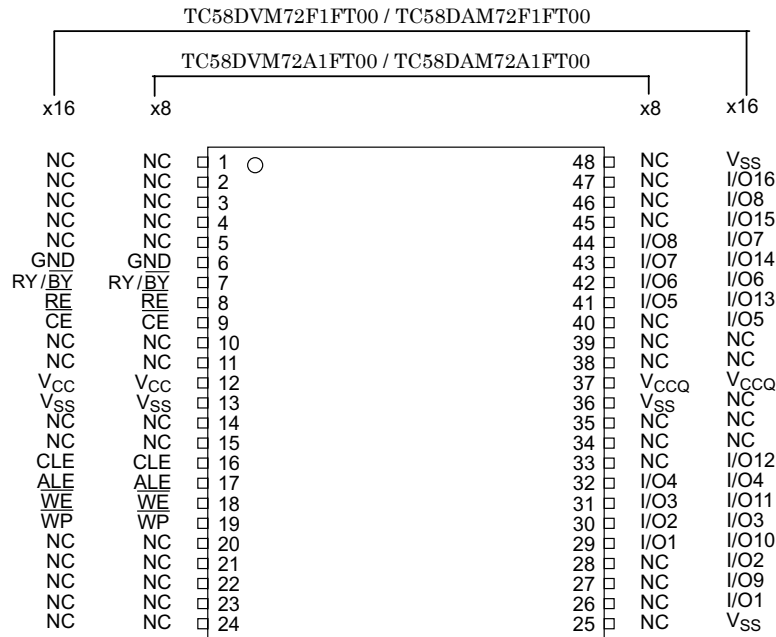
FEATURES

- Organization   TC58DxM72A1xxxx   TC58DxM72F1xxxx
  - Memory cell allay   528 × 32K × 8   264 x 32k x 16
  - Register   528 × 8   264 x 16
  - Page size   528 bytes   264 words
  - Block size   (16K + 512) bytes   (8k + 256) words
- Modes
  - Read, Reset, Auto Page Program
  - Auto Block Erase, Status Read
- Mode control
  - Serial input/output
  - Command control
- Power supply   TC58DVM72x1xxxx   TC58DAM72x1xxxx
  - Vcc: 2.7V to 3.6V   2.7V to 3.6V
  - Vccq: 2.7V to 3.6V   1.65V to 1.95V
- Program/Erase Cycles   1E5 cycle (with ECC)
- Access time
  - Cell array to register   25 μs max
  - Serial Read Cycle   50 ns min
- Operating current
  - Read (50 ns cycle)   10 mA typ.
  - Program (avg.)   10 mA typ.
  - Erase (avg.)   10 mA typ.
  - Standby   50 μA max.
- Package
 - TSOP I 48-P-1220-0.50 (Weight:0.53g typ)

000707EBA1

PIN ASSIGNMENT (TOP VIEW)

TC58DVM72F1FT00 / TC58DAM72F1FT00

TC58DVM72A1FT00 / TC58DAM72A1FT00

x16	x8	Pin	Pin	x8	x16
NC	NC	1 ○	48	NC	Vss
NC	NC	2	47	NC	I/O16
NC	NC	3	46	NC	I/O8
NC	NC	4	45	NC	I/O15
NC	NC	5	44	I/O8	I/O7
GND	GND	6	43	I/O7	I/O14
RY/$\overline{BY}$	RY/$\overline{BY}$	7	42	I/O6	I/O6
$\overline{RE}$	$\overline{RE}$	8	41	I/O5	I/O13
$\overline{CE}$	$\overline{CE}$	9	40	NC	I/O5
NC	NC	10	39	NC	NC
NC	NC	11	38	NC	NC
Vcc	Vcc	12	37	Vccq	Vccq
Vss	Vss	13	36	Vss	NC
NC	NC	14	35	NC	NC
NC	NC	15	34	NC	NC
CLE	CLE	16	33	NC	I/O12
$\overline{ALE}$	$\overline{ALE}$	17	32	I/O4	I/O4
$\overline{WE}$	$\overline{WE}$	18	31	I/O3	I/O11
WP	WP	19	30	I/O2	I/O3
NC	NC	20	29	I/O1	I/O10
NC	NC	21	28	NC	I/O2
NC	NC	22	27	NC	I/O9
NC	NC	23	26	NC	I/O1
NC	NC	24	25	NC	Vss

PINNAMES

I/O1 to I/O8	I/O port
I/O9 to I/O16	I/O port (x16)
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY/$\overline{BY}$	Ready/Busy
GND	Ground input
V_{CC}	Power supply
V_{CCQ}	I/O port Power supply
V_{SS}	Ground

BLOCK DIAGRAM
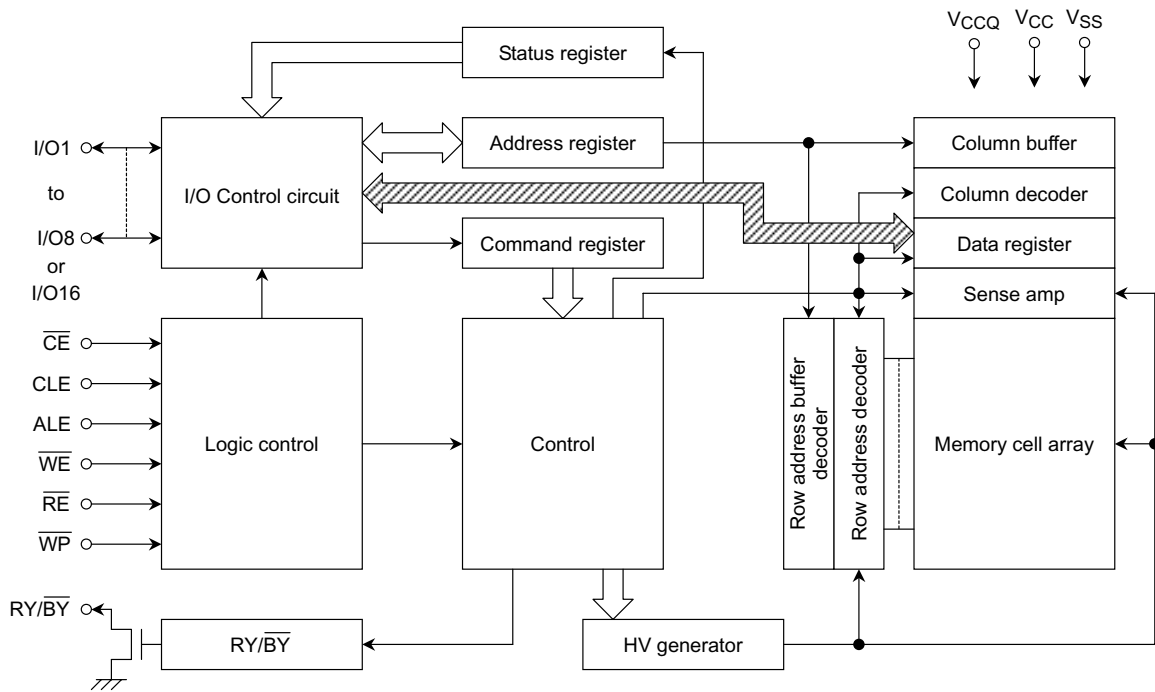
ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE		unit
		TC58DVxxxxx	TC58DAxxxx	
V_{CC}	Power Supply Voltage	−0.6~4.6	−0.6~4.6	V
V_{CCQ}	I/O port Power Supply Voltage	−0.6~4.6	−0.6~2.6	V
V_{IN}	Input Voltage for Control pins	−0.6~4.6	−0.6~2.6	V
$V_{I/O}$	Input/Output Voltage for I/O pins	−0.6 V~V_{CCQ} + 0.3 V ($\leqq$ 4.6 V)	−0.6 V~V_{CCQ} + 0.3 V ($\leqq$ 2.6 V)	
P_D	Power Dissipation	0.3	0.3	W
T_{solder}	Soldering Temperature(10s)	260	260	°C
T_{stg}	Storage Temperature	−55~150	−55~150	°C
T_{opr}	Operating Temperature	0~70	0~70	°C

CAPACITANCE *(Ta =25°C, f= 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS (1)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	1004	—	1024	Blocks

(1) The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.

(2) The first block (block address #00) is guaranteed to be a valid block at the time of shipment.

RECOMMENDED DC OPERATING CONDITIONS

TC58DVM72A1xxxx,TC58DVM72F1xxxx

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	3.3	3.6	V
V_{CCQ}	I/O Port Power Supply Voltage	2.7	3.3	3.6	V
V_{IH}	High Level input Voltage	2.0	—	$V_{CCQ} + 0.3$	V
V_{IL}	Low Level Input Voltage	−0.3*	—	0.8	V

* −2 V (pulse width lower than 20 ns)

TC58DAM72A1xxxx,TC58DAM72F1xxxx

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	3.3	3.6	V
V_{CCQ}	I/O Port Power Supply Voltage	1.65	1.8	1.95	V
V_{IH}	High Level input Voltage	V_{CCQ} X 0.78	—	$V_{CCQ} + 0.3$	V
V_{IL}	Low Level Input Voltage	−0.3*	—	V_{CCQ} X 0.22	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CCQ}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CCQ}	—	—	±10	μA
I_{CCO1}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, t_{cycle} = 50 ns	—	10	30	mA
I_{CCO3}	Operating Current (Command Input)	t_{cycle} = 50 ns	—	10	30	mA
I_{CCO4}	Operating Current (Data Input)	t_{cycle} = 50 ns	—	10	30	mA
I_{CCO5}	Operating Current (Address Input)	t_{cycle} = 50 ns	—	10	30	mA
I_{CCO7}	Programming Current	—	—	10	30	mA
I_{CCO8}	Erasing Current	—	—	10	30	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = $V_{IH,}$ $\overline{WP}$ = 0 V/V_{CCQ}	—	—	1	mA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CCQ} − 0.2 V, $\overline{WP}$ = 0 V/V_{CCQ}	—	10	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = −0.5 mA	V_{CCQ} -0.5	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA	—	—	0.4	V
I_{OL} (RY/$\overline{BY}$)	Output Current of RY/$\overline{BY}$ pin	V_{OL} = 0.4 V	—	8	—	mA

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AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS
(Ta = 0° to 70°C, V$_{CC}$ = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t$_{CLS}$	CLE Setup Time	0	—	ns	
t$_{CLH}$	CLE Hold Time	10	—	ns	
t$_{CS}$	$\overline{CE}$ Setup Time	0	—	ns	
t$_{CH}$	$\overline{CE}$ Hold Time	10	—	ns	
t$_{WP}$	Write Pulse Width	25	—	ns	
t$_{ALS}$	ALE Setup Time	0	—	ns	
t$_{ALH}$	ALE Hold Time	10	—	ns	
t$_{DS}$	Data Setup Time	20	—	ns	
t$_{DH}$	Data Hold Time	10	—	ns	
t$_{WC}$	Write Cycle Time	50	—	ns	
t$_{WH}$	$\overline{WE}$ High Hold Time	15	—	ns	
t$_{WW}$	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns	
t$_{RR}$	Ready to $\overline{RE}$ Falling Edge	20	—	ns	
t$_{RP}$	Read Pulse Width	35	—	ns	
t$_{RC}$	Read Cycle Time	50	—	ns	
t$_{REA}$	$\overline{RE}$ Access Time (Serial Data Access)	—	35	ns	
t$_{CEA}$	$\overline{CE}$ Access Time (Serial Data Access,ID Read)	—	45	ns	
t$_{ALEA}$	ALE Access Time (ID Read)	—	45	ns	
t$_{CEH}$	$\overline{CE}$ High Time for Last Address in Serial Read Cycle	100	—	Ns	(2)
t$_{REAID}$	$\overline{RE}$ Access Time (ID Read)	—	35	ns	
t$_{OH}$	Data Output Hold Time	10	—	ns	
t$_{RHZ}$	$\overline{RE}$ High to Output High Impedance	—	30	ns	
t$_{CHZ}$	$\overline{CE}$ High to Output High Impedance	—	20	ns	
t$_{REH}$	$\overline{RE}$ High Hold Time	15	—	ns	
t$_{IR}$	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns	
t$_{RSTO}$	$\overline{RE}$ Access Time (Status Read)	—	35	ns	
t$_{CSTO}$	$\overline{CE}$ Access Time (Status Read)	—	45	ns	
t$_{RHW}$	$\overline{RE}$ High to $\overline{WE}$ Low	0	—	ns	
t$_{WHC}$	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns	
t$_{WHR}$	$\overline{WE}$ High to $\overline{RE}$ Low	30	—	ns	
t$_{R}$	Memory Cell Array to Starting Address	—	25	μs	
t$_{WB}$	$\overline{WE}$ High to Busy	—	200	ns	
t$_{AR2}$	ALE Low to $\overline{RE}$ Low (Read Cycle)	50	—	ns	
t$_{RB}$	$\overline{RE}$ Last Clock Rising Edge to Busy(in Sequential Read)	—	200	ns	
t$_{CRY}$	$\overline{CE}$ High to Ready(When interrupted by $\overline{CE}$ in Read Mode)	—	1+ tr(RY/$\overline{BY}$)	μs	(1)(2)
t$_{RST}$	Device Reset Time (Read/Program/Erase)	—	6/10/500	μs	

AC TEST CONDITIONS

PARAMETER	CONDITION	
	TC58DVxxxxx	TC58DAxxxx
Input level	2.4 V, 0.4 V	V$_{CCQ}$ -0.2 V, 0.2 V
Input pulse rise and fall time	3 ns	3 ns
Input comparison level	1.5 V, 1.5 V	0.9 V, 0.9 V
Output data comparison level	1.5 V, 1.5 V	0.9 V, 0.9 V
Output load	C$_L$ (100 pF) + 1 TTL	C$_L$ (30 pF)

Note: (1) $\overline{CE}$ High to Ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document.)

(2) Sequential Read is terminated when t$_{CEH}$ is greater than or equal to 100 ns. If the $\overline{RE}$ to $\overline{CE}$ delay is less than 30 ns, RY/$\overline{BY}$ signal stays Ready.
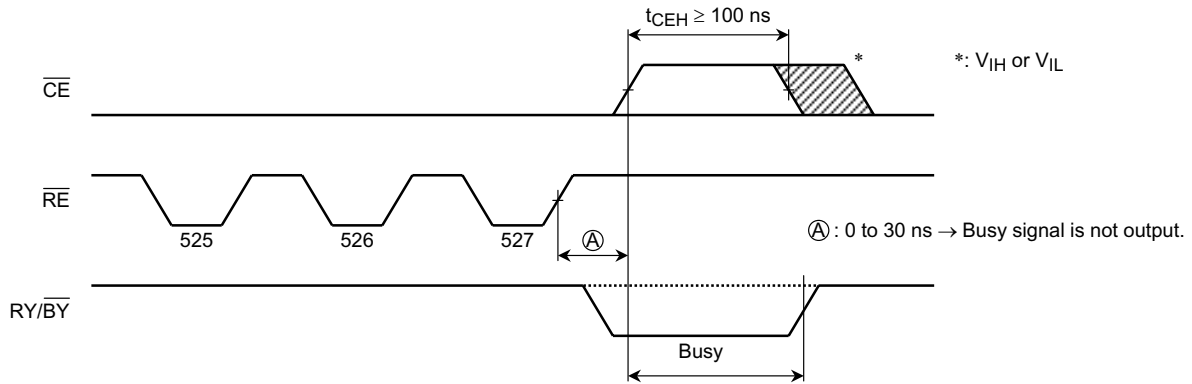
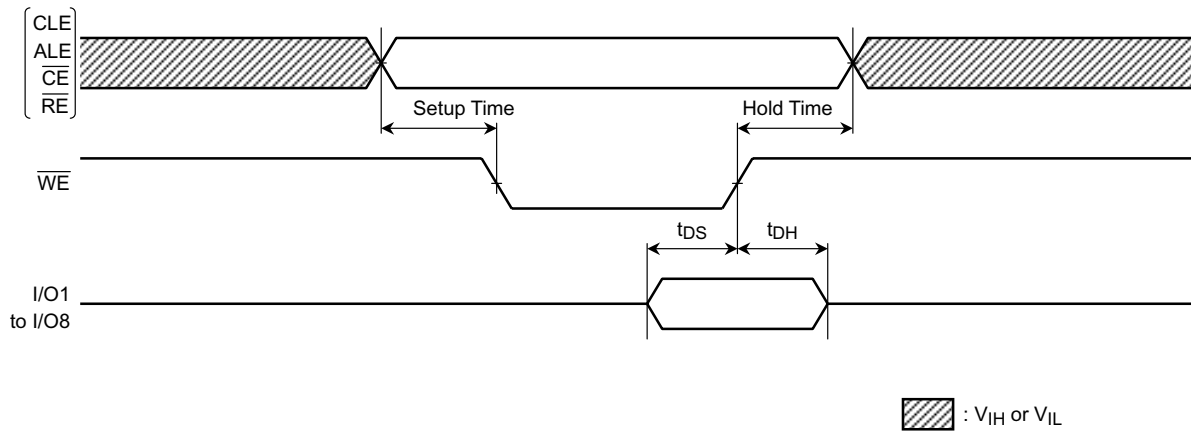
PROGRAMMING AND ERASING CHARACTERISTICS
(Ta =0° to 70°C, V$_{CC}$ = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t$_{PROG}$	Programming Time	—	200	1000	µs	
N	Number of Programming Cycles on Same Page	—	—	3		(1)
t$_{BERASE}$	Block Erasing Time	—	2	10	ms	

(1): Refer to Application Note (12) toward the end of this document.

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TIMING DIAGRAMS

Latch Timing Diagram for Command/Address/Data

Command Input Cycle Timing Diagram
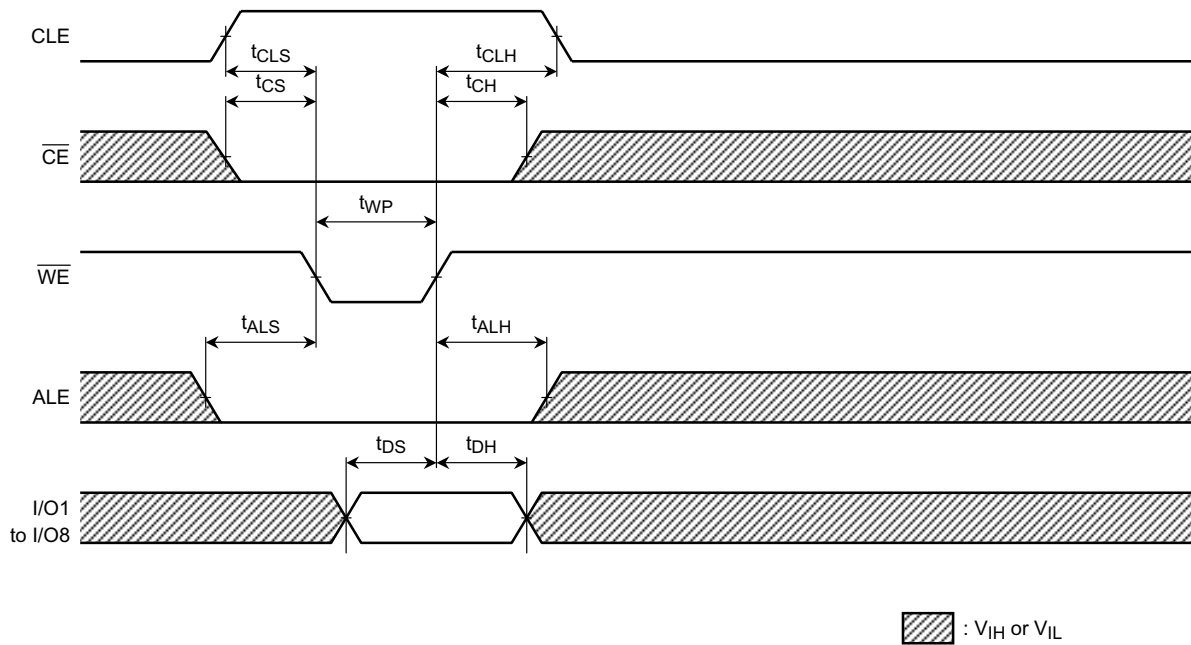
Address Input Cycle Timing Diagram
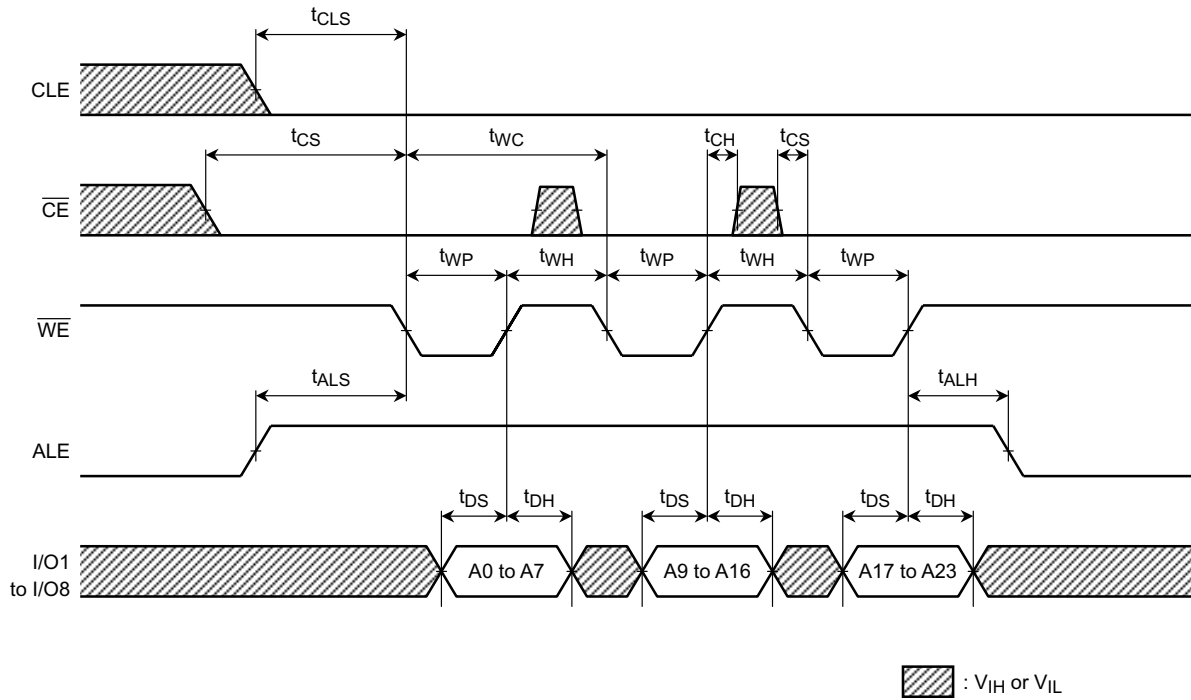
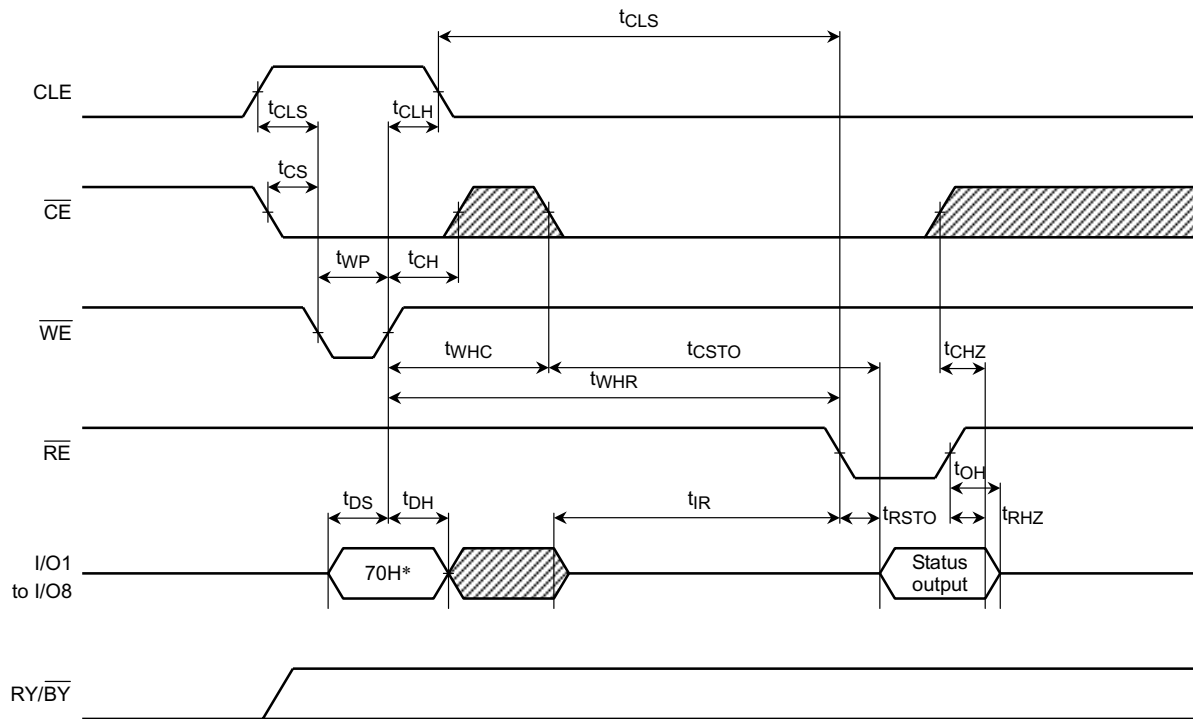$: V_{IH}$ or V_{IL}

Data Input Cycle Timing Diagram
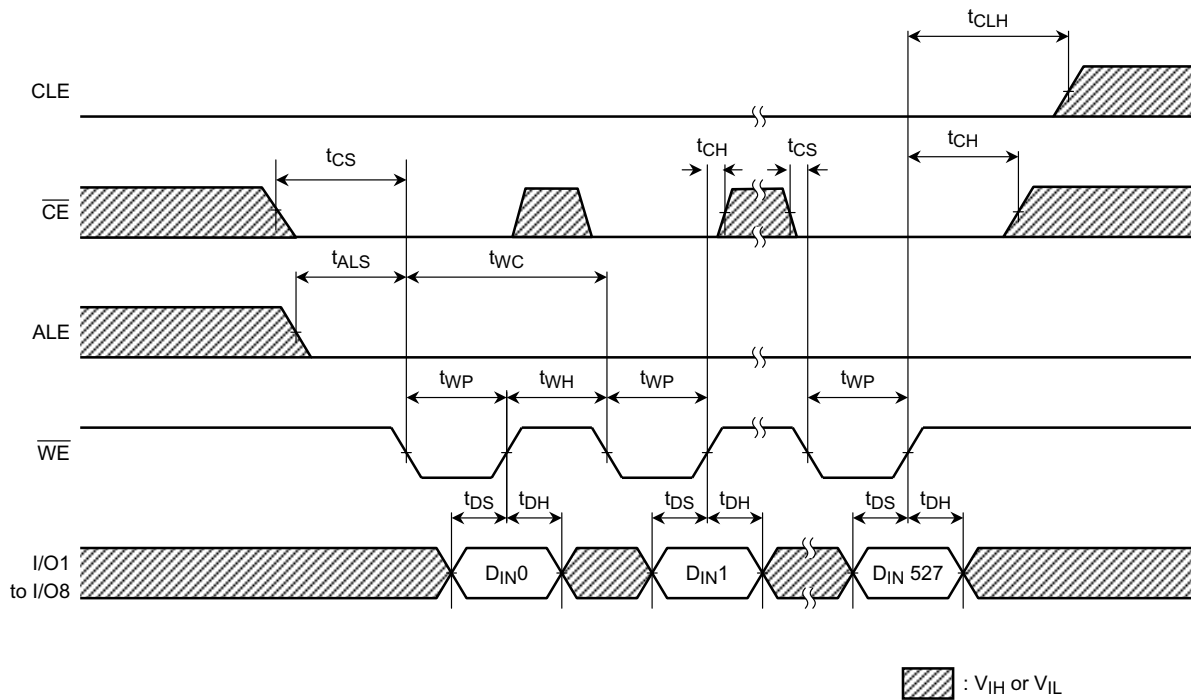
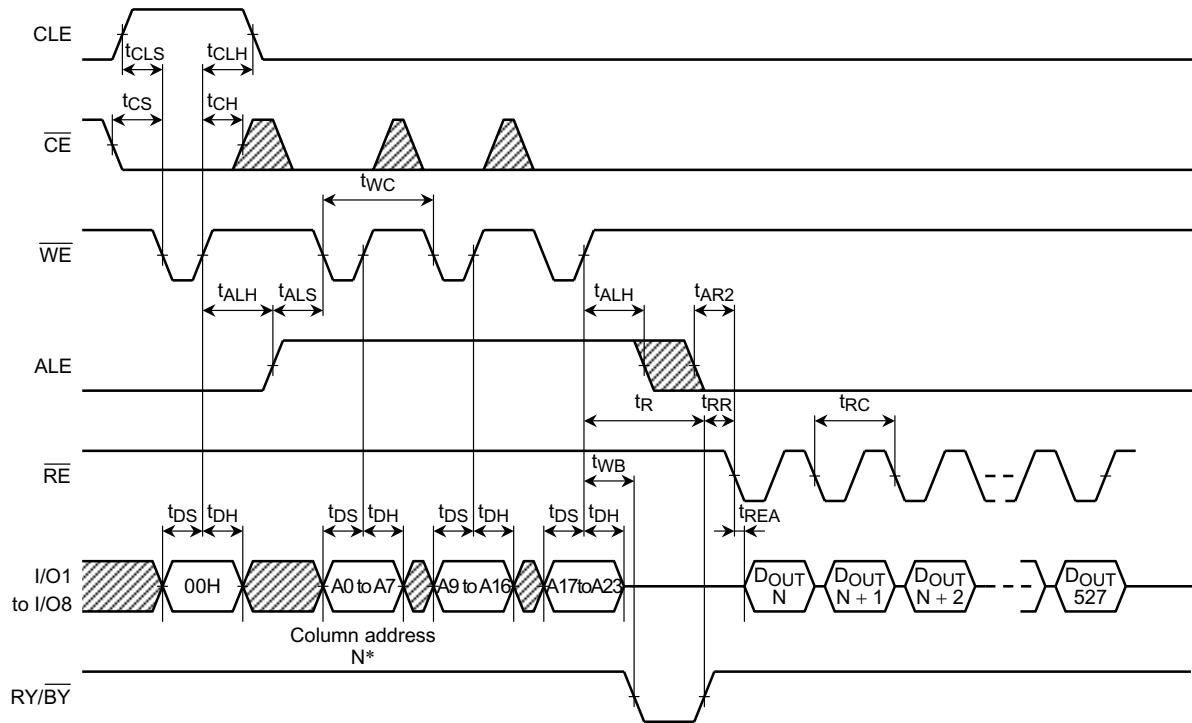$: V_{IH}$ or V_{IL}

Serial Read Cycle Timing Diagram
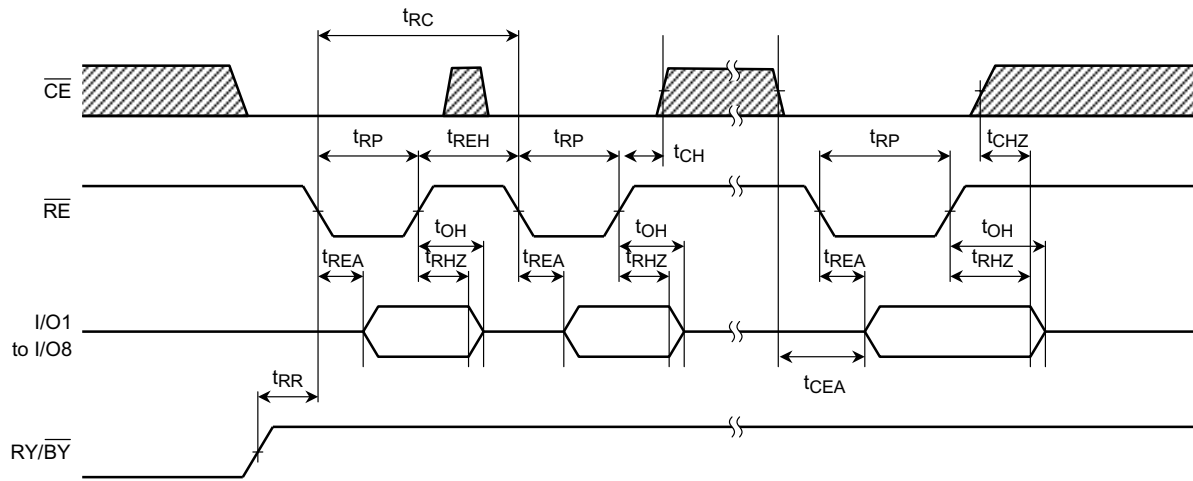
Status Read Cycle Timing Diagram

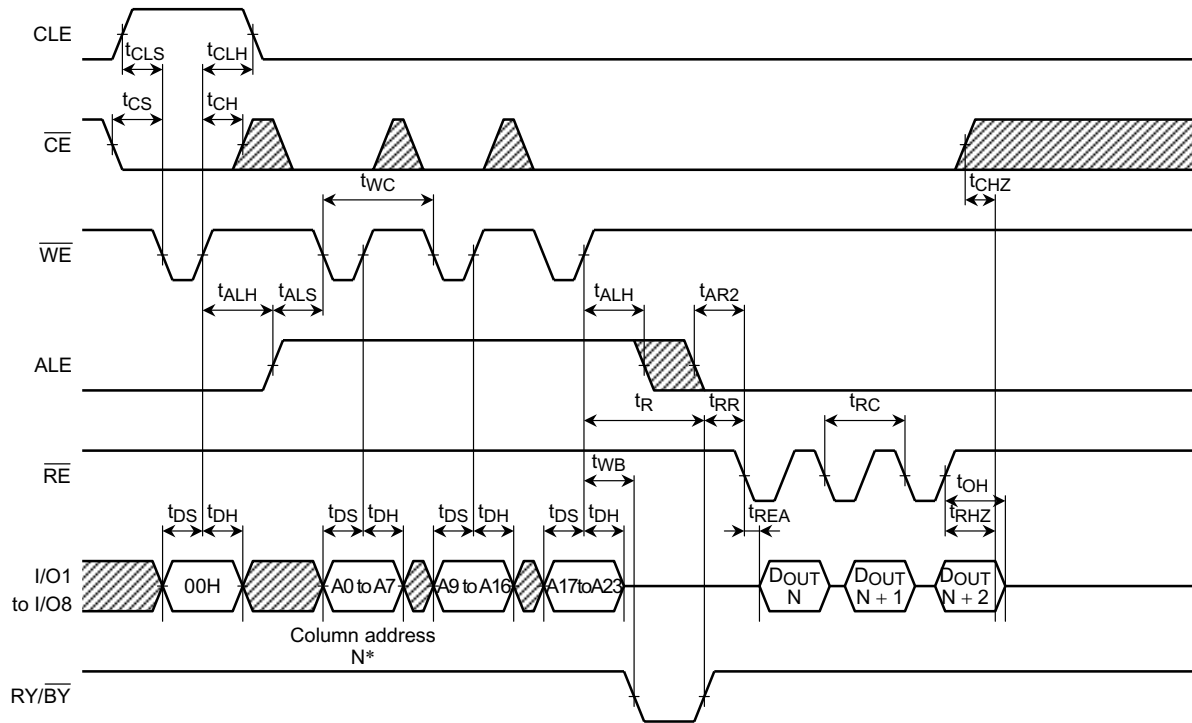* 70H represents the hexadecimal number

▨ : V_{IH} or V_{IL}

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Read Cycle (1) Timing Diagram

* Read Operation using 00H Command   N: 0 to 255

⬛ : V_IH or V_IL

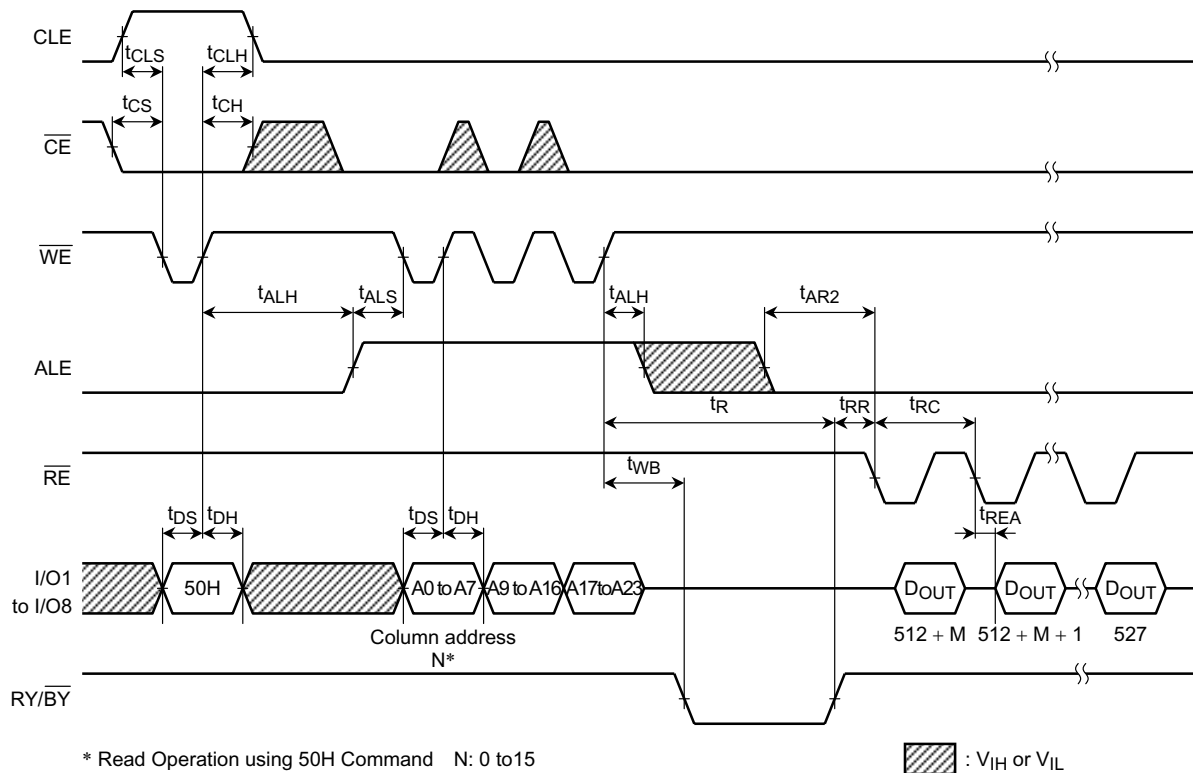## Read Cycle (1) Timing Diagram: When Interrupted by $\overline{CE}$

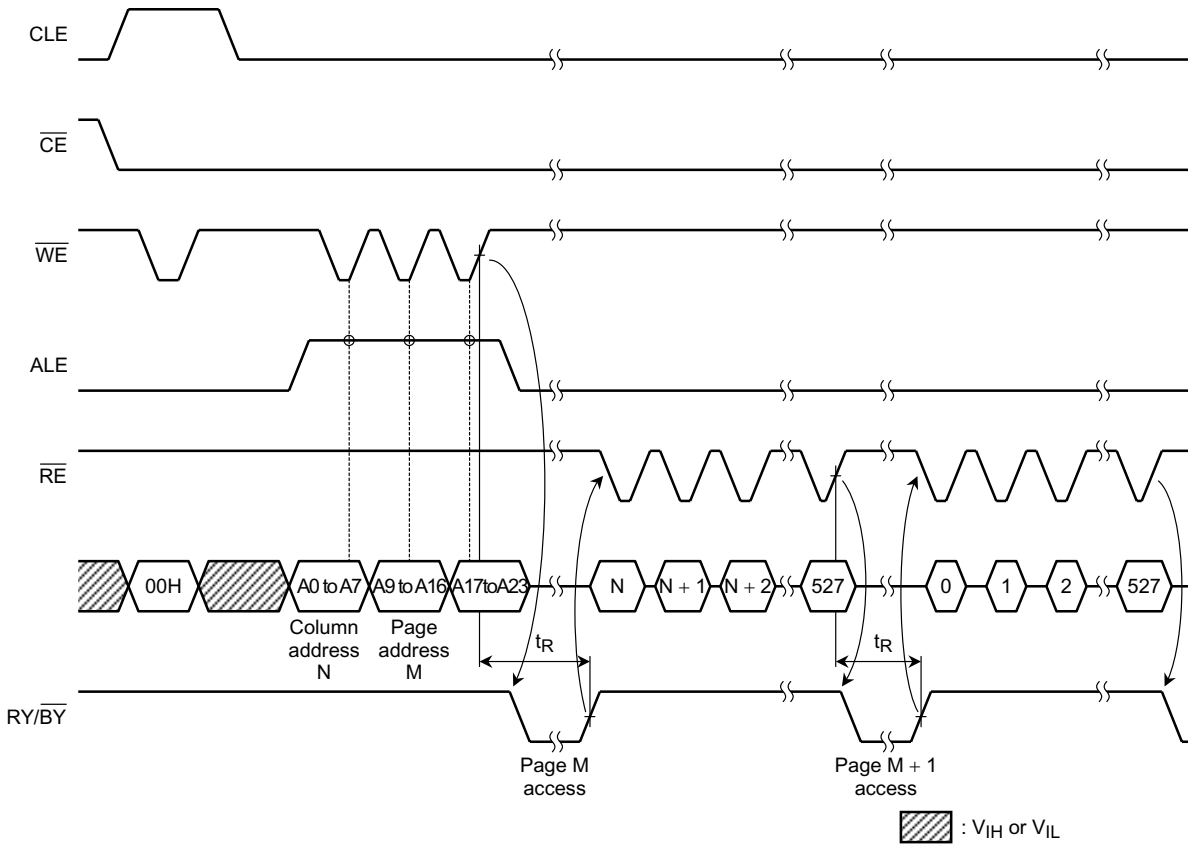* Read Operation using 00H Command   N: 0 to 255
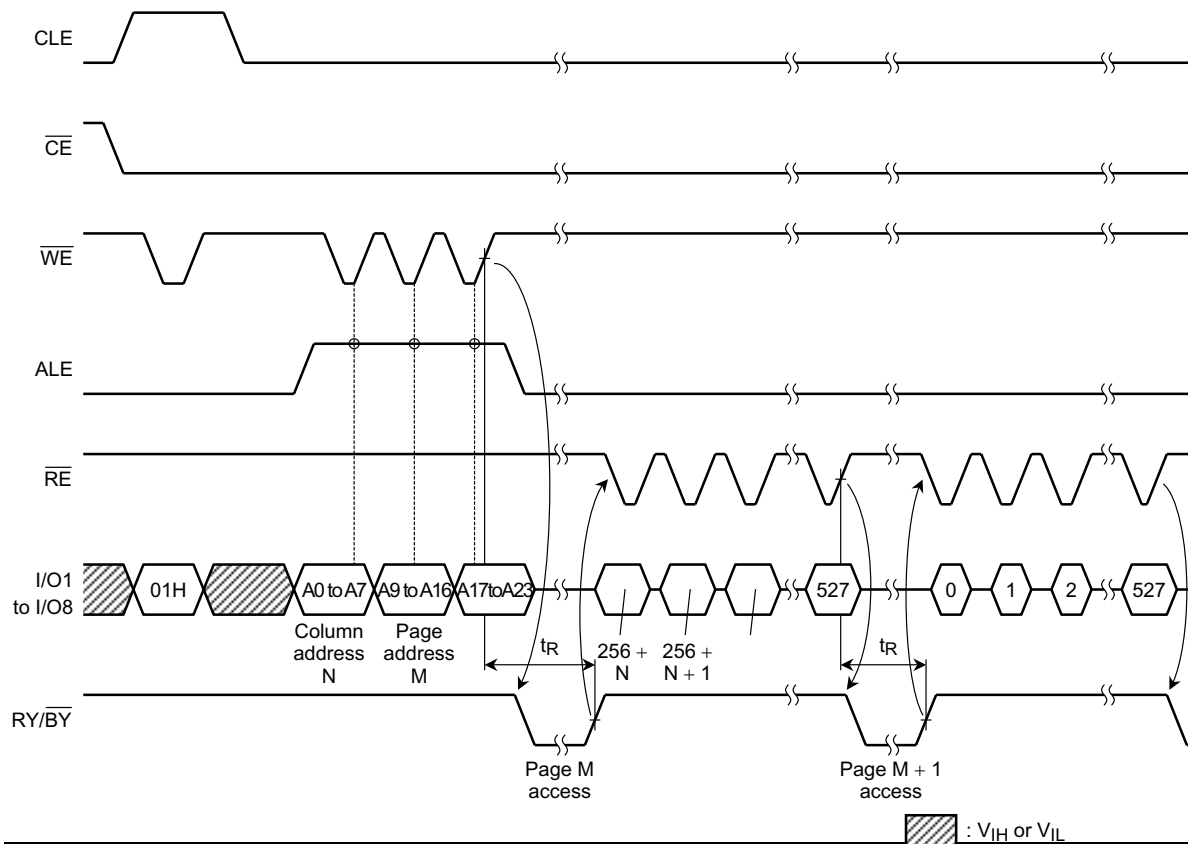
⬛ : V_IH or V_IL

Read Cycle (2) Timing Diagram

* Read Operation using 01H Command   N: 0 to 255

▨ : V_{IH} or V_{IL}
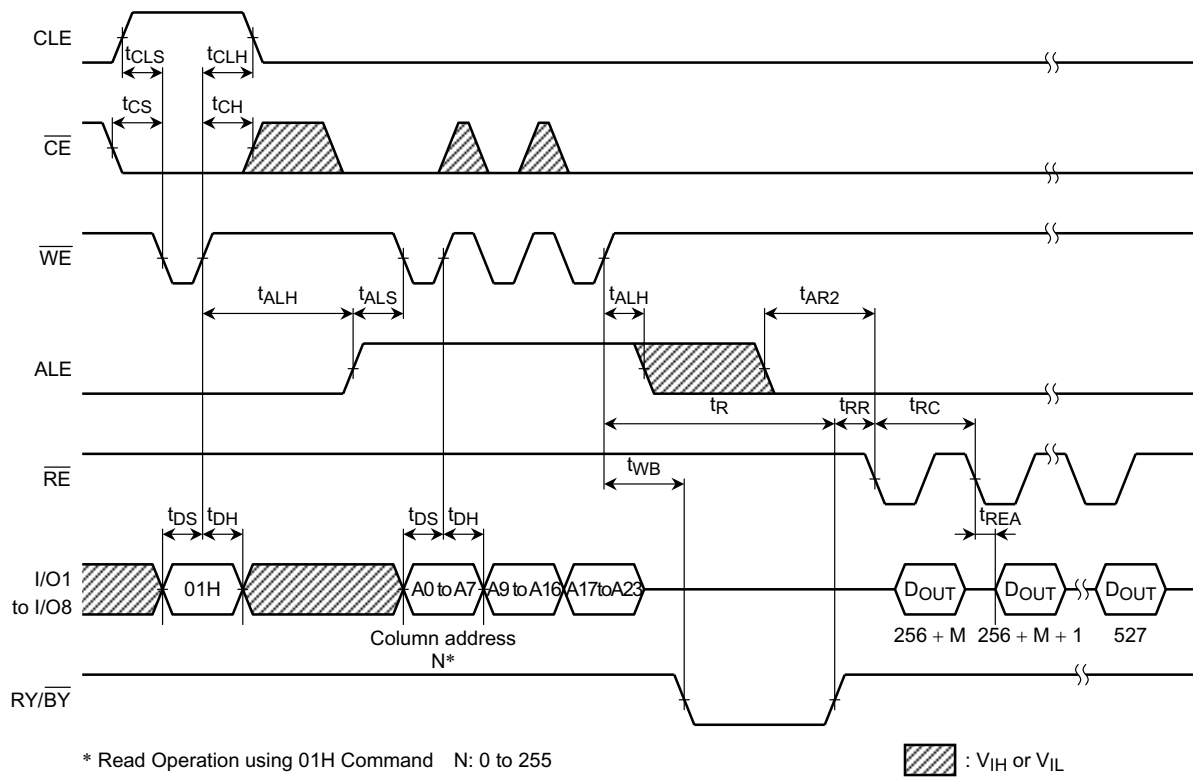
Read Cycle (3) Timing Diagram

* Read Operation using 50H Command   N: 0 to15

▨ : V_{IH} or V_{IL}

Sequential Read (1) Timing Diagram

Page M access

Page M + 1 access

▨ : V_{IH} or V_{IL}

Sequential Read (2) Timing Diagram

Page M access

Page M + 1 access
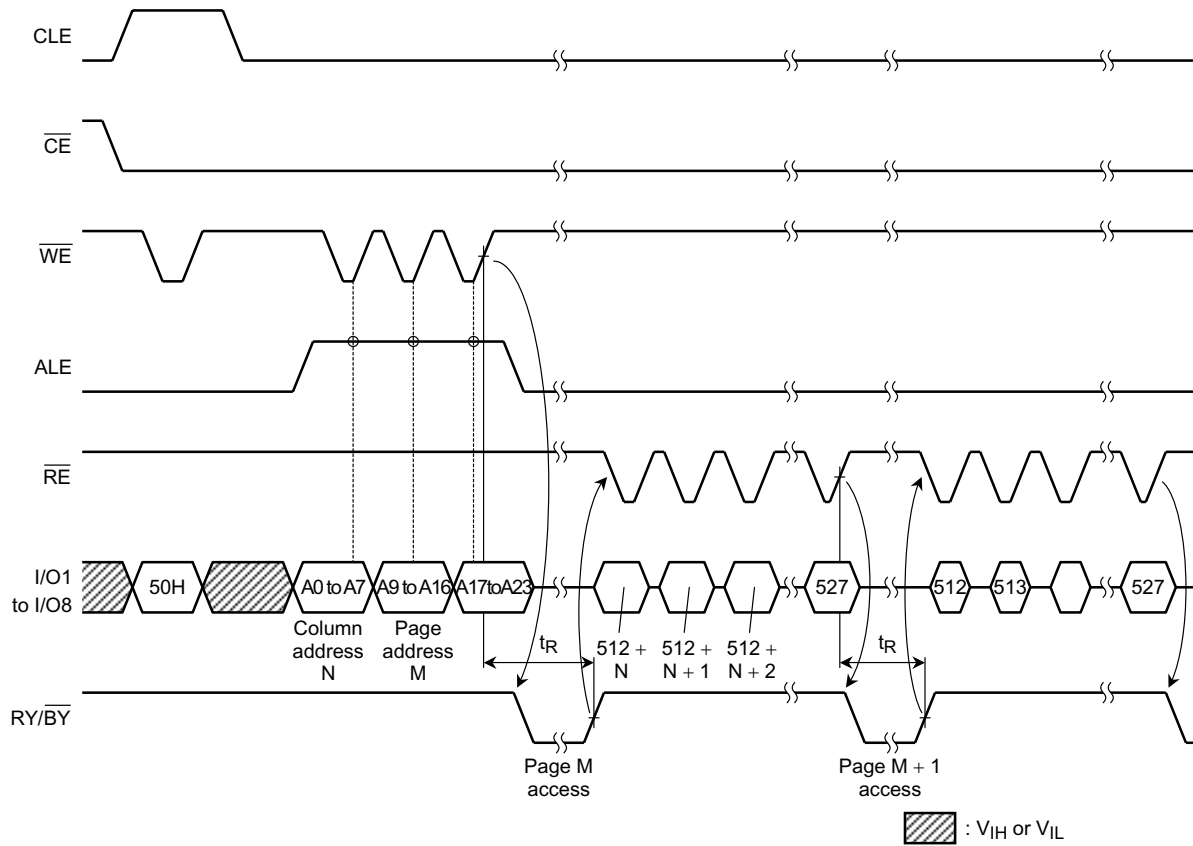
▨ : V_{IH} or V_{IL}

▨ : V_{IH} or V_{IL}

Auto-Program Operation Timing Diagram

$\boxed{///}$: V_{IH} or V_{IL} $\boxed{\#\#}$: Do not input data while data is being output.
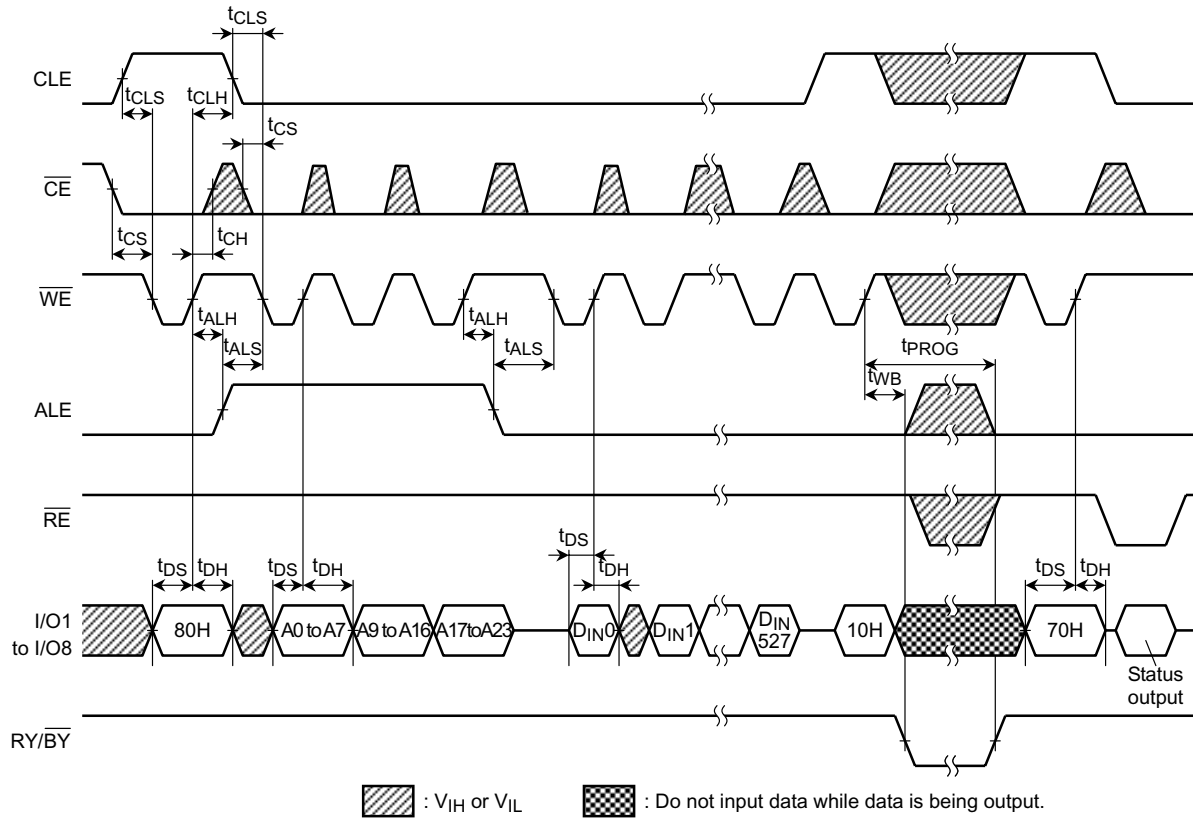
Auto Block Erase Timing Diagram

$\boxed{///}$: V_{IH} or V_{IL} $\boxed{\#\#}$: Do not input data while data is being output.

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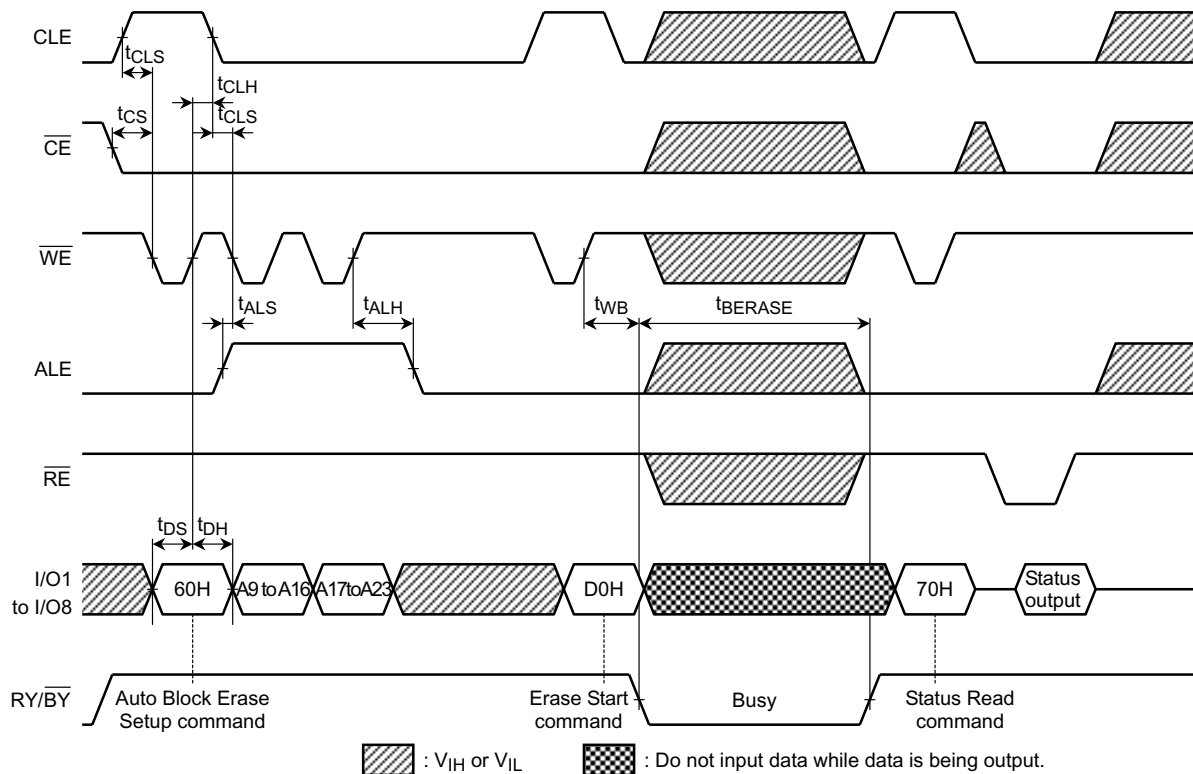
ID Read Operation Timing Diagram
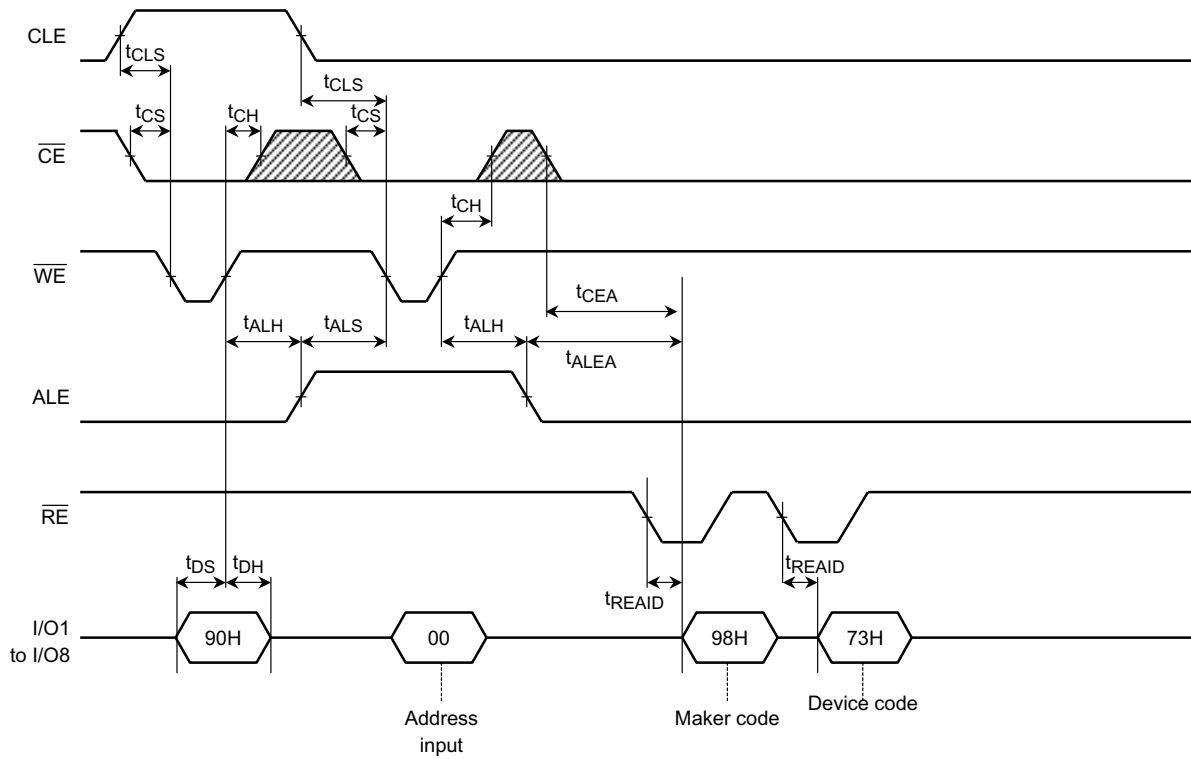
: V_{IH} or V_{IL}

PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register.

Address information is latched on the rising edge of $\overline{WE}$ if ALE is High.
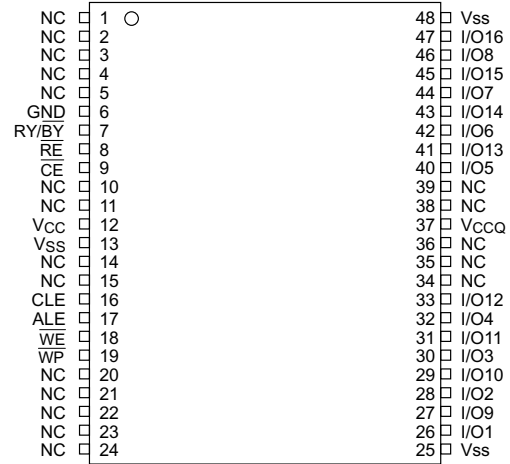
Input data is latched if ALE is Low.

Pin		Pin	
NC	1 ○	48	Vss
NC	2	47	I/O16
NC	3	46	I/O8
NC	4	45	I/O15
NC	5	44	I/O7
GND	6	43	I/O14
RY/$\overline{BY}$	7	42	I/O6
$\overline{RE}$	8	41	I/O13
$\overline{CE}$	9	40	I/O5
NC	10	39	NC
NC	11	38	NC
Vcc	12	37	VccQ
Vss	13	36	NC
NC	14	35	NC
NC	15	34	NC
CLE	16	33	I/O12
ALE	17	32	I/O4
$\overline{WE}$	18	31	I/O11
$\overline{WP}$	19	30	I/O3
NC	20	29	I/O10
NC	21	28	I/O2
NC	22	27	I/O9
NC	23	26	I/O1
NC	24	25	Vss

Figure 1 pinout

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during a Read operation. The $\overline{CE}$ signal is ignored when device is in Busy state (RY/$\overline{BY}$ = L), such as during a Program or Erase operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High. The $\overline{CE}$ signal must stay Low during the Read mode Busy state to ensure that memory array data is correctly transferred to the data register.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.

The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

I/O Port: I/O9 to 16

The I/O9 to 16 pins are used as a port for input/output data to and from the device. The I/O9 to 16 pins are low level(VIL) when address and command are asserted.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: RY/$\overline{BY}$

The RY/$\overline{BY}$ output signal is used to indicate the operating condition of the device. The RY/$\overline{BY}$ signal is in Busy state (RY/$\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state (RY/$\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.
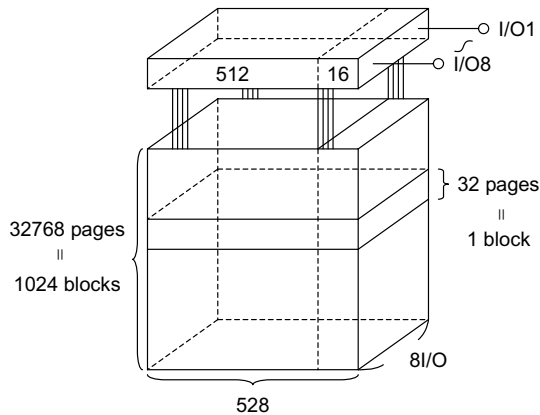

Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are used for main memory storage and 16 bytes are for redundancy or for other uses.

1 page = 528 bytes
1 block = 528 bytes × 32 pages = (16K + 512) bytes
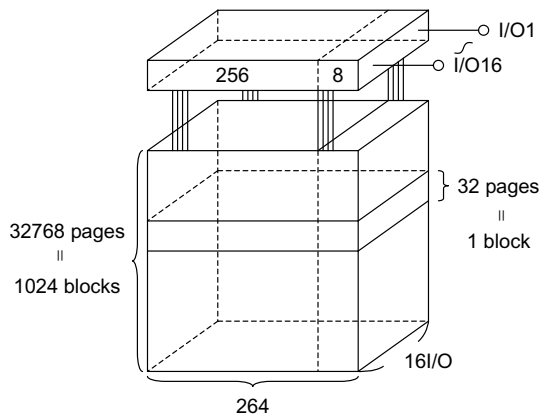Capacity = 528 bytes × 32 pages × 1024 blocks

Figure 2-2. x16 Schematic Cell Layout

A page consists of 264 words in which 256 words are used for main memory storage and 8 words are for redundancy or for other uses.

1 page = 264 words
1 block = 264 words × 32 pages = (8K + 256) words
Capacity = 264 words × 32 pages × 1024 blocks

An address is read in via the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	A16	A15	A14	A13	A12	A11	A10	A9
Third cycle	*L	A23	A22	A21	A20	A19	A18	A17

A0~A7: Column address
A9~A23: Page address
A14~A23: Block address
A9~A13: NAND address in block

*: A8 is automatically set to Low or High by a 00H command or a 01H command.
I/O9-16 should be low when address is input.

* I/O8 must be set to Low in the third cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the ten different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic table

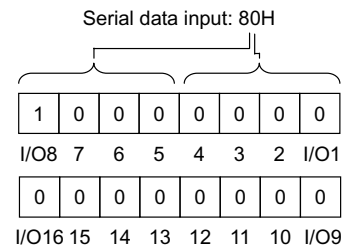|	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L	⌐_⌐	H	*
Address Input	L	H	L	⌐_⌐	H	*
Data Input	L	L	L	⌐_⌐	H	H
Serial Data Output	L	L	L	H	⌐_⌐	*
During Read (Busy)	*	*	L	H	H	*
	*	*	H	*	*	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/Vcc

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read Mode (1)	00	—	
Read Mode (2)	01	—	
Read Mode (3)	50	—	
Reset	FF	—	○
Auto Program	10	—	
Auto Block Erase	60	D0	
Status Read	70	—	○
ID Read	90	—	

HEX data bit assignment (Example)

Serial data input: 80H

1	0	0	0	0	0	0	0
I/O8	7	6	5	4	3	2	I/O1

0	0	0	0	0	0	0	0
I/O16	15	14	13	12	11	10	I/O9

01 command isn't implemented by x16.

Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1~I/O16	Power
Output Select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a 00H command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.
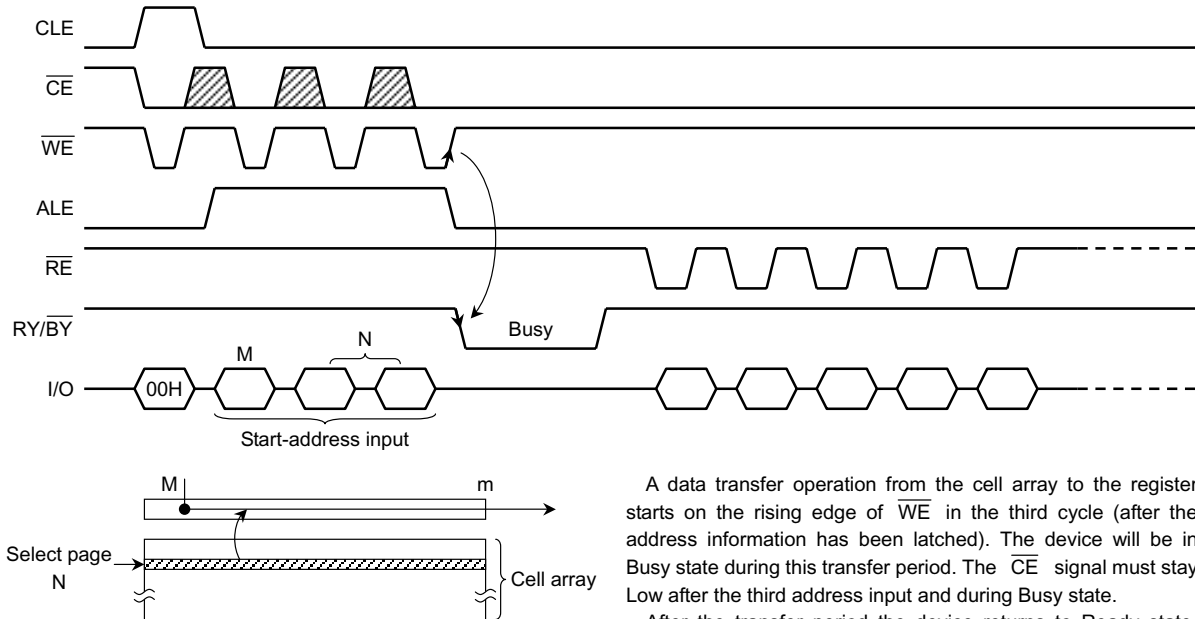

Figure 3. Read mode (1) operation

X8 : m=527
X16 : m=263

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the third cycle (after the address information has been latched). The device will be in Busy state during this transfer period. The $\overline{CE}$ signal must stay Low after the third address input and during Busy state.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start pointer designated in the address input cycle.

Read Mode (2)　x8 only
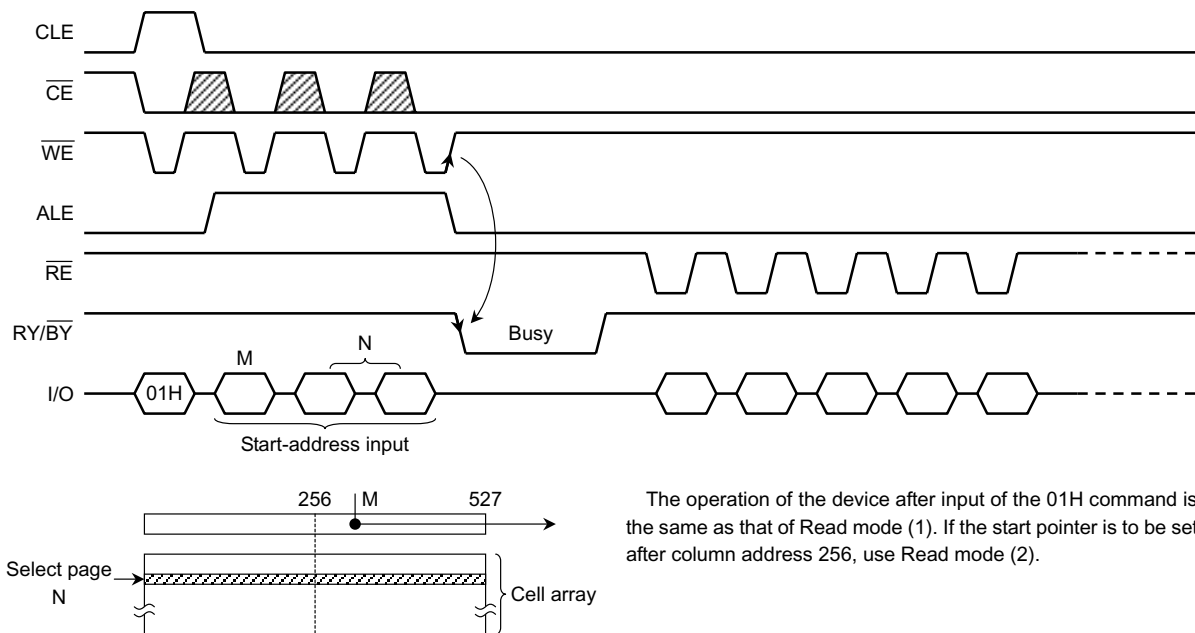
Figure 4. Read mode (2) operation

The operation of the device after input of the 01H command is the same as that of Read mode (1). If the start pointer is to be set after column address 256, use Read mode (2).

Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.
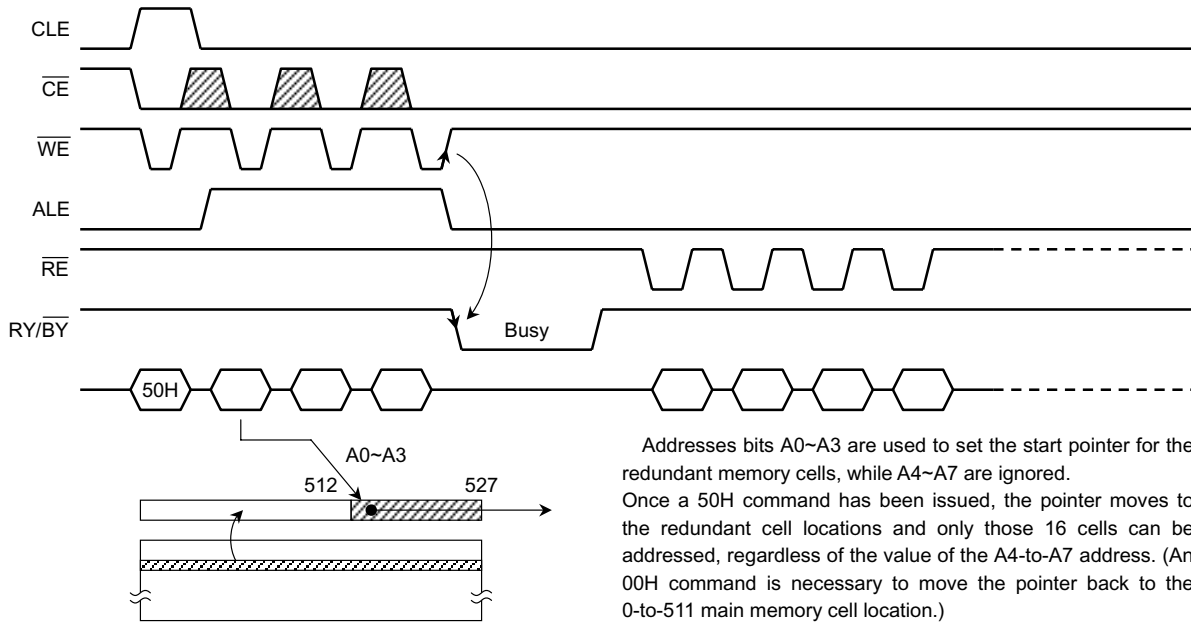

Addresses bits A0~A3 are used to set the start pointer for the redundant memory cells, while A4~A7 are ignored.

Once a 50H command has been issued, the pointer moves to the redundant cell locations and only those 16 cells can be addressed, regardless of the value of the A4-to-A7 address. (An 00H command is necessary to move the pointer back to the 0-to-511 main memory cell location.)

Figure 5. Read mode (3) operation

X8：m=527 , n=512
X16：m=263 , n=256

Sequential Read(1)(2)(3)

This mode allows the sequential reading of pages without additional address input.

Sequential Read (1)

Sequential Read (2)
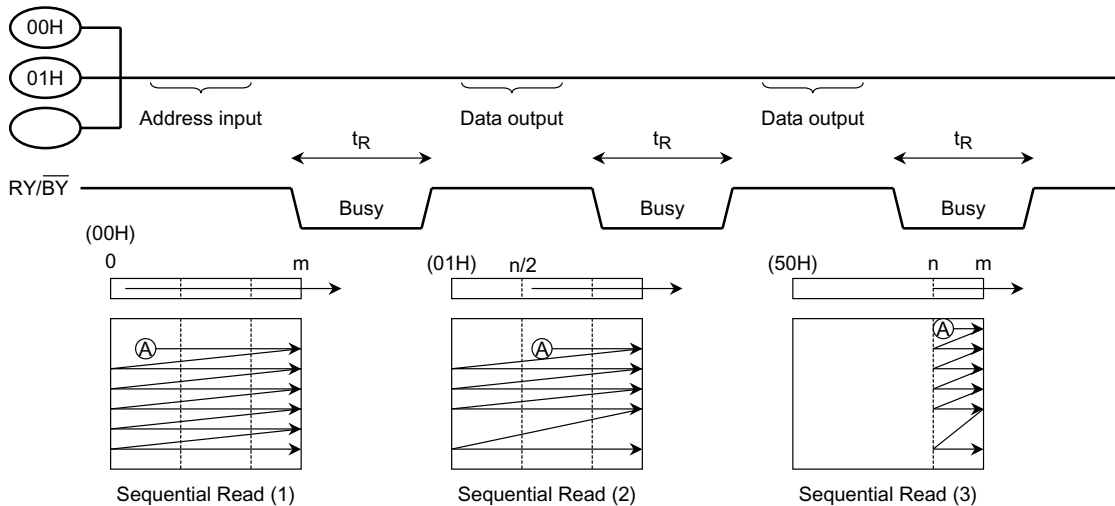
Sequential Read (3)

Sequential Read modes (1) and (2) output the contents of addresses 0~m as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only. When the pointer reaches the last address, the device continues to output the data from this address ** on each $\overline{RE}$ clock signal.

X8： m=527,n=512
X16：m=263,n=256

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the $\overline{RE}$ clock after a 70H command input. The resulting information is outlined in Table 5.

Table 5. Status output table

	STATUS	OUTPUT	
I/O1	Pass/Fail	Pass: 0	Fail: 1
I/O2	Not Used	0	
I/O3	Not Used	0	
I/O4	Not Used	0	
I/O5	Not Used	0	
I/O6	Not Used	0	
I/O7	Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protected: 1
I/O9 to I/O16	Not Used	0	

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.
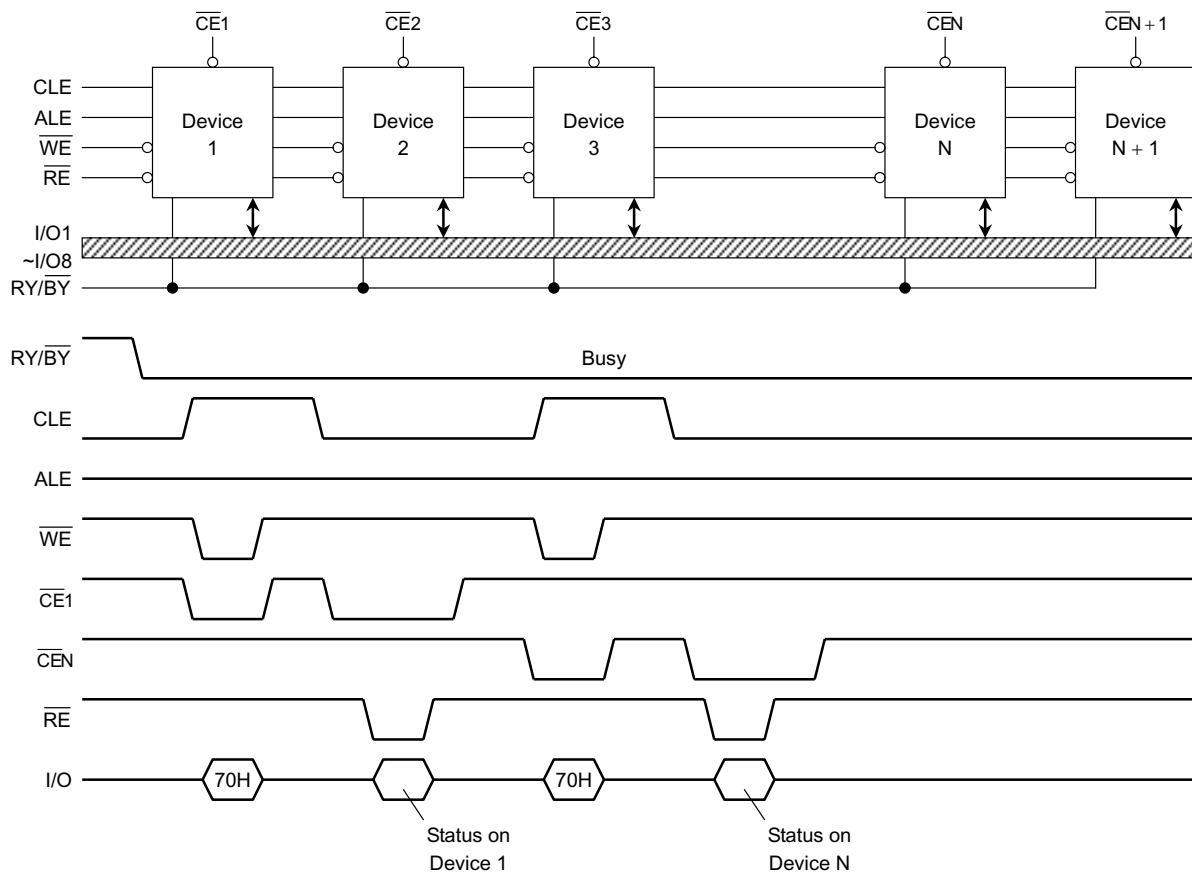
Figure 6. Status Read timing application example

System Design Note: If the RY/$\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device carries out an Automatic Page Program operation when it receives a "10H" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)


The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following input of the "10H" command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Figure 7. Auto Page Program operation

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command "D0H" which follows the Erase Setup command "60H". This two-cycle process for Erase operations acts as an ertra layer of protection from aceidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.
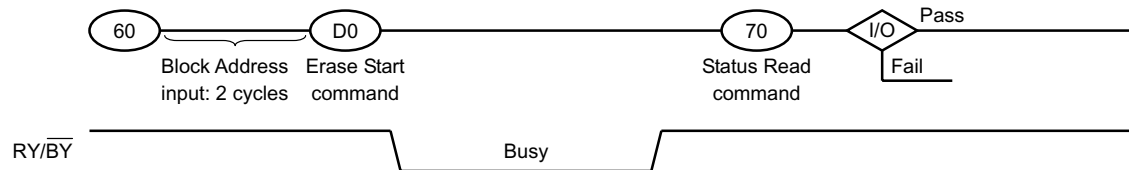
Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.

The response to an "FFH" Reset command input during the various device operations is as follows:

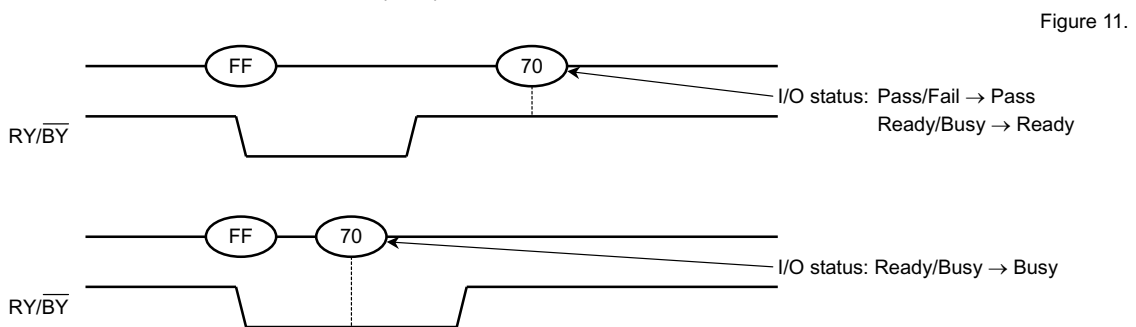<u>When a Reset (FFH) command is input during programming</u>

Figure 8.
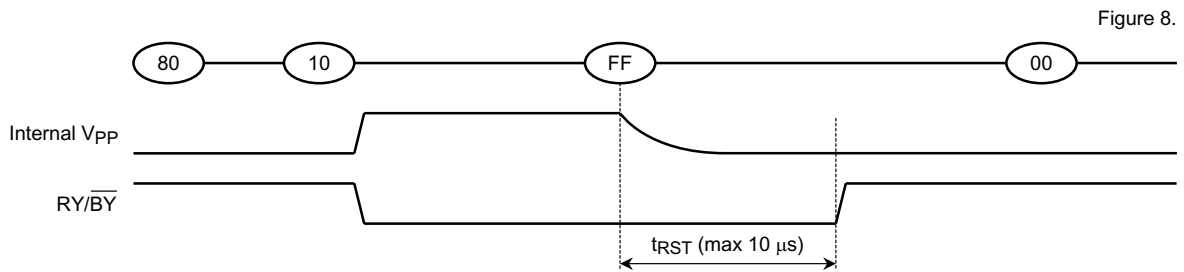
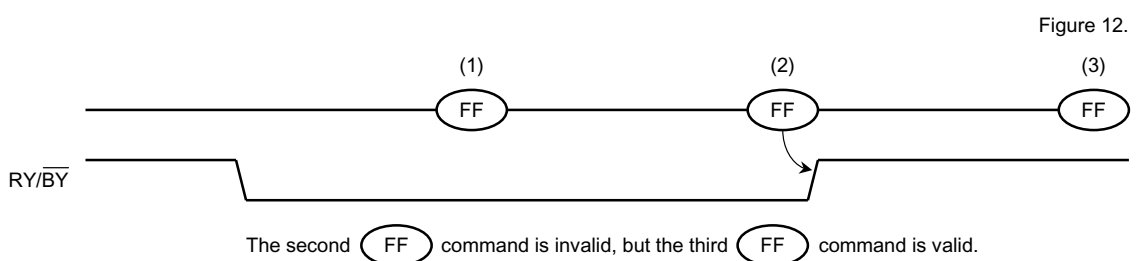<u>When a Reset (FFH) command is input during erasing</u>

Figure 9.
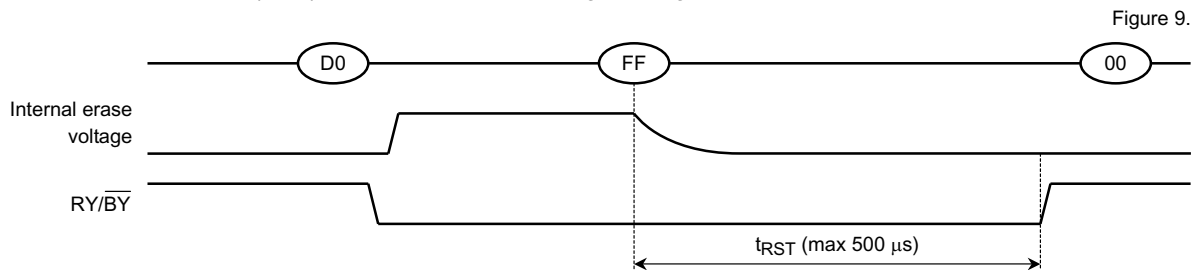
<u>When a Reset (FFH) command is input during Read operation</u>

Figure 10.
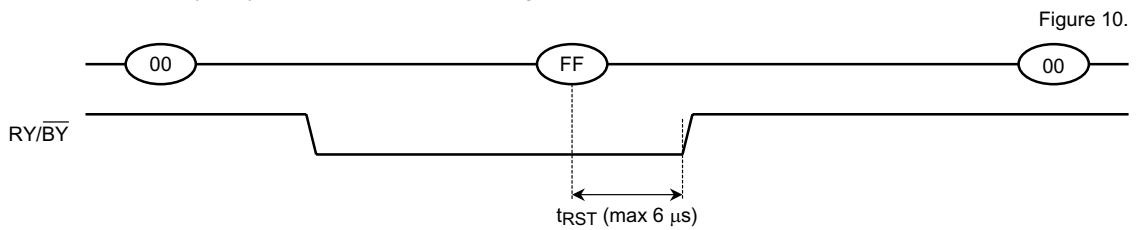
<u>When a Status Read command (70H) is input after a Reset</u>

Figure 11.

I/O status: Pass/Fail → Pass
Ready/Busy → Ready

I/O status: Ready/Busy → Busy

<u>When two or more Reset commands are input in succession</u>

Figure 12.

The second FF command is invalid, but the third FF command is valid.

TOSHIBA

ID Read

The device contains ID codes which identify the device type and the manufacturer.

The ID codes can be read out under the following timing conditions:

For the specifications of the access times t_{REAID}, t_{CR} and t_{AR1} refer to the AC Characteristics.
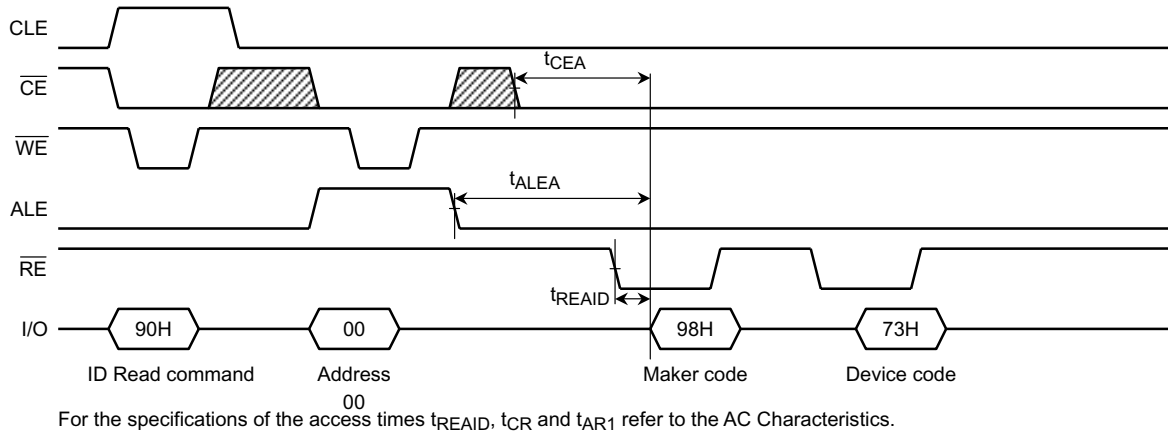
Figure 13. ID Read timing

Table 6. ID Codes read out by ID read command 90H

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker code	1	0	0	1	1	0	0	0	98H
Device code	0	1	1	1	0	0	1	1	73H

I/O9 to I/O16 are "0".

TOSHIBA

APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary.

The $\overline{WP}$ signal may be negated any time after the V_{CC} reaches 2.5 V and $\overline{CE}$ signal is kept high in power up sequence.
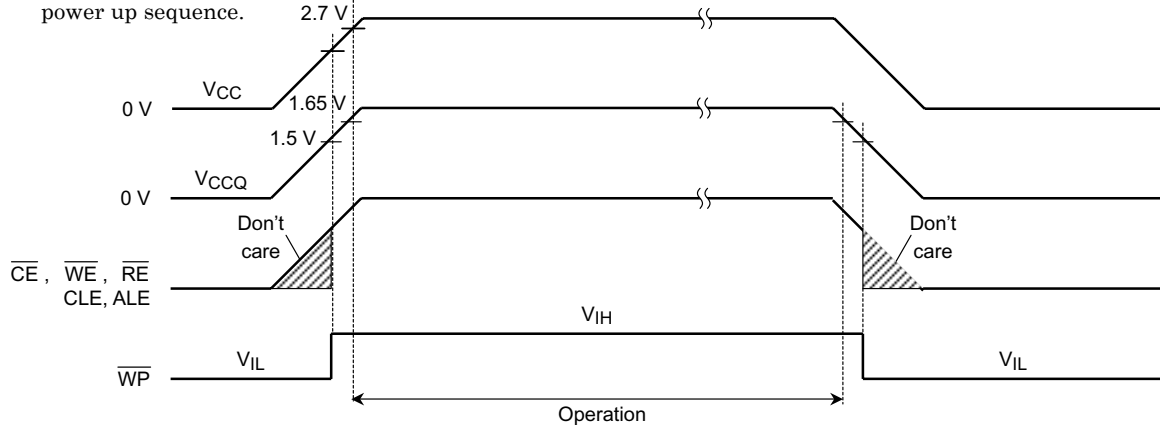
Figure 15. Power-on/off Sequence

In order to operate this device stably, after V_{CC} becomes 2.5 V and V_{CCQ} becomes 1.5V, it recommends starting access after about 200 μs.

(2) Status after power-on

The following sequence is necessary because some input signals may not be stable at power-on.
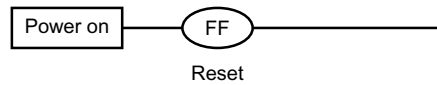
Figure 16.

(3) Prohibition of unspecified commands

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of command while Busy state

During Busy state, do not input any command except 70H and FFH.

(5) Acceptable commands after Serial Input command "80H"

Once the Serial Input command "80H" has been input, do not input any command other than the Program Execution command "10H" or the Reset command "FFH".

If a command other than "10H" or "FFH" is input, the Program operation is not performed.

2003-01-24   25/34
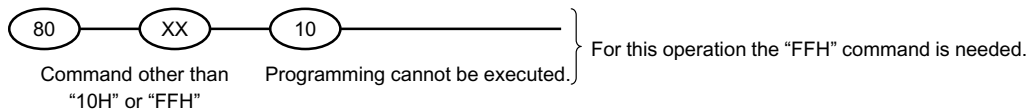
(6)   Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.
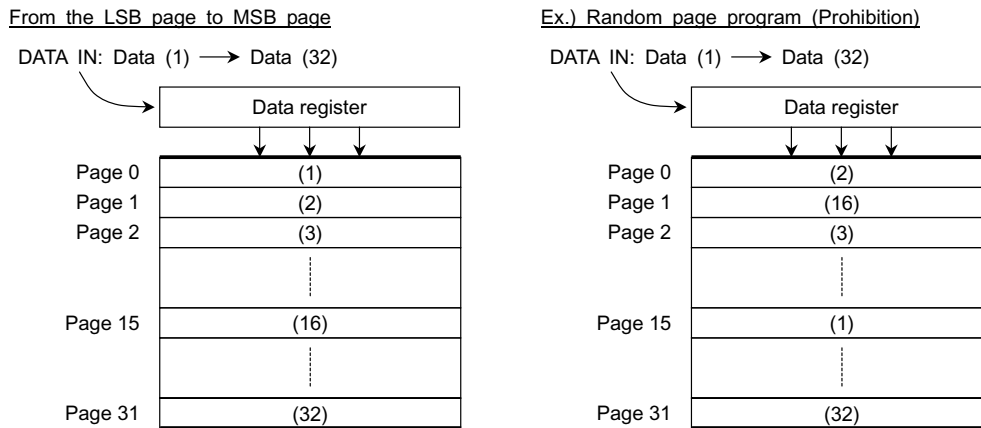
From the LSB page to MSB page

DATA IN: Data (1) ⟶ Data (32)

Data register		

Page 0	(1)
Page 1	(2)
Page 2	(3)
	⋮
Page 15	(16)
	⋮
Page 31	(32)

Ex.) Random page program (Prohibition)

DATA IN: Data (1) ⟶ Data (32)

Data register		

Page 0	(2)
Page 1	(16)
Page 2	(3)
	⋮
Page 15	(1)
	⋮
Page 31	(32)

Figure 17. page programming within a block

(7)   Status Read during a Read operation
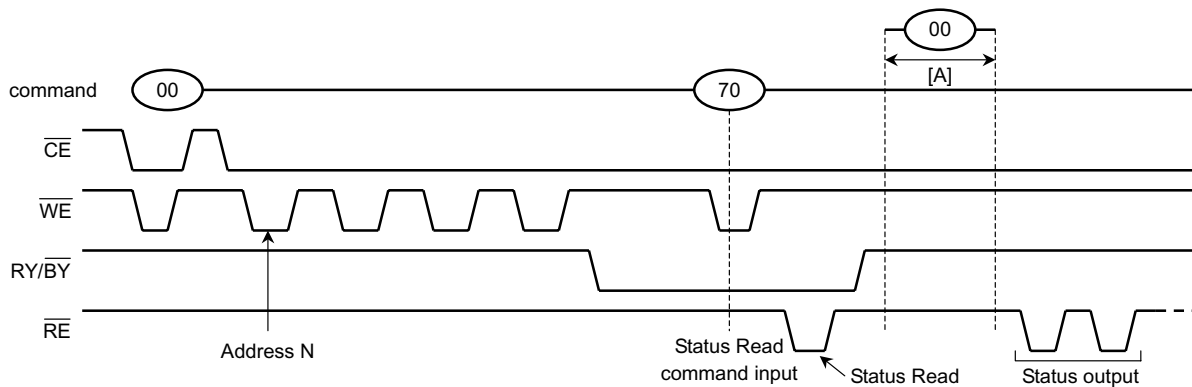
Figure 18.

The device status can be read out by inputting the Status Read command "70H" in Read mode.

Once the device has been set to Status Read mode by a "70H" command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command "00H" is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

(8)   Pointer control for "00H", "01H" and "50H"

The device has three Read modes which set the destination of the pointer. Table 8 shows the destination of the pointer, and Figure 19 is a block diagram of their operations.

Table 8. Pointer Destination

Read Mode	Command	Pointer	
		(x8)	(x16)
(1)	00H	0~255	0~255
(2)	01H	256~511	―――
(3)	50H	512~527	256~263
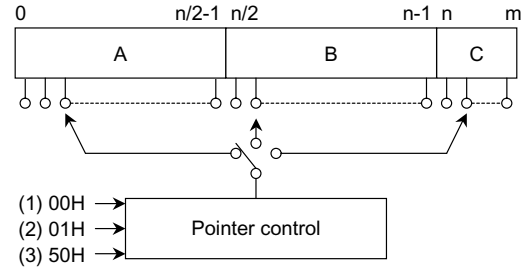
Figure 19 Pointer control

The pointer is set to region A by the "00H" command, to region B by the "01H" command, and to region C by the "50H" command.

(Example)

The "00H" command must be input to set the pointer back to region A when the pointer is pointing to region C.
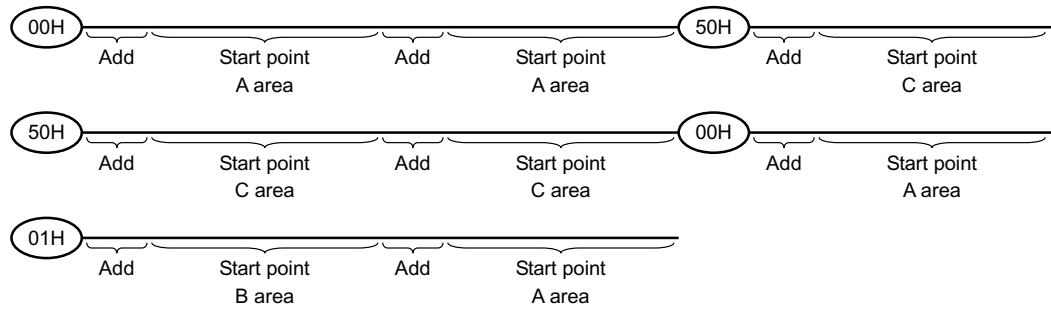
To program region C only, set the start point to region C using the 50H command.
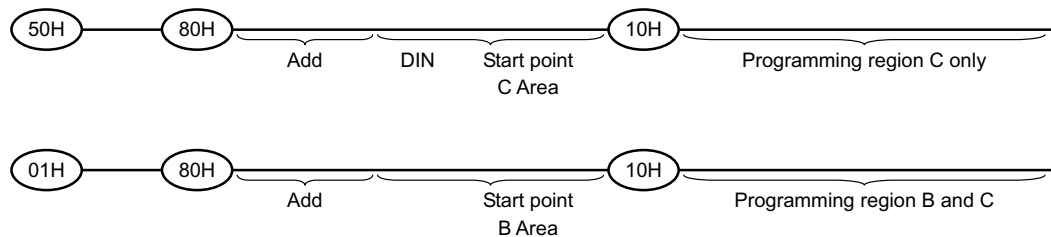
Figure 20. Example of How to Set the Pointer

(9) RY/$\overline{BY}$: termination for the Ready/Busy pin (RY/$\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY/$\overline{BY}$ buffer consists of an open drain circuit.
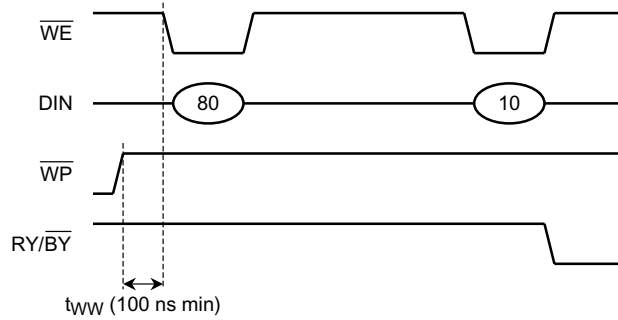

Figure 21.
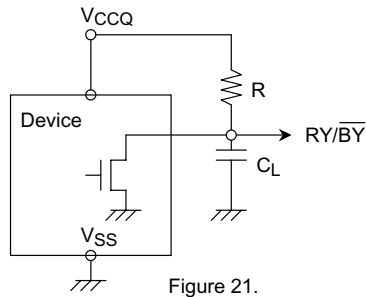
This data may vary from device to device.
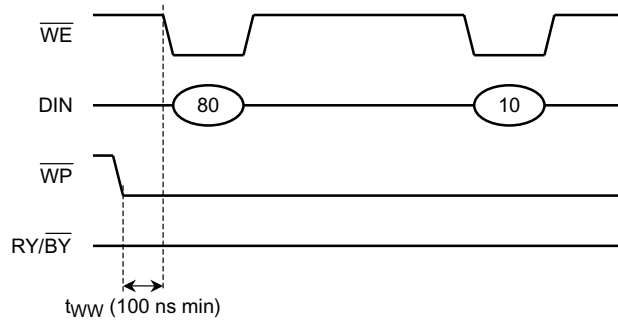We recommend that you use this data as a reference when selecting a resistor value.

TOSHIBA
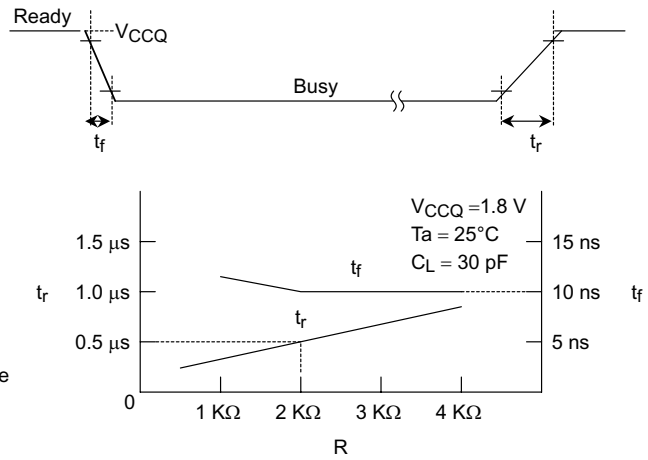
(10) Note regarding the $\overline{\text{WP}}$ signal

The Erase and Program operations are automatically reset when $\overline{\text{WP}}$ goes Low. The operations are enabled and disabled as follows:
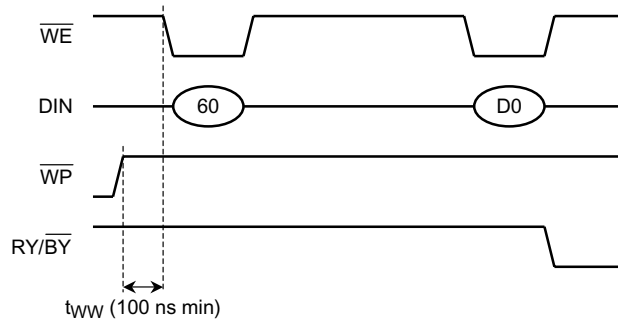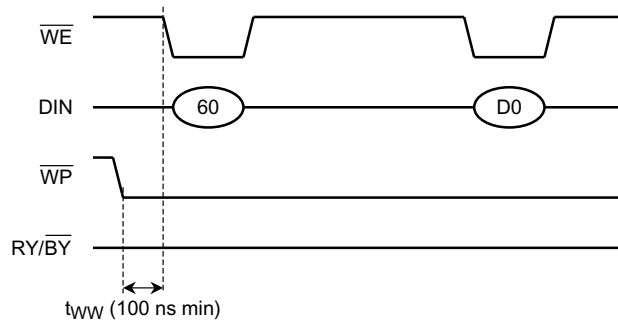
Enable Programming

t_{WW} (100 ns min)

Disable Programming

t_{WW} (100 ns min)

Enable Erasing
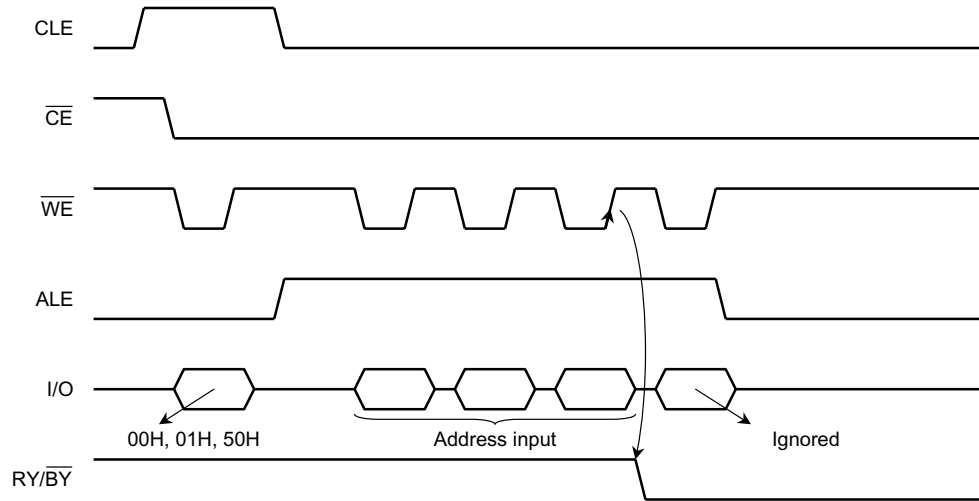

t_{WW} (100 ns min)

Disable Erasing

t_{WW} (100 ns min)

(11)   When four address cycles are input

Although the device may read in a fourth address, it is ignored inside the chip.

Read operation

Internal read operation starts when $\overline{WE}$ goes High in the third cycle.

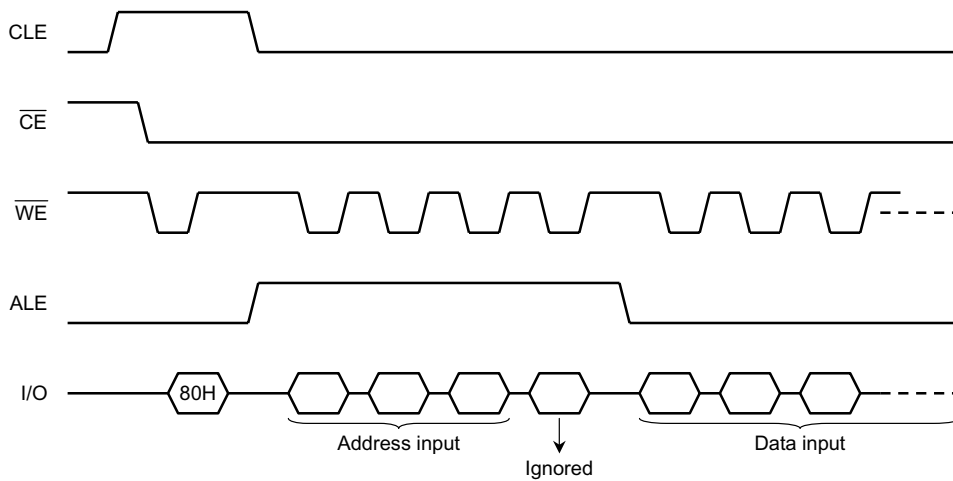Figure 22.

Program operation

Figure 23.

(12)   Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 3 segments. Each segment can be programmed individually as follows:

1st programming | Data Pattern 1 | All 1s

2nd programming | All 1s | Data Pattern 2 | All 1s

3rd programming | All 1s | Data Pattern 3

Result | Data Pattern 1 | Data Pattern 2 | ---- | Data Pattern 3
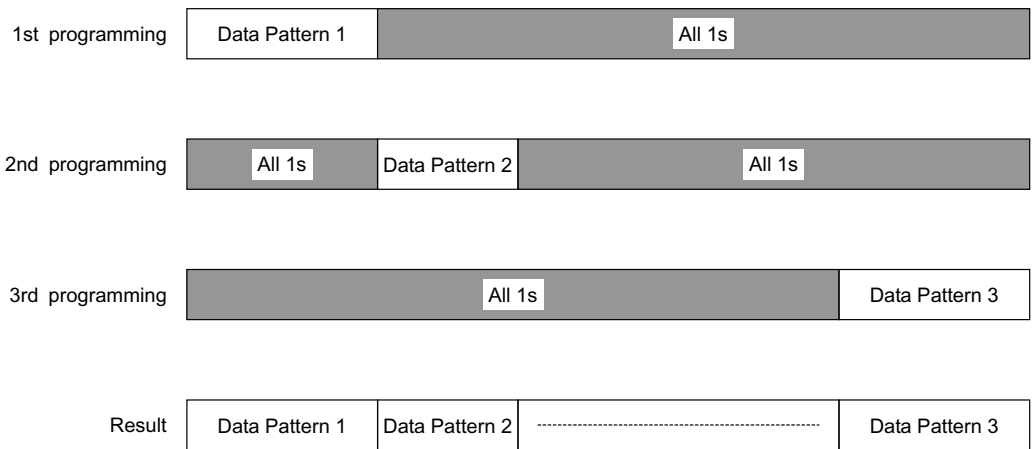
Figure 24.

Note: The input data for unprogrammed or previously programmed page segments must be "1"

(13)   Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, at the time of use, please check whether a block is bad and do not use these bad blocks.
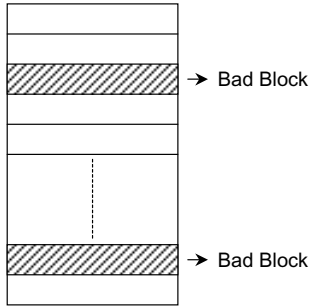

→ Bad Block

→ Bad Block

Figure 26.

At the time of shipment, all data bytes in a Valid Block are FFh(x8) or FFFFh(x16). For Bad Block, all bytes are not in the FFh state(x8) or FFFFh state(x16). Please don't perform erase operation to Bad Block.
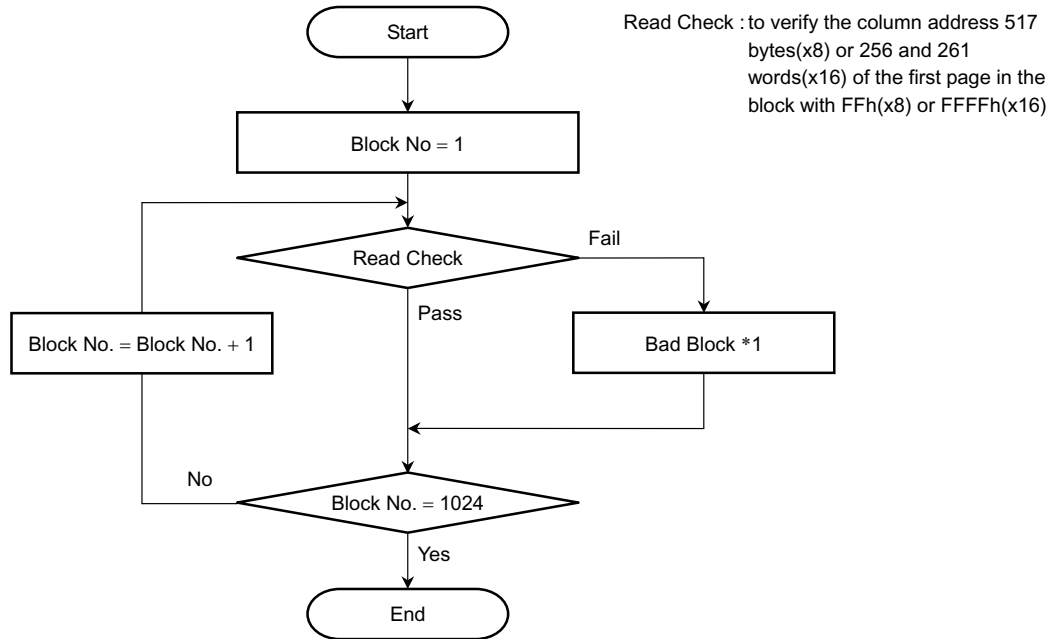
Check if the device has any bad blocks after installation into the system. Figure 27 shows the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the Bit line by the Select gate

The number of valid blocks at the time of shipment is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	1004	—	1024	Block

Bad Block Test Flow

Read Check : to verify the column address 517 bytes(x8) or 256 and 261 words(x16) of the first page in the block with FFh(x8) or FFFFh(x16)

*1: No erase operation is allowed to detected bad blocks

Figure 27

(14)   Failure phenomena for Program and Erase operations

   The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

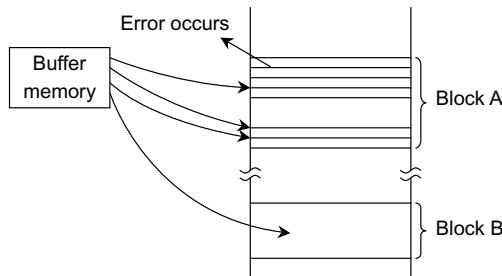| FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure 1 → 0	(1) Block Verify after Program → Retry
		(2) ECC

- ECC: Error Correction Code

- Block Replacement

   Program

   When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using an another appropriate scheme).

Figure 28.

   Erase
       When an error occurs in an Erase operation, prevent future accesses to this bad block
       (again by creating a table within the system or by using another appropriate scheme).

(15)   Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shoetage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.
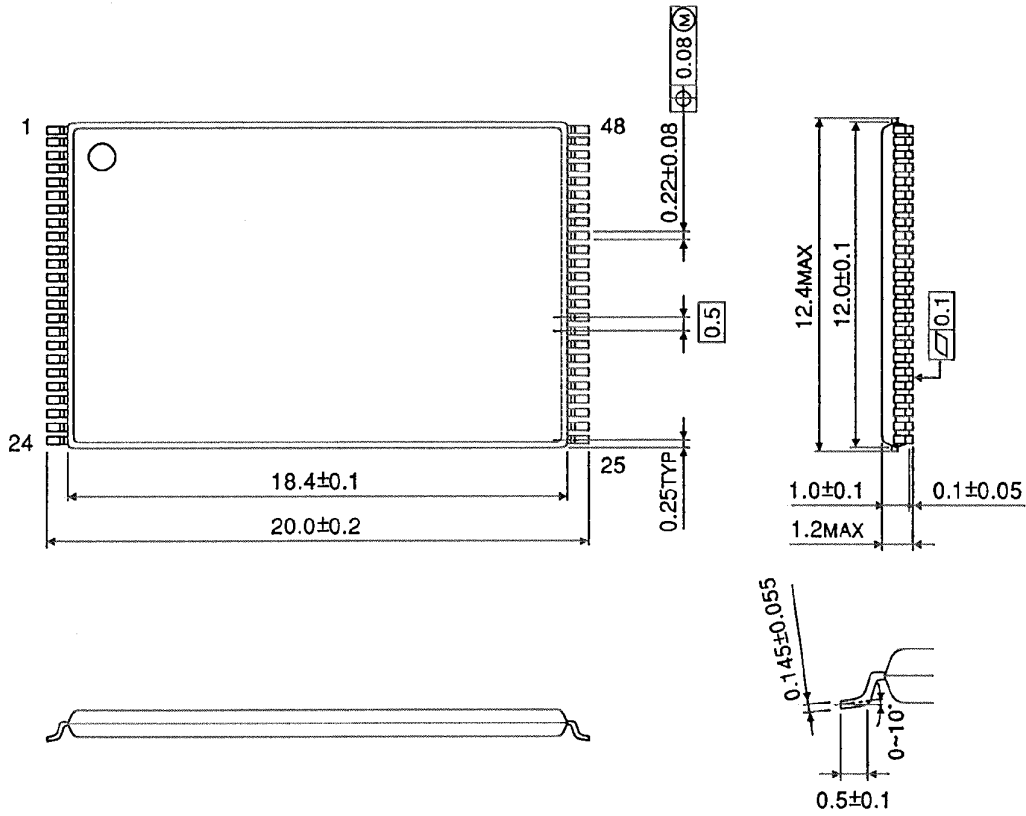
Package Dimensions

Unit : mm

TSOPI48-P-1220-0.50

Unit: mm

Weight: 0.53g (typ.)