FAIRCHILD SEMICONDUCTOR™

July 1998

NM95MS16
Plug and Play Front-End Devices for ISA-BUS Systems

General Description

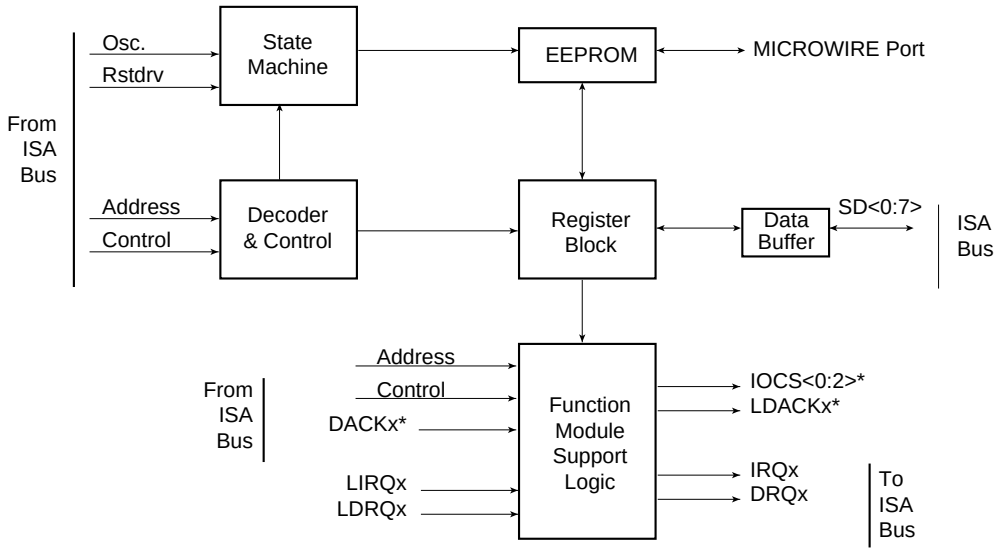
The NM95MS16 is the smaller of a family of devices designed to provide complete Plug and Play Capability for ISA bus systems. The NM95MS16 includes the necessary state machine logic to manage the Plug and Play protocol in addition to switches for steering Interrupt and DMA requests. It also features a built-in 2 kbits of serial EEPROM for storing the resource data specified in the Plug and Play Standard. In addition, 4 kbits of EEPROM is available for use by other on-board logic. This device provides a Òtruly completeÓ single-chip solution for implementing Plug and Play on ISA-Bus Adapter cards. The NM95MS16 supports one logical device with a flexible choice of DMA/IRQ selection and I/O Chipselect generation as well as offering 16-bit addressing in Mode 1.

NM95MS16 is implemented using FairchildÕs Advanced CMOS process and operates single power supply. The NM95MS16 is available in a 48-pin TQFP package and 52-pin PLCC package.

Features

- Complete Implementation of Plug and Play Standard
  - Ñ Direct interface to ISA bus
- Two modes of operation
  - Ñ DMA mode
  - Ñ Extended Interrupt mode (Windows ¨ 95 logo compatible)
- 6 or 8 ISA bus interrupt lines and 2 DRQ/DACK lines supported
- On-chip EEPROM for resource request table
- Additional 4 kbits of on-chip EEPROM available for external access
- 24 mA Drivers for Data outputs
- Complete compliance to ISA PnP specification (Ver. 1.0A)
- 48-Pin TQFP, and 52-Pin PLCC Packages

Block Diagram



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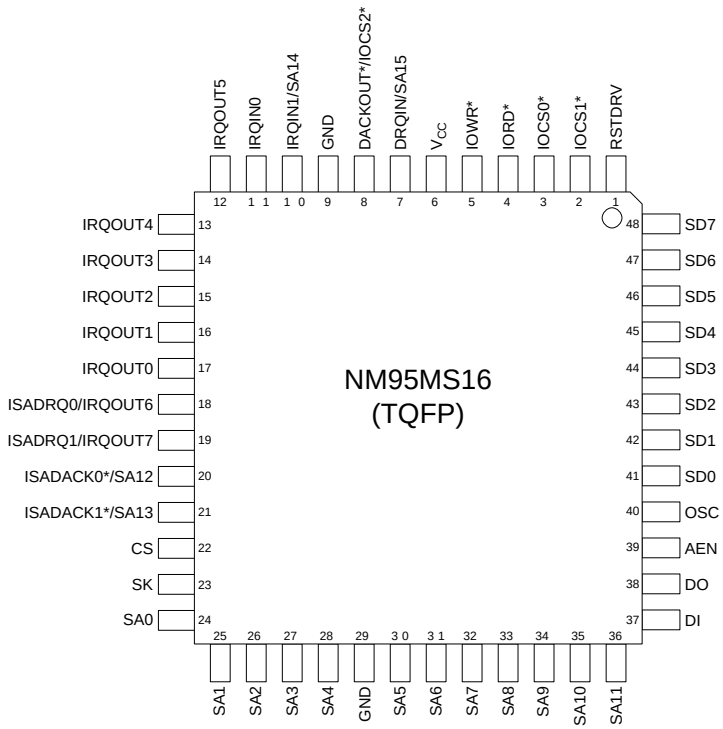
Windows¨ 95 is a registered trademark of Microsoft Corporation.

Connection Diagrams

Commercial Temperature Range (0 °C to +70 °C)



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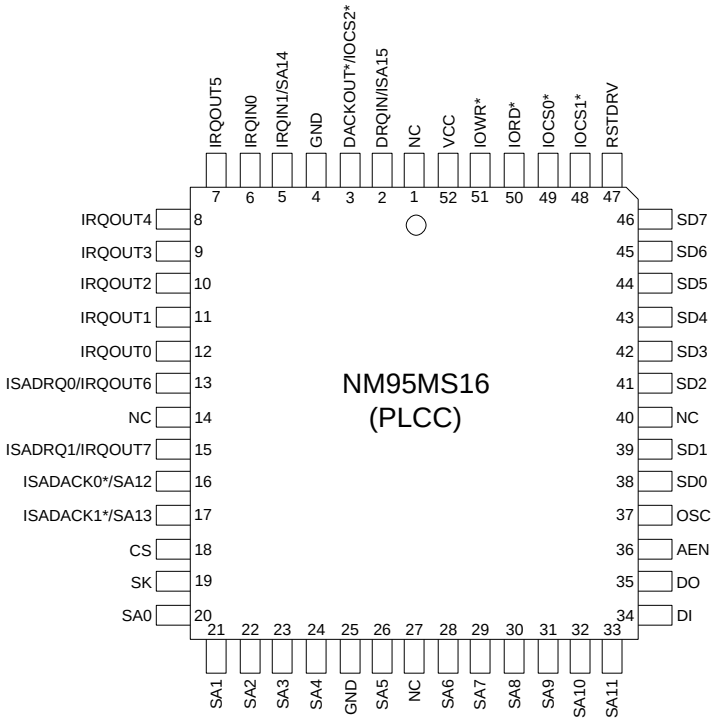
Order Number NM95MS16VBH



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Order Number NM95MS16V

Connection Diagrams (Continued)

Signals	Type	Description
SA<11:0>	I	Address inputs from the ISA bus.
IORD*	I	I/O read strobe from the ISA bus.
IOWR*	I	I/O write strobe from the ISA bus.
AEN	I	Address Enable from ISA Bus Ñused in conjunction with DMA.
SD<7:0>	I/O	Data bus Ñlower byte Ñfrom/to the ISA bus.
OSC (Note 1)	I	ÒOSCÓ clock from the ISA bus Ñused for internal state machines.
RSTDRV	I	Reset input from the ISA bus.
CS	I	Chip select for Microwire port. There should be a pull down resistor of 4.7k on CS pin if unused externally, or directly connected to GND.
SK, DI	I	Clock and Data input lines for Microwire bus connection to access a portion (4k) on chip EEPROM.
DO	O	Data output line for the Microwire interface detailed above.
IRQOUT<5:0>	O	Connection to ISA bus interrupt request pins. On-chip interrupt request(s) may be connected to any 6 of the ISA IRQ lines.
IRQIN<1:0>	I	Interrupt request from on-board logic
DRQin/SA<15>	I	DMA request from on-board logic, or Address input from ISA bus depending on mode selected.
DACKOUT* /IOCS2*	O	DMA Acknowledge for on-board logic or Programmable chipselect (2) depending on mode selected.
ISADRQ<1:0>/IRQOUT<7:6>	O	Connection for two ISA bus DMA Request lines, or additional interrupt request lines depending on the mode selected.
ISADACK<1:0>*/SA<13:12>	I	DMA Acknowledge from the ISA bus or additional address lines depending on the mode selected.
IOCS<1:0>*	O	Programmable chip selects to address on-board peripheral.
IRQIN<1>/SA<14>	I	Interrupt request from on board logic or Address input from ISA bus depending on mode selected.

*Signal name with a Ò*Ó means its an active low signal.

Note 1: ÒOSCÓ clock from ISA Bus is fixed at a standard frequency of 14.318 MHz. NM95MS16 is designed and tested for 14.318 MHz. However NM95MS16 can handle frequencies up to 24 MHz though it is not 100% tested.

Pinout Details for the NM95MS16

Mode 00 = DMA Mode; Mode 01 = Extended Interrupt Mode

TQFP Pin	DMA Mode	Ext.Intr.Mode
1	RSTDRV	RSTDRV
2	IOCS1*	IOCS1*
3	IOCS0*	IOCS0*
4	IORD*	IORD*
5	IOWR*	IOWR*
6	V_{CC}	V_{CC}
7	DRQIN	SA15
8	DACKOUT*	IOCS2*
9	GND	GND
10	IRQIN1	SA14
11	IRQIN0	IRQIN0
12	IRQOUT5	IRQOUT5
13	IRQOUT4	IRQOUT4
14	IRQOUT3	IRQOUT3
15	IRQOUT2	IRQOUT2
16	IRQOUT1	IRQOUT1
17	IRQOUT0	IRQOUT0
18	ISADRQ0	IRQOUT6
19	ISADRQ1	IRQOUT7
20	ISADACK0*	SA12
21	ISADACK1*	SA13
22	CS	CS
23	SK	SK
24	SA0	SA0

TQFP Pin	DMA Mode	Ext.Intr.Mode
25	SA1	SA1
26	SA2	SA2
27	SA3	SA3
28	SA4	SA4
29	GND	GND
30	SA5	SA5
31	SA6	SA6
32	SA7	SA7
33	SA8	SA8
34	SA9	SA9
35	SA10	SA10
36	SA11	SA11
37	DI	DI
38	DO	DO
39	AEN	AEN
40	OSC	OSC
41	SD0	SD0
42	SD1	SD1
43	SD2	SD2
44	SD3	SD3
45	SD4	SD4
46	SD5	SD5
47	SD6	SD6
48	SD7	SD7

Note: Mode selection (00 or 01) is done by setting MS bits in the EEPROM configuration register. Detailed information about this is described in UserÕs Guide.

Absolute Maximum Ratings (Note 2)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} + 1V to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V Min

Operating Conditions

Ambient Operating Temperature NM95MS16	0°C to +70°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 3)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz			15	mA
I_{LI}	Input Leakage Current	V_{IN} = GND or V_{CC}		0.2	15	mA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			15	mA
V_{IL}	Input Low Voltage		-0.1	0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA (Note 5) I_{OL} = 2.1 mA (Note 6)			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -3 mA (Note 5) I_{OH} = -400 mA (Note 6)	2.4 2.4			V V

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
CI/O (Note 4)	Input/Output Capacitance	VI/O = 0V	8	pF
CIN (Note 4)	Input Capacitance	VIN = 0V	6	pF
COUT (Note 4)	Output Capacitance	VOUT = 0V	6	pF

Note 2: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 4: This parameter is periodically sampled and not 100% tested.

Note 5: These values are for ISA signals like SD[0:7], IRQx, DRQx.

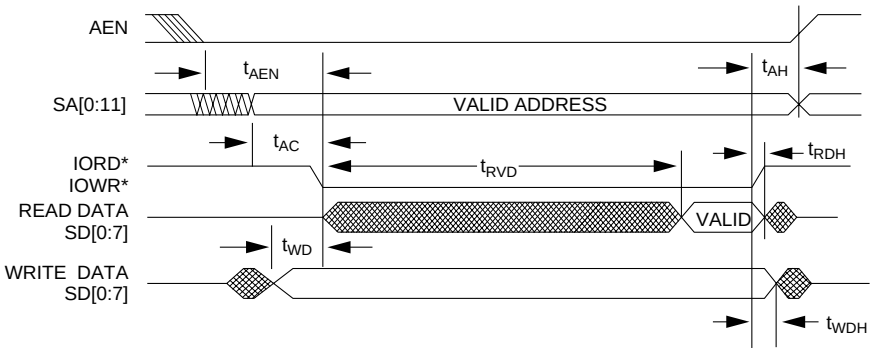
Note 6: These values are for card signal like IOCS[0:3]*, DO(EEPROM).

AC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
t_{AEN}	AEN Valid to Command Active	100		ns
t_{AC}	Address Valid to Command Active	88		ns
t_{RVD}	Active Read to Valid Data		200	ns
t_{AH}	Address, AEN Hold from Inactive Command	30		ns
t_{RDH}	Read Data Hold from Inactive Read		5	ns
t_{WD}	Write Data Valid before Write Active	22		ns
t_{WDH}	Write Data Hold after Write Inactive	25		ns
t_{CSA}	Chip Selects Valid from Address Valid	5	25	ns
t_{CSC}	Chip Selects Valid from Command Active	5	25	ns
t_{IDD}	Propagation Delay for IRQ/DRQ/DACK	5	25	ns

Timing Diagrams

Timings for ISA Read/Write Cycle



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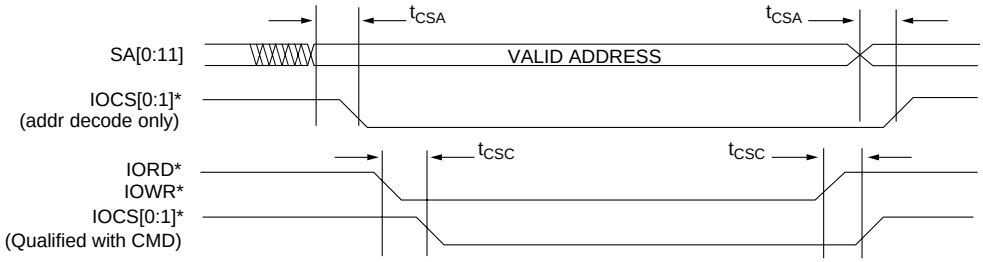
Decode Delay for Chipselect Generation



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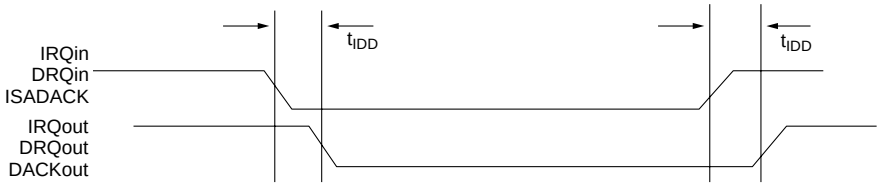
Propagation Delay for IRQ/DRQ/DACK



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INTRODUCTION

The NM95MS16 is a single-chip solution for the ISA Plug and Play (PnP) specification. It implements the complete state machine and the necessary logic for supporting configurable Interrrupts and DMA channels on the ISA bus for one logical device. Apart from providing ÒPnPÓ capability, it has built-in EEPROM that eliminates external EEPROM. This device is available in a space saving 48-pin Thin Quad Flat Pack (TQFP) package.

Functional Description

NM95MS16 has two modes of operation, viz, ÒDMA modeÓ and ÒExtended Interrupt modeÓ. These modes are programmed using the mode select (MS) bits in one of the configuration registers (Refer to the NM95MS16 UserÕs guide for detailed information). Each of these modes are discussed below.

DMA Mode

In the DMA mode, support is provided for

1. One on-board DMA request that is switchable to any two DMA channels on the ISA bus.
2. Two on-board interrupt request lines switchable to any six IRQ lines on the ISA bus.
3. Two programmable I/O chip selects for on-board logic.

Figure 1 shows a Block Diagram of NM95MS16 configured for DMA Mode.

INTRODUCTION (Continued)

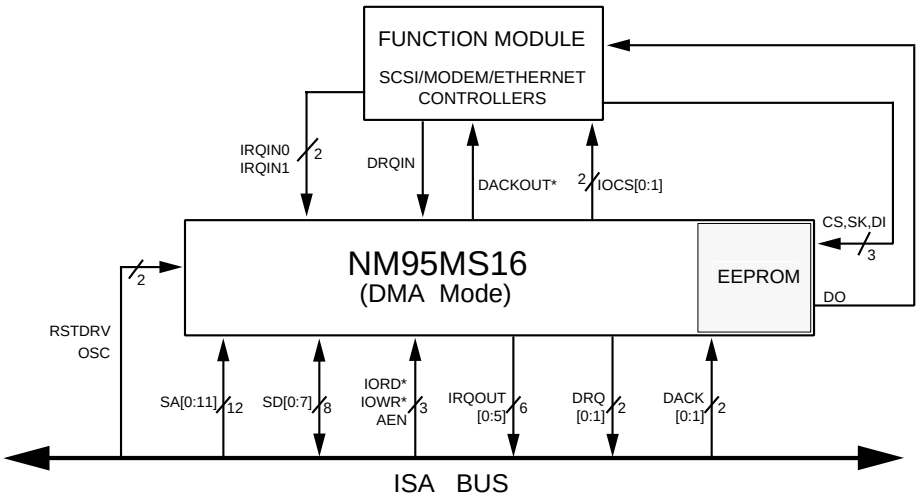

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FIGURE 1.

Extended Interrupt Mode

In the Ext.Int. mode, support is provided for:

1. Two on-board interrupt request lines switchable to any eight IRQ lines on the ISA bus.
2. Three programmable I/O chip selects for on-board logic.
3. ISA address SA12ÐSA15 are also included for extended decode.

Figure 2 shows a Block Diagram of NM95MS16 configured for Extended Interrupt Mode.

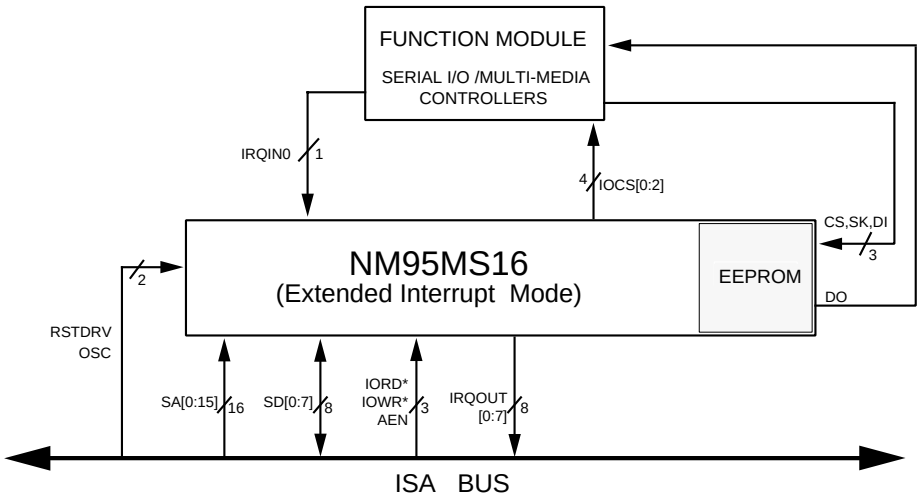

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FIGURE 2.

Chipselect Generation

Individual I/O chipselect can be generated in the following two ways:

A) Address Decode only

B) Address Decode qualified by Command (IORD*, IOWR*).

On-Chip EEPROM

NM95MS16 has 6 kbits of EEPROM on chip. All the PnP resource data structure for the logical device is stored in this EEPROM. Of the 6 kbits, 4 kbits are available for the logical deviceÕs external usage. The logical device can access the EEPROM through a microwire port, which is essentially a 4-wire serial bus. The pins CS, SK, DI and DO follow the exact timing as the standard microwire bus and are compatible to the NM93Cxx family of EEPROMs.

INTRODUCTION (Continued)

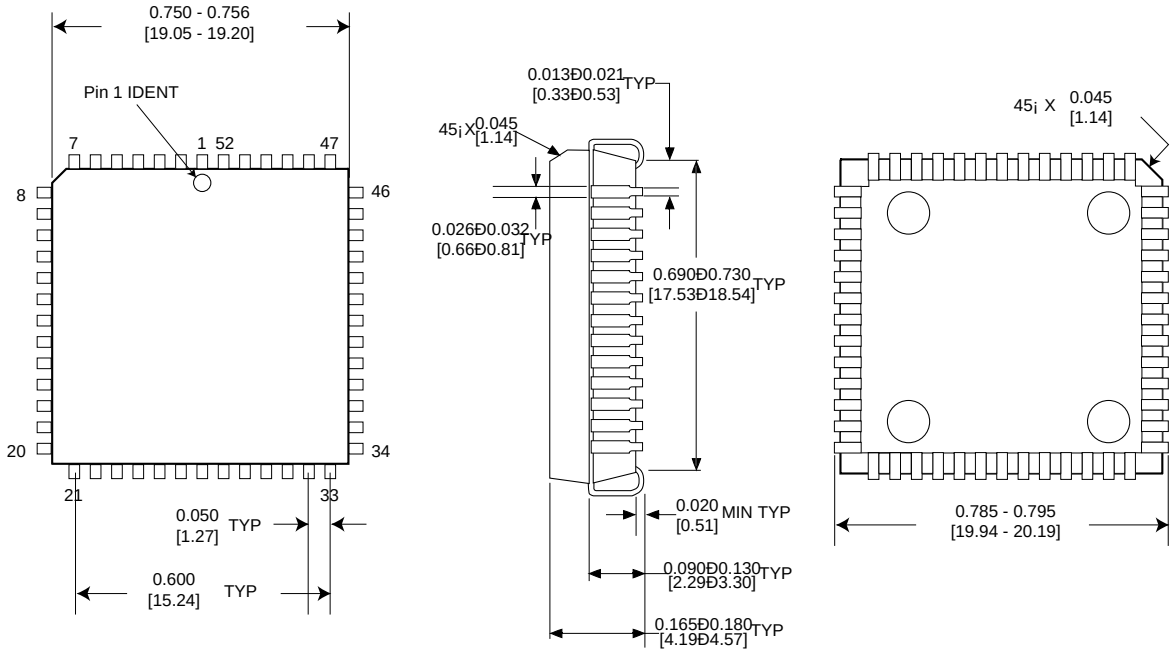
EEPROM Programming

The entire 6 kbits of EEPROM can be programmed through the ISA bus. The EEPROM can be programmed by putting the device (NM95MS16) in the Config. state (as defined in the PnP standard). Under this state 4 registers at address 0xF0Đ0xF3 are accessible to program the EEPROM. The data to be programmed is loaded in register at address 0xF3 and 0xF2 (LSB and MSB respectively). The address to be programmed is loaded in register at address 0xF1. The Ninth bit of address for 6 kbits of memory is provided through the register at address 0xF0. Both read write are possible. The actual operation does not begin until Go Ahead (GA) bit is set. Programming a word takes approximately 10 ms. The status of the operation can be polled by the Status bit. This bit is set when the operation is in progress and will be reset when complete. The register at address 0xF0 is COMMAND register. This is the handshake register in programming the EEPROM and is explained below in a tabular format.

COMMAND Register	0xF0	Bit[1:0]	ÑOP Code bits	10 - Read operation 01 - Write operation 11 - Erase operation
		Bit[2]	ÑGA(Go ahead bits)	If set to 1 the programming will continue.
		Bit[6:3]	ÑReserved, should be 0.	
		Bit[7]	ÑIt provides A8 of the address. A[0:7] is provided by 0xF1 reg. (Note 7)	
Address Register	0xF1	AddressRegister [A0ĐA7]		
Data Register	0xF2	Data Byte [MSB]		
Data Register	0xF3	Data Byte [LSB]		
STATUS Register	0x05	Bit[0]	ÑStatus/Busy bit.	Ò0Ó if busy, Ò1Ó is done.

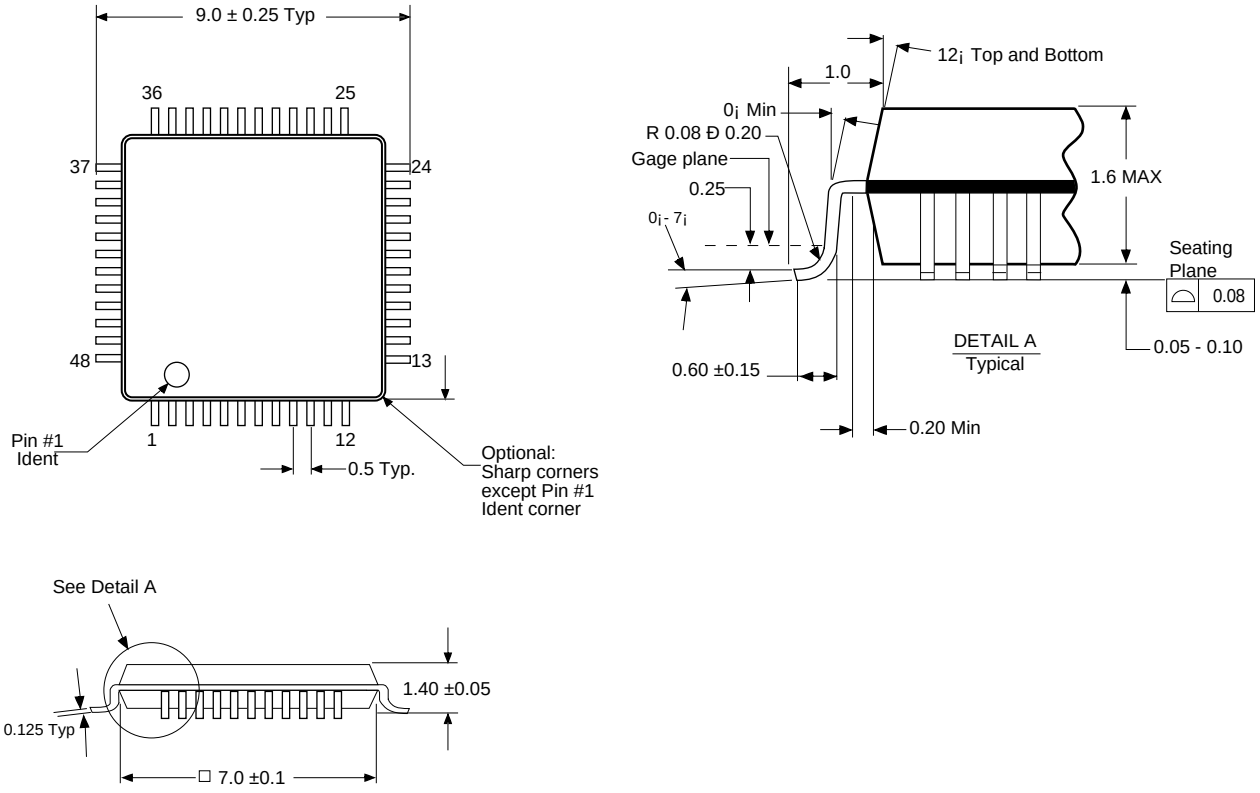
Note 7: The PNP resource data portion of the internal memory is at high address. Hence to program that portion, bit [7] of register 0xF0 (Address A8) should be set to Ò1Ó.

Physical Dimensions inches (millimeters) unless otherwise noted



52-Lead Molded Plastic Leaded Chip Carrier
Package Number V52A
Order Number NM95MS16V

Physical Dimensions inches (millimeters) unless otherwise noted



TQFP Package (VBH)
Package Number VBH48A
Order Number NM95MS16VBH

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