Obsolete Device

27C512A

512K (64K x 8) CMOS EPROM

FEATURES

- High speed performance
- CMOS Technology for low power consumption
  - 25 mA Active current
  - 30 µA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- High speed express programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - Tape and reel
- Data Retention > 200 years
- Available for the following temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

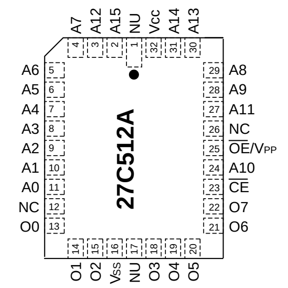
DESCRIPTION

The Microchip Technology Inc. 27C512A is a CMOS 512K bit electrically Programmable Read Only Memory (EPROM). The device is organized into 64K words by 8 bits (64K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

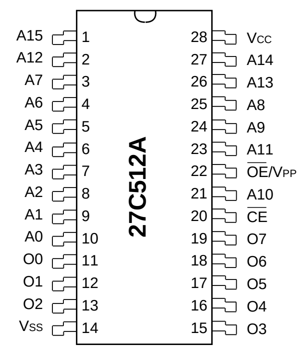
A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape or reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

PLCC



DIP/SOIC



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC} and input voltages w.r.t. V_{SS} .... -0.6V to +7.25V

V_{PP} voltage w.r.t. V_{SS} during programming .... -0.6V to +14V

Voltage on A9 w.r.t. V_{SS} .... -0.6V to +13.5V

Output voltage w.r.t. V_{SS} ....-0.6V to V_{CC} +1.0V

Storage temperature ....-65°C to +150°C

Ambient temp. with power applied .....-65°C to +125°C

*Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A15	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable/Programming Voltage
O0 - O7	Data Output
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

V_{CC} = +5V ±10%
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.5	V_{CC}+1 0.8	V V	
Input Leakage	all		I_{LI}	-10	10	µA	V_{IN} = 0 to V_{CC}
Output Voltages	all	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 400 µA I_{OL} = 2.1 mA
Output Leakage	all	—	I_{LO}	-10	10	µA	V_{OUT} = 0V to V_{CC}
Input Capacitance	all	—	C_{IN}	—	6	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	C_{OUT}	—	12	pF	V_{OUT} = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I, E	TTL input TTL input	I_{CC} I_{CC}	— —	25 35	mA mA	V_{CC} = 5.5V f = 1 MHz; $\overline{OE}/V_{PP}$ = $\overline{CE}$ = V_{IL}; I_{OUT} = 0 mA; V_{IL} = -0.1 to 0.8V; V_{IH} = 2.0 to V_{CC}; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	$I_{CC(S)TLL}$ $I_{CC(S)TLL}$ $I_{CC(S)CMOS}$	— — —	1 2 30	mA mA µA	 $\overline{CE}$ = Vcc±0.2V

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

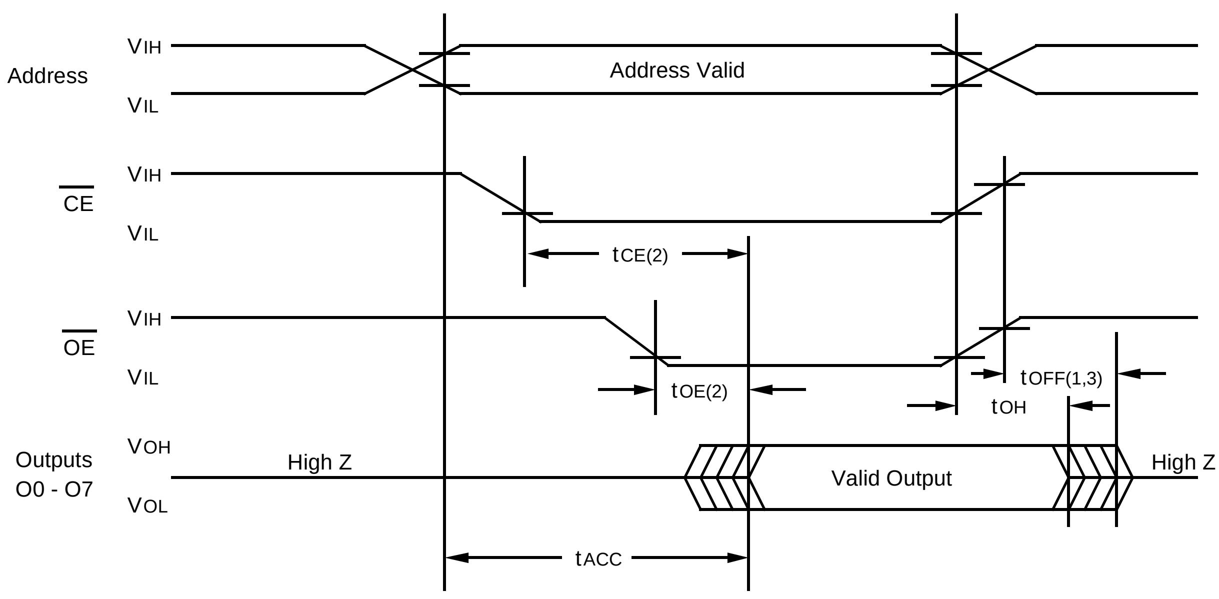
TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform:	V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 2.0V and V_{OL} = 0.8V
Output Load:	1 TTL Load + 100 pF
Input Rise and Fall Times:	10 ns
Ambient Temperature:	Commercial: Tamb = 0°C to +70°C
	Industrial: Tamb = -40°C to +85°C
	Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Sym	27C512-90*		27C512-10*		27C512-12		27C512-15		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	90	—	100	—	120	—	150	ns	$\overline{CE}$ = $\overline{OE}$/V_{PP} = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	90	—	100	—	120	—	150	ns	$\overline{OE}$/V_{PP} = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	—	40	—	40	—	50	—	60	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to Output High Impedance	t_{OFF}	0	35	0	35	0	40	0	45	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$/V_{PP}, whichever occurred first	t_{OH}	0	—	0	—	0	—	0	—	ns	

*90/10 AC Testing Waveforms: V_{IH} = 3.0V and V_{IL} = 0V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: Tamb = 25°C ± 5°C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25V

Parameter	Status	Symbol	Min.	Max.	Units	Conditions (See Note 1)
Input Voltages	Logic “1” Logic “0”	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	µA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic “1” Logic “0”	V_{OH} V_{OL}	2.4 —	 0.45	V V	I_{OH} = -400 µA I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	35	mA	$\overline{CE}$ = V_{IL}
$\overline{OE}/V_{PP}$ Current, program	—	I_{PP2}	—	25	mA	
A9 Product Identification	—	V_{ID}	11.5	12.5	V	

Note 1: V_{CC} must be applied simultaneously or before V_{PP} voltage on $\overline{OE}/V_{PP}$ and removed simultaneously or after the V_{PP} voltage on $\overline{OE}/V_{PP}$.

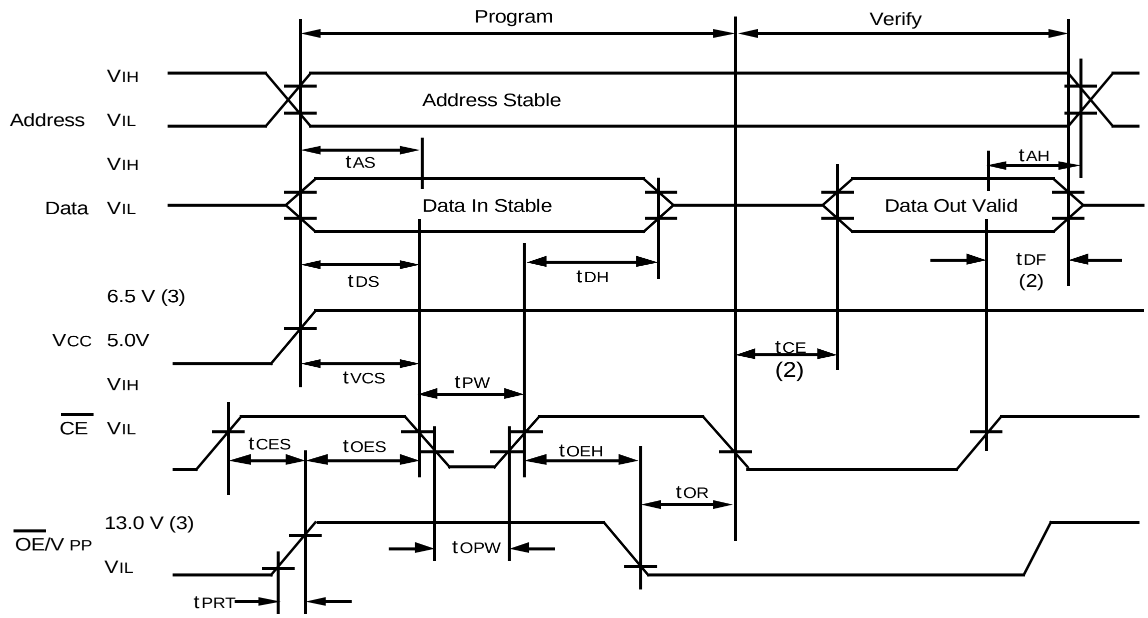
TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes
AC Testing Waveform: V_{IH}=2.4V and V_{IL}=0.45V; V_{OH}=2.0V; V_{OL}=0.8V
Ambient Temperature: 25°C ±5°C
V_{CC} = 6.5V ± 0.25V, $\overline{OE}/V_{PP}$ = V_H = 13.0V ± 0.25 V

Parameter	Symbol	Min.	Max.	Units	Remarks
Address Set-Up Time	t_{AS}	2	—	µs	
Data Set-Up Time	t_{DS}	2	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Float Delay (2)	t_{DF}	0	130	ns	
V_{CC} Set-Up Time	t_{VCS}	2	—	µs	
Program Pulse Width (1)	t_{PW}	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	µs	
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	µs	
$\overline{OE}$ Hold Time	t_{OEH}	2	—	µs	
$\overline{OE}$ Recovery Time	t_{OR}	2	—	µs	
$\overline{OE}$ /V_{PP} Rise Time During Programming	t_{PRT}	50	—	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
2: This parameter is only sampled and not 100% teted. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
(2) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer.
(3) V_{CC} = 6.5V ±0.25V, V_{PP} = V_H = 13.0V ±0.5V for express programming algorithm.

TABLE 1-6: MODES

Operation Mode	CE	OE/VPP	A9	O0 - O7
Read	VIL	VIL	X	DOUT
Program	VIL	VH	X	DIN
Program Verify	VIL	VIL	X	DOUT
Program Inhibit	VIH	VH	X	High Z
Standby	VIH	X	X	High Z
Output Disable	VIL	VIH	X	High Z
Identity	VIL	VIL	VH	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the CE pin is low to power up (enable) the chip
b) the OE/VPP pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of OE/VPP.

1.3 Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and the program mode is not identified.

When this conditions are met, the supply current will drop from 25 mA to 30 µA.

1.4 Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus connection in multiple bus microprocessor systems and the outputs go to high impedance when:

- the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

1.5 Erase Mode (UV Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1's" state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/ cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 mW/cm^2 for approximately 40 minutes.

1.6 Programming Mode

The Express algorithm must be used for best results. It has been developed to improve programming yields and throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level, and
c) $\overline{CE}$ line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) the $\overline{OE}$/VPP pin is low, and
c) the $\overline{CE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

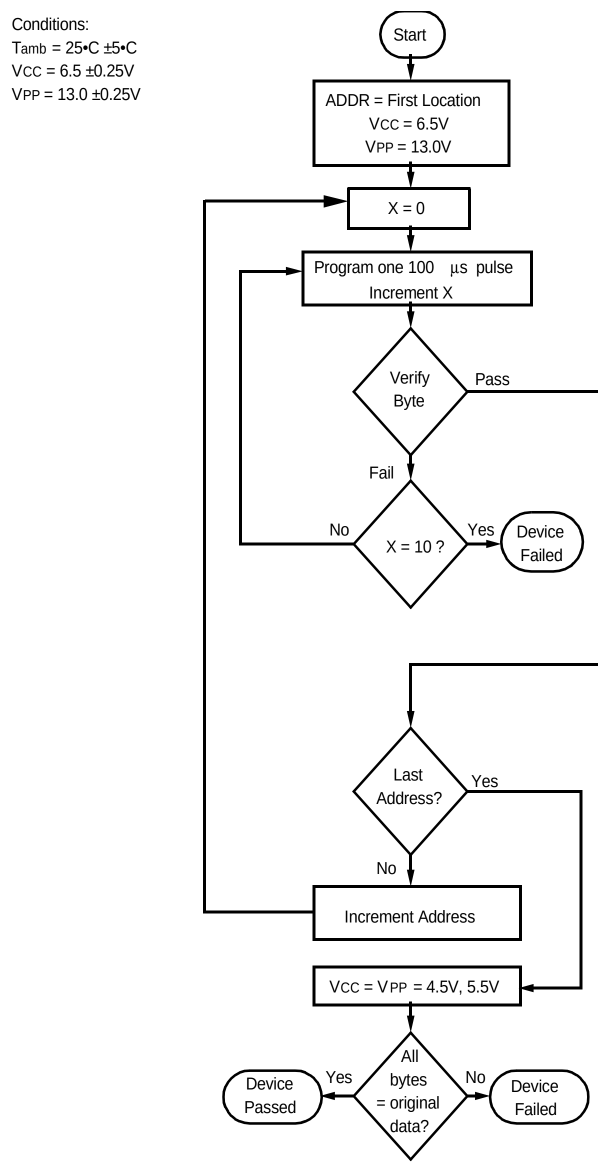
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin	Input	Output								
Identity	A0	07	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	1	1	0	0	0D

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C512A Product Identification System

To order or to obtain information (e.g., on pricing or delivery),, please use listed part numbers, and refer to factory or listed sales offices.

27C512A – 70 I /P

Package:	L	=	Plastic Leaded Chip Carrier
	P	=	Plastic DIP (600 Mil)
	SO	=	Plastic SOIC (300 Mil)
Temperature Range:	Blank	=	0°C to +70°C
	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Access Time:	90	=	90 ns
	10	=	100 ns
	12	=	120 ns
	15	=	150 ns
Device:	27C512A		512K (64K x 8) CMOS EPROM

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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