Honeywell

HTMOS™ High Temperature Products

HIGH TEMPERATURE 32K x 8 STATIC RAM HT6256

FEATURES

- Specified Over -55 to +225°C
- Fabricated with HTMOS™ IV Silicon on Insulator (SOI)
- Read/Write Cycle Times ≤ 50 ns Support 20 MHz Clock
- Asynchronous Operation
- CMOS Input/Output Buffers
- Single 5 V ± 10% Power Supply
- Hermetic 28-Lead Ceramic DIP

APPLICATONS

- Down-Hole Oil Well
- Avionics
- Turbine Engine Control
- Industrial Process Control
- Nuclear Reactor
- Electric Power Conversion
- Heavy Duty Internal Combustion Engines

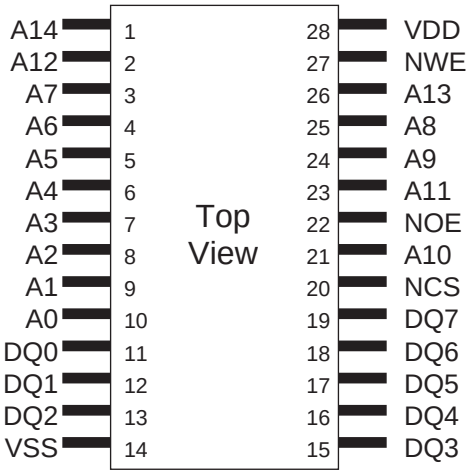
GENERAL DESCRIPTION

The 32K x 8 High Temperature Static RAM is a high performance 32,768 word x 8-bit static random access memory with industry-standard functionality. It is fabricated with Honeywell's HTMOS™ technology, and is designed for use in systems operating in severe high temperature environments.

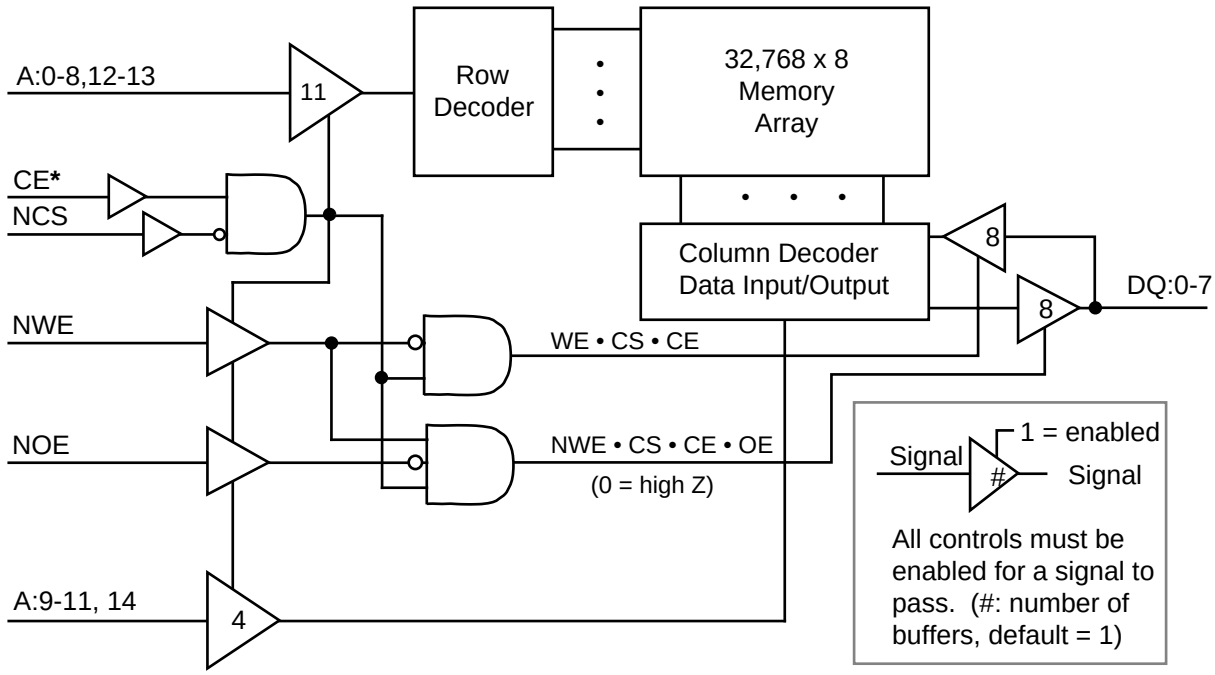
The RAM requires only a single 5 V ± 10% power supply and has CMOS compatible I/O. Power consumption is typically less than 30 mW/MHz in operation, and less than 10 mW when de-selected. The RAM read operation is fully asynchronous, with an associated typical access time of 50 ns at 5 V.

The RAM provides guaranteed performance over the full -55 to +225°C temperature range. Typically, parts will operate up to +300°C for a year, with derated performance. All parts are burned in at 250°C to eliminate infant mortality.

PACKAGE PINOUT



FUNCTIONAL DIAGRAM



SIGNAL DEFINITIONS

A: 0-14 Address input pins which select a particular eight-bit word within the memory array.

DQ: 0-7 Bidirectional data pins which serve as data outputs during a read operation and as data inputs during a write operation.

NCS Negative chip select, when at a low level allows normal read or write operation. When at a high level NCS forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables all input buffers. If this signal is not used it must be connected to VSS.

NWE Negative write enable, when at a low level activates a write operation and holds the data output drivers in a high impedance state. When at a high level NWE allows normal read operation.

NOE Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by NCS and NWE. If this signal is not used it must be connected to VSS.

CE* External control of Chip Enable is an extra feature available only in other package options. Chip enable, when at a high level allows normal operation. When at a low level CE forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables all the input buffers except the NCS input buffer. If this signal is not used it must be connected to VDD.

TRUTH TABLE

NCS	CE*	NWE	NOE	MODE	DQ
L	H	H	L	Read	Data Out
L	H	L	X	Write	Data In
H	X	XX	XX	Deselected	High Z
X	L	XX	XX	Disabled	High Z

Notes:
X: VI=VIH or VIL
XX: VSS≤VI≤VDD
NOE=H: High Z output state maintained for NCS=X, CE=X, NWE=X

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter		Rating		Units
			Min	Max	
VDD	Supply Voltage Range (2)		-0.5	6.5	V
VPIN	Voltage on Any Pin (2)		-0.5	VDD+0.5	V
TSTORE	Storage Temperature (Zero Bias)		-65	325	°C
TSOLDER	Soldering Temperature (5 Seconds)			355	°C
PD	Maximum Power Dissipation (3)			2	W
IOUT	DC or Average Output Current			25	mA
VPROT	ESD Input Protection Voltage (4)		2000		V
ΘJC	Thermal Resistance (Jct-to-Case)	28 DIP		10	°C/W

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Voltage referenced to VSS.
(3) RAM power dissipation (IDDSB + IDDOP) plus RAM output driver power dissipation due to external loading must not exceed this specification.
(4) Class 2 electrostatic discharge (ESD) input protection. Tested per MIL-STD-883, Method 3015 by DESC certified lab.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Description			Units
		Min	Typ	Max	
VDD	Supply Voltage (referenced to VSS)	4.5	5.0	5.5	V
TA	Ambient Temperature	-55	25	225	°C
VPIN	Voltage on Any Pin (referenced to VSS)	-0.3		VDD+0.3	V

CAPACITANCE (1)

Symbol	Parameter	Typical (2)	Worst Case		Units	Test Conditions
			Min	Max		
CI	Input Capacitance	5		7	pF	VI=VDD or VSS, f=1 MHz
CO	Output Capacitance	7		9	pF	VIO=VDD or VSS, f=1 MHz

(1) This parameter is tested during initial design characterization only
(2) Typical operating conditions: TA= 25°C.

DATA RETENTION CHARACTERISTICS (1)

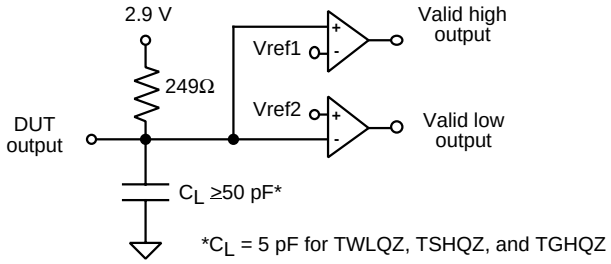
Symbol	Parameter	Typical	Worst Case		Units	Test Conditions
			Min	Max		
VDR	Data Retention Voltage		2.5		V	NCS=VDR VI=VDR or VSS
IDR	Data Retention Current			500 330	µA µA	NCS=VDD=2.5V, VI=VDD or VSS NCS=VDD=3.0V, VI=VDD or VSS

(1) Operating conditions: TA= -55°C to +125°C.

DC ELECTRICAL CHARACTERISTICS

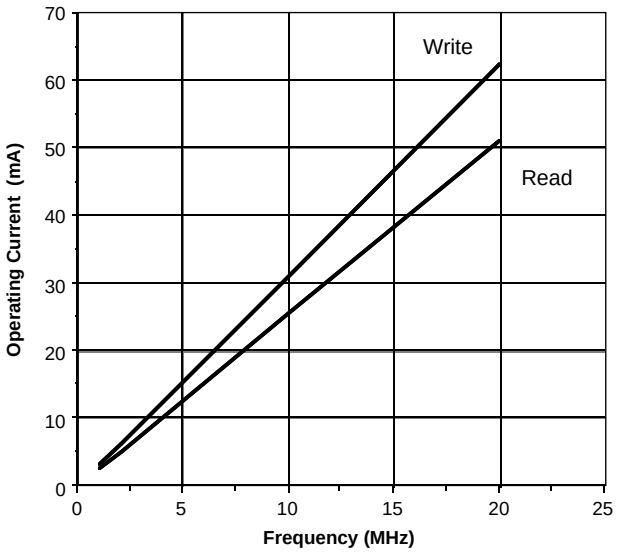
Symbol	Parameter	Test Conditions	Typ (1)	Worst Case (2)		Units
				Min	Max	
IDDSB1	Static Supply Current	VIH=VDD, IO=0 VIL=VSS, f=0MHz	0.2		2.0	mA
IDDSBMF	Standby Supply Current—Deselected	NCS=VDD, IO=0, f=40 MHz	0.2		2.0	mA
IDDOPW	Dynamic Supply Current—Selected (Write)	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS (3)	3.4		4.0	mA
IDDOPR	Dynamic Supply Current—Selected (Read)	f=1 MHz, IO=0, CE=VIH=VDD NCS=VIL=VSS (3)	2.8		4.0	mA
II	Input Leakage Current	VSS VI VDD		-5	+5	µA
IOZ	Output Leakage Current	VSS VIO VDD Output=high Z		-10	+10	µA
VIL	Low-Level Input voltage	March Pattern	1.7		0.3xVdd	V
VIH	high-Level Input Voltage	March Pattern	3.2	0.7xVdd		V
VOL	Low-Level Output voltage	VD =4.5V, IOL=10 mA (CMOS) VDD=4.5V, IO =200 µA	0.3 0.005		0.4 0.05	V V
VOH	High-Level Output Voltage	VDD=4.5V, IOH=-5 mA VDD=4.5V, IOH=-200 µA	4.3 4.5	4.2 Vdd-0.05		V V

(1) Typical operating conditions: VDD= 5.0 V,TA=25°C.
(2) Worst case operating conditions: VDD= 5.0 V ±10%, TA=-55°C to +225°C.
(3) All inputs switching. DC average current. External control of Chip Enable (CE) is available only in other package options.

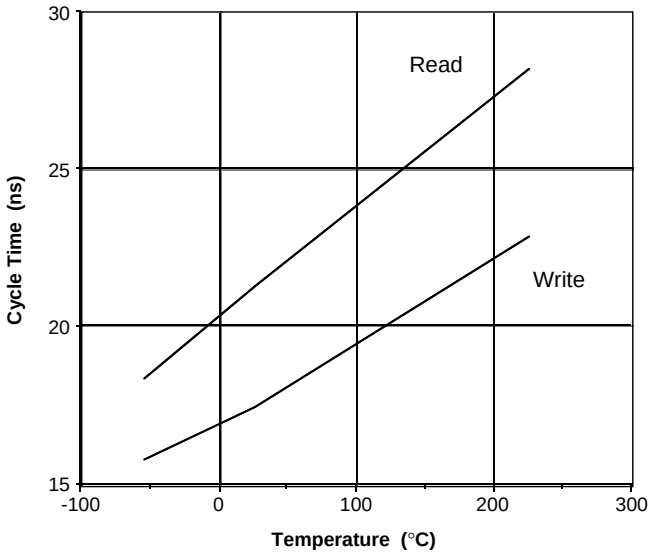


Tester Equivalent Load Circuit

Operating Current vs. Frequency @ 225°C



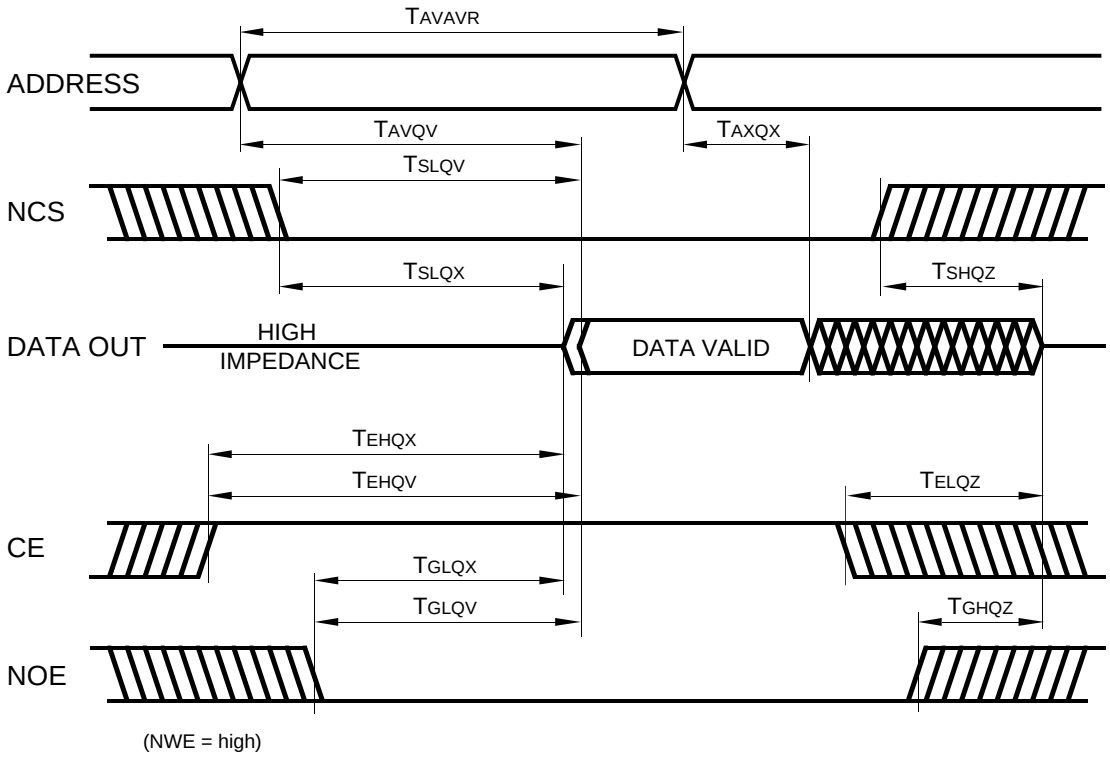
Cycle Times vs. Temperature



READ CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameter	Typical (2)	Worst Case (3)		Units
			Min	Max	
TAVAVR	Address Read Cycle Time		50		ns
TAVQV	Address Access Time			50	ns
TAXQX	Address Change to Output Invalid Time		3		ns
TSLQV	Chip Select Access Time			50	ns
TSLQX	Chip Select Output Enable Time		5		ns
TSHQZ	Chip Select Output Disable Time			20	ns
TGLQV	Output Enable Access Time			15	ns
TGLQX	Output Enable Output Enable Time		0		ns
TGHQZ	Output Enable Output Disable Time			15	ns
TEHQV	Chip Enable Output Access Time (4)	17		25	ns
TEHQX	Chip Enable Output enable Time (4)	10	5		ns
TELQZ	Chip Enable Output Disable Time (4)	4		10	ns

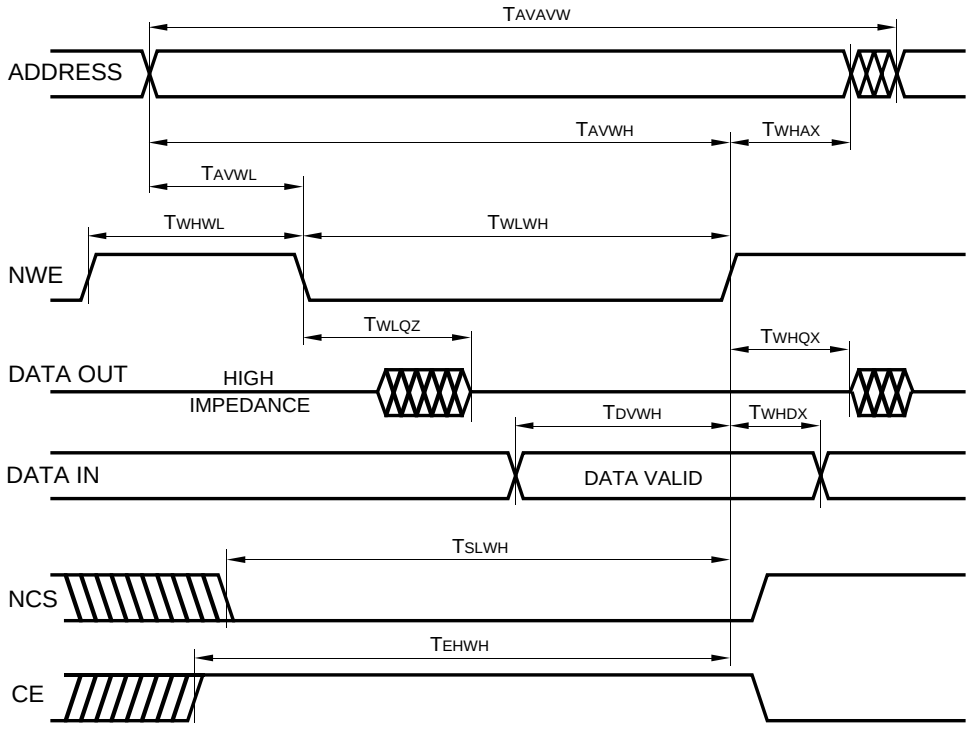
(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V, input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading $C_L \geq 50$ pF, or equivalent capacitive output loading C_L=5 pF for TSHQZ and TGHQZ. For C_L >50 pF, derate access times by 0.02 ns/pF (typical).
(2) Typical operating conditions: VDD=5.0 V, TA=25°C.
(3) Worst case operating conditions: VDD=4.5 V to 5.5 V, -55 to 225°C.
(4) External control of Chip Enable (CE) is available only in other package options.



WRITE CYCLE AC TIMING CHARACTERISTICS (1)

Symbol	Parameters	Typical (2)	Worst Case (3)		Units
			Min	Max	
TAVAVW	Write Cycle Timing (4)		50		ns
TWLWH	Write Enable Write Pulse Width		45		ns
TSLWH	Chip Select to End of Write Time		45		ns
TDVWH	Data Valid to End of Write Time		35		ns
TAVWH	Address Valid to End of Write Time		45		ns
TWHDX	Data Hold Time after End of Write Time		0		ns
TAVWL	Address Valid Setup to Start of Write Time		0		ns
TWHAX	Address Valid after End of Write Time		0		ns
TWLQZ	Write Enable to Output Disable Time		0	15	ns
TWHQX	Write Disable to Ouput Enable Time		5		ns
TWHWL	Write Disable to Write Enable Pulse Width (5)		5		ns
TEHWH	Chip Enable to End of Write Time (6)		45		ns

(1) Test conditions: input switching levels VIL/VIH=0.5V/VDD-0.5V, input rise and fall times <1 ns/V, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading ≥50 pF, or equivalent capacitive load of 5 pF for TWLQZ.
(2) Typical operating conditions: VDD=5.0 V, TA=25°C.
(3) Worst case operation conditions: VDD=4.5 V to 5.5 V, -55 to 225°C.
(4) TAVAVW = TWLWH + TWHWL
(5) Guaranteed but not tested.
(6) External control of Chip Enable (CE) is available only in other package options.



DYNAMIC ELECTRICAL CHARACTERISTICS

Read Cycle

The RAM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select (NCS), or chip enable (CE) (refer to Read Cycle timing diagram). To perform a valid read operation, both chip select and output enable (NOE) must be low and chip enable and write enable (NWE) must be high. The output drivers can be controlled independently by the NOE signal. Consecutive read cycles can be executed with NCS held continuously low, and with CE held continuously high, and toggling the addresses.

For an address activated read cycle, NCS and CE must be valid prior to or coincident with the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid TAVQV time following the latest occurring address edge transition. The minimum address activated read cycle time is TAVAV. When the RAM is operated at the minimum address activated read cycle time, the data outputs will remain valid on the RAM I/O until TAXQX time following the next sequential address transition.

To control a read cycle with NCS, all addresses and CE must be valid prior to or coincident with the enabling NCS edge transition. Address or CE edge transitions can occur later than the specified setup times to NCS, however, the valid data access time will be delayed. Any address edge transition, which occurs during the time when NCS is low, will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TSHQZ time following a disabling NCS edge transition.

To control a read cycle with CE, all addresses and NCS must be valid prior to or coincident with the enabling CE edge transition. Address or NCS edge transitions can occur later than the specified setup times to CE; however, the valid data access time will be delayed. Any address edge transition which occurs during the time when CE is high will initiate a new read access, and data outputs will not become valid until TAVQV time following the address edge transition. Data outputs will enter a high impedance state TELQZ time following a disabling CE edge transition.

Write Cycle

The write operation is synchronous with respect to the address bits, and control is governed by write enable (NWE), chip select (NCS), or chip enable (CE) edge transitions (refer to Write Cycle timing diagrams). To perform a write operation, both NWE and NCS must be low, and CE must be high. Consecutive write cycles can be performed with NWE or NCS held continuously low, or CE held continuously high. At least one of the control signals must transition to the opposite state between consecutive write operations.

The write mode can be controlled via three different control signals: NWE, NCS, and CE. All three modes of control are similar except the NCS and CE controlled modes actually disable the RAM during the write recovery pulse. Both CE and NCS fully disable the RAM decode logic and input buffers for power savings. Only the NWE controlled mode is shown in the table and diagram on the previous page for simplicity. However, each mode of control provides the same write cycle timing characteristics. Thus, some of the parameter names referenced below are not shown in the write cycle table or diagram, but indicate which control pin is in control as it switches high or low.

To write data into the RAM, NWE and NCS must be held low and CE must be held high for at least TWLWH/TSLSH/TEHEL time. Any amount of edge skew between the signals can be tolerated, and any one of the control signals can initiate or terminate the write operation. For consecutive write operations, write pulses must be separated by the minimum specified TWHWL/TSHSL/TELEH time. Address inputs must be valid at least TAVWL/TAVSL/TAVEH time before the enabling NWE/NCS/CE edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of TDVWH/TDVSH/TDVEL, and an address valid to end of write time of TAVWH/TAVSH/TAVEL also must be provided for during the write operation. Hold times for address inputs and data inputs with respect to the disabling NWE/NCS/CE edge transition must be a minimum of TWHAX/TSHAX/TELAX time and TWHDX/TSHDX/TELDX time, respectively. The minimum write cycle time is TAVAV.

QUALITY ASSURANCE

Honeywell maintains a high level of product integrity through process control utilizing statistical process control, a complete “Total Quality Assurance System,” and a computer data base process performance tracking system. This Total Quality approach ensures our customers of a reliable product by engineering in reliability, starting with process development and continuing through product qualification and screening.

SCREENING LEVELS

Honeywell offers several levels of device screening to meet your system needs. Hi-Rel Level B devices undergo additional screening per the requirements of MIL-STD-883.

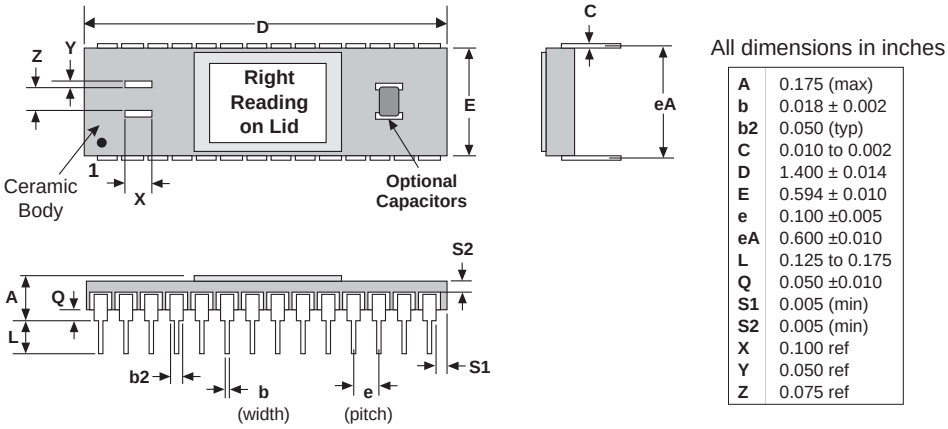
RELIABILITY

Honeywell understands the stringent reliability requirements for extreme environment systems and has extensive experience in reliability testing on programs of this nature. Reliability attributes of the HTMOS process were characterized by testing test structures from which specific failure mechanisms were evaluated. These specific mechanisms included, but were not limited to, hot carriers, electromigration and time dependent dielectric breakdown. This data was then used to make changes to the design models and process to ensure reliable -55 to +225°C specified products.

PACKAGING

The standard package is a hermetic 28-lead DIP constructed of multilayer ceramic (Al_2O_3) and features internal power and ground planes. Ceramic chip capacitors can be mounted to the package by the user to maximize supply noise decoupling and increase board packing density. These capacitors connect to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package. For packaging options with surface mount capability or external control of Chip Enable (CE), call Honeywell.

28-LEAD DIP PACKAGE



All dimensions in inches

A	0.175 (max)
b	0.018 ± 0.002
b2	0.050 (typ)
C	0.010 to 0.002
D	1.400 ± 0.014
E	0.594 ± 0.010
e	0.100 ±0.005
eA	0.600 ±0.010
L	0.125 to 0.175
Q	0.050 ±0.010
S1	0.005 (min)
S2	0.005 (min)
X	0.100 ref
Y	0.050 ref
Z	0.075 ref

ORDERING INFORMATION (1)

HT6256DC

D - Indicates package type
D = 28-Lead DIP

C - Indicates screening level
B = High Temperature Class B
C = Commercial

For packaging options, call Honeywell

(1) Orders may be faxed to 612-954-2257. Please contact our Customer Service Department at 612-954-2888 for further information.

To learn more about Honeywell Solid State Electronics Center, visit our web site at http://www.ssec.honeywell.com

Honeywell

Helping You Control Your World