STK16CA8

128K x 8 *AutoStorePlus*™ nvSRAM
QuantumTrap™ CMOS Nonvolatile Static RAM
Preliminary

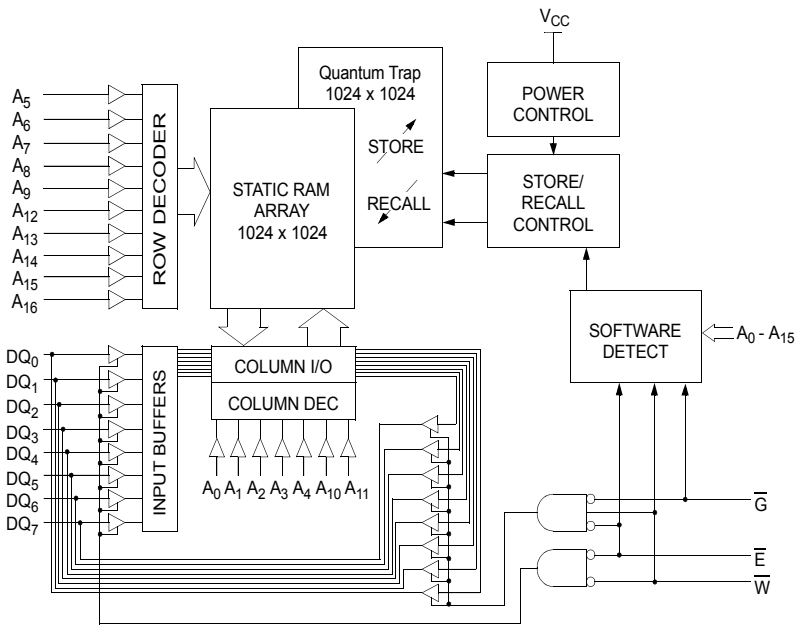
FEATURES

- **25ns, 35ns and 45ns Access Times**
- **Directly Replaces 128K x 8 Static RAM, Battery-Backed RAM or EEPROM**
- **Transparent Data Save on Power Down**
- ***STORE* to *QuantumTrap*™ Nonvolatile Elements is Initiated by Software or *AutoStorePlus*™ on Power Down**
- ***RECALL* to SRAM Initiated by Software or Power Restore**
- **5mA Typical I_{CC} at 200ns Cycle Time**
- **Unlimited READ and WRITE Cycles to SRAM**
- **100-Year Data Retention to Quantum Trap**
- **Single 3V +20%, -10% Operation**
- **Commercial and Industrial Temperatures**
- **32-Pin DIP Package**

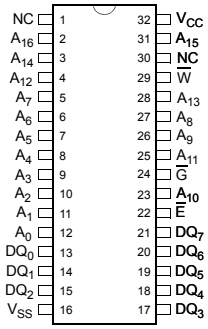
DESCRIPTION

The Simtek STK16CA8 is a fast static RAM with a nonvolatile element in each static memory cell. The embedded nonvolatile elements incorporate Simtek's *QuantumTrap*™ technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the nonvolatile elements. Data transfers from the SRAM to the nonvolatile elements (the *STORE* operation) can take place automatically on power down or under software control. An internal capacitor guarantees the *STORE* operation, even under extreme power-down slew rates or loss of power from "hot swapping". Transfers from the nonvolatile elements to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of *STORE* and *RECALL* cycles can also be controlled by entering control sequences on the SRAM inputs. The STK16CA8 is pin-compatible with 128k x 8 SRAMs and battery-backed SRAMs, allowing direct substitution while providing superior performance.

BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

A_0 - A_{16}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Power (+ 3V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Power Supply Voltage . . . . . –0.5V to +3.9V
Voltage on Input Relative to V_{SS} . . . . . –0.5V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} . . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias. . . . . –55°C to 125°C
Storage Temperature . . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 3.0V +20%, -10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[b]	Average V_{CC} Current		50 40 35		55 45 35	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC_2}[c]	Average V_{CC} Current during *STORE*		1.5		1.5	mA	All Inputs Don't Care, V_{CC} = max
I_{CC_3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns 3V, 25°C, Typical		5		5	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{SB}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		1		1	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.0	V_{CC} + .3	2.0	V_{CC} + .3	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –2mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 4mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC_2} is the average current required for the duration of the *STORE* cycle (t_{STORE}).
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input Pulse Levels . . . . . 0V to 3V
Input Rise and Fall Times. . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

CAPACITANCE[e]

(T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

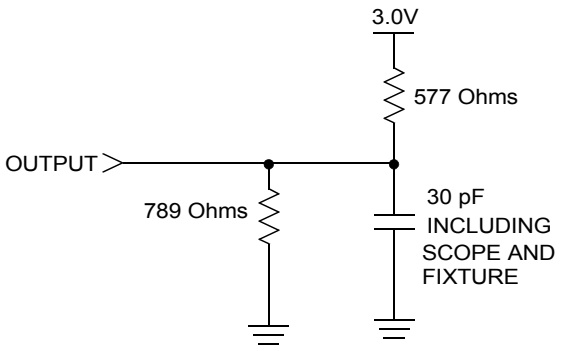


Figure 1: AC Output Loading

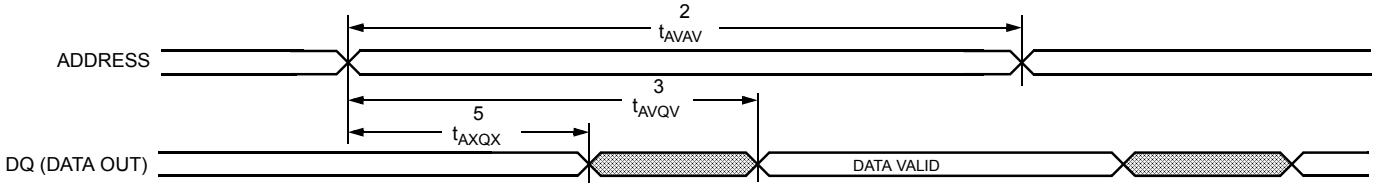
SRAM READ CYCLES #1 & #2

(V_{CC} = 3.0V +20%, -10%)

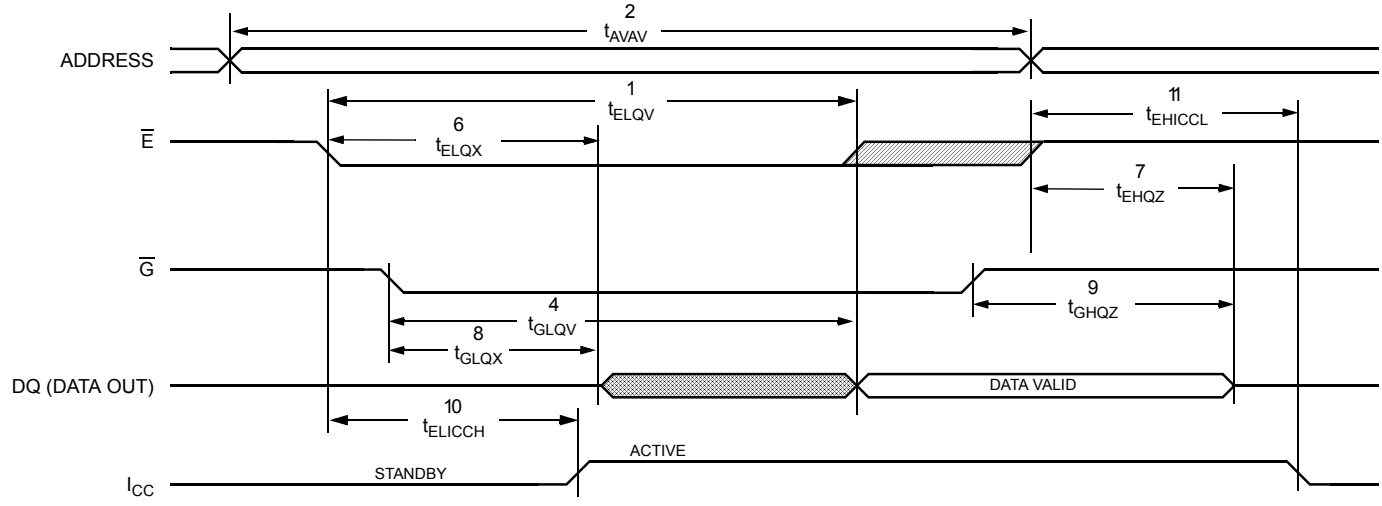
NO.	SYMBOLS		PARAMETER	STK16CA8-25		STK16CA8-35		STK16CA8-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[f]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[g]	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}[g]	t_{OH}	Output Hold after Address Change	3		3		3		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	3		3		3		ns
7	t_{EHQZ}[h]	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}[h]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}[e]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}[e]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note f: $\overline{W}$ must be high during SRAM READ cycles.
Note g: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low.
Note h: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[f, g]



SRAM READ CYCLE #2: $\overline{E}$ Controlled[f]



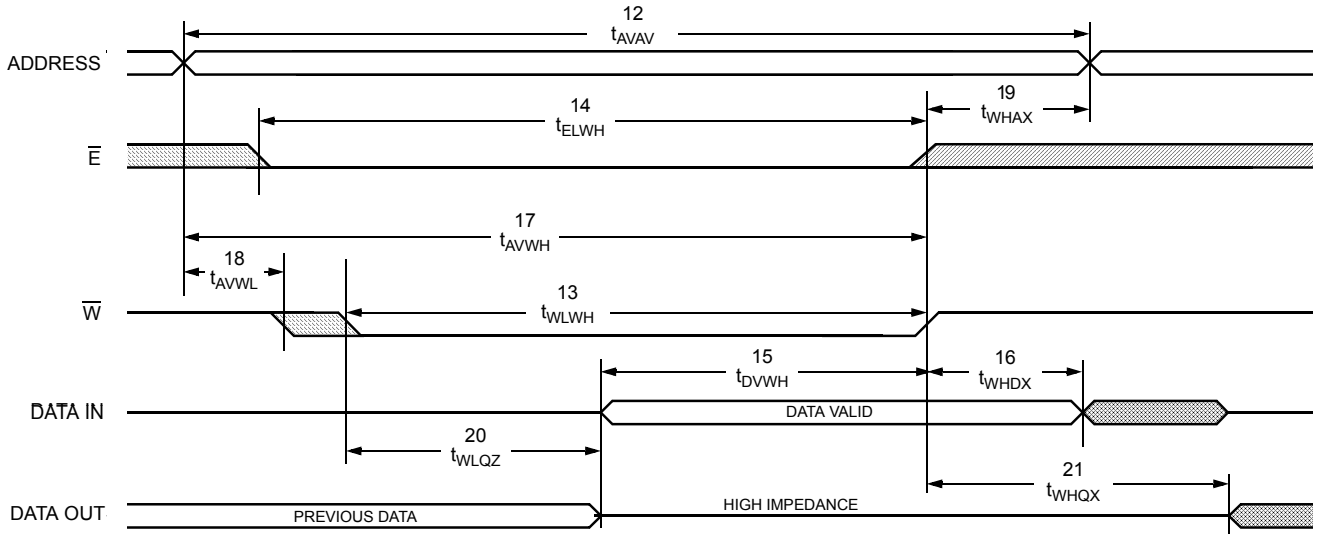
SRAM WRITE CYCLES #1 & #2

(V_{CC} = 3.0V +20%, -10%)

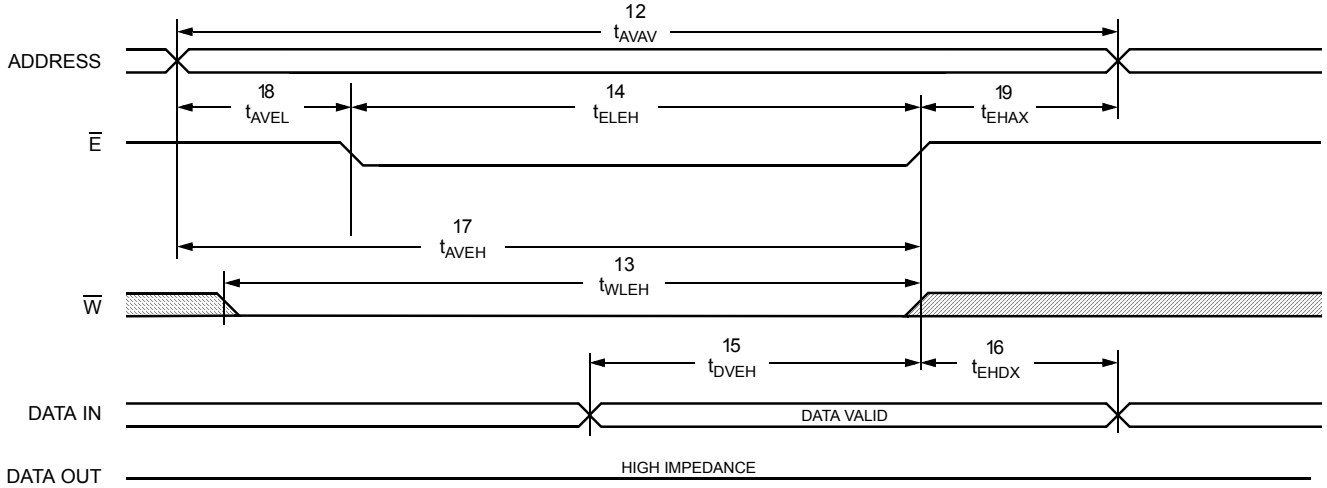
NO.	SYMBOLS			PARAMETER	STK16CA8-25		STK16CA8-35		STK16CA8-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	t_{WLQZ}[h, i]		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	3		3		3		ns

Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note j: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[j]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[j]



MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	A_{15} - A_0 (hex)	MODE	I/O	POWER	NOTES
H	X	X	X	Not Selected	Output High Z	Standby	
L	H	L	X	Read SRAM	Output Data	Active	
L	L	X	X	Write SRAM	Input Data	Active	
L	H	L	4E38 B1C7 83E0 7C1F 703F 8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Autostore Inhibit	Output Data Output Data Output Data Output Data Output Data Output Data	Active	k, l, m
L	H	L	4E38 B1C7 83E0 7C1F 703F 4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Autostore inhibit off	Output Data Output Data Output Data Output Data Output Data Output Data	Active	k, l, m
L	H	L	4E38 B1C7 83E0 7C1F 703F 8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC_2}	k, l, m
L	H	L	4E38 B1C7 83E0 7C1F 703F 4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	k, l, m

Note k: The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.
Note l: While there are 17 addresses on the STK16CA8, only the lower 16 are used to control software modes.
Note m: I/O state depends on the state of $\overline{G}$. The I/O table shown assumes $\overline{G}$ low.

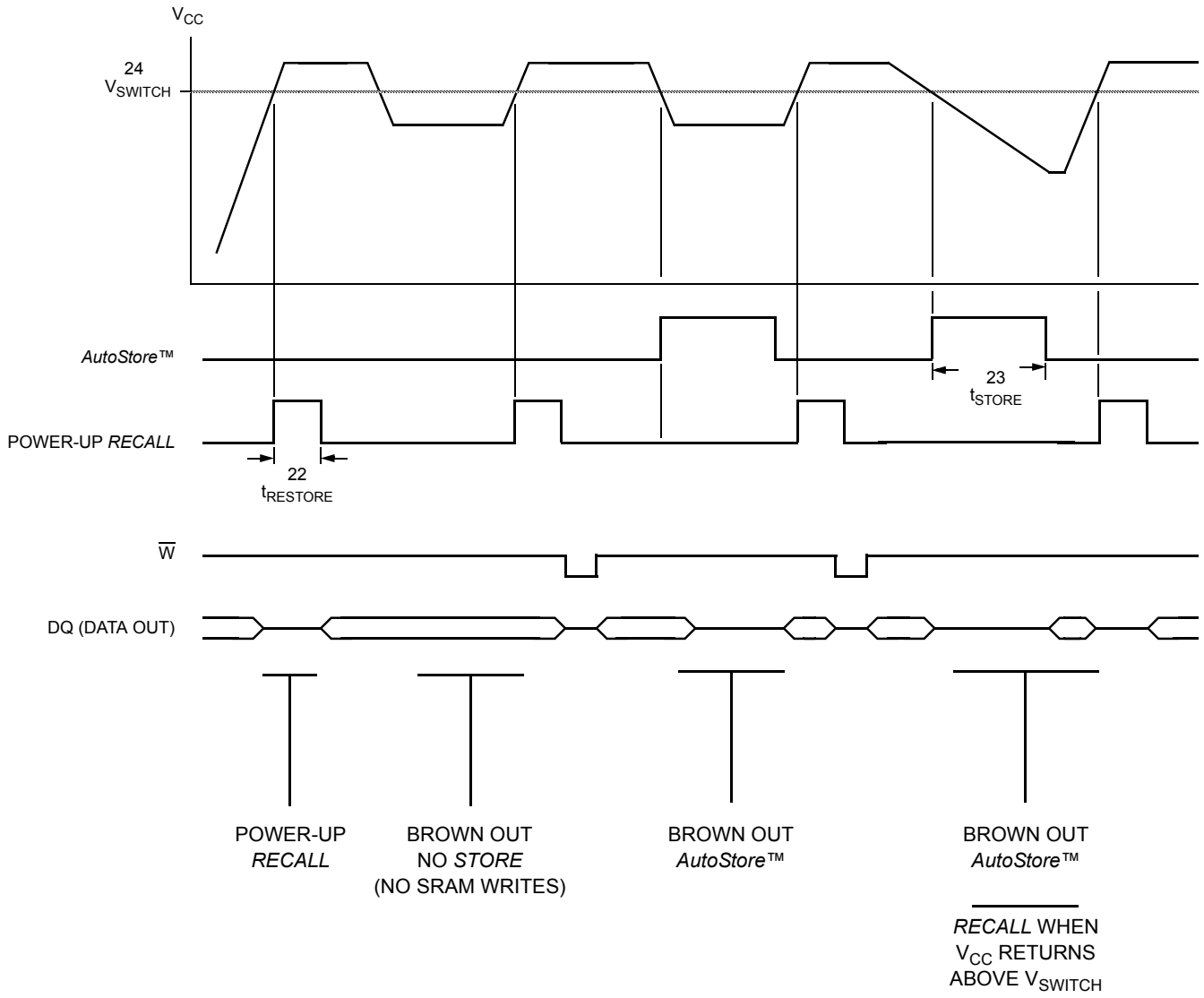
AutoStorePlus™/POWER-UP *RECALL*

(V_{CC} = 3.0V +20%, -10%)

NO.	SYMBOLS		PARAMETER	STK16CA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	$t_{RESTORE}$		Power-up *RECALL* Duration		5	ms	n
23	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	o
24	V_{SWITCH}		Low Voltage Trigger Level	2.55	2.65	V	

Note n: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.
Note o: If an SRAM WRITE has not taken place since the last nonvolatile cycle, no *STORE* will take place.

AutoStorePlus™/POWER-UP *RECALL*

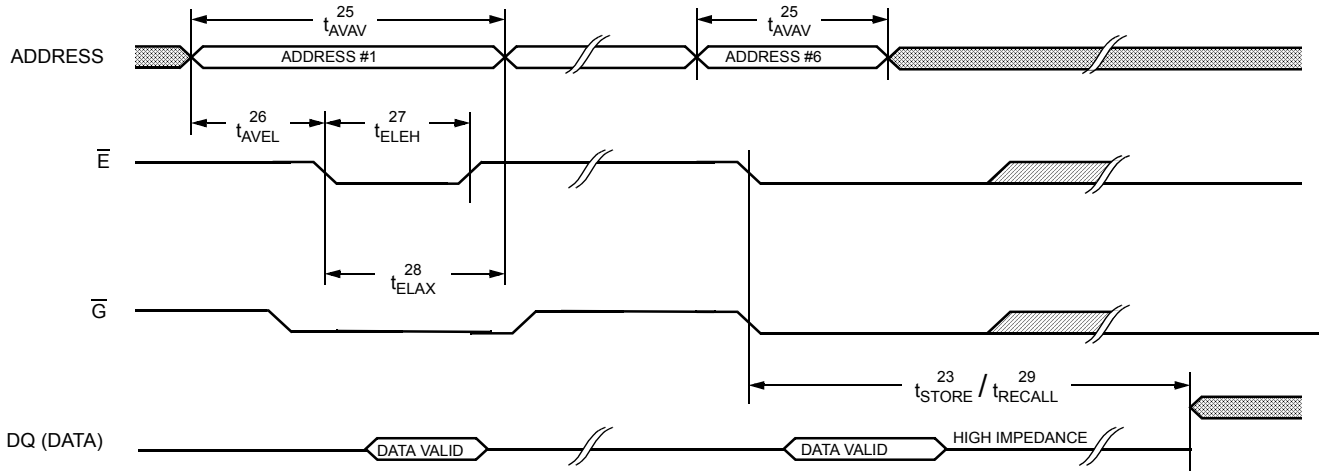


SOFTWARE-CONTROLLED *STORE*/*RECALL* CYCLE[p] (V_{CC} = 3.0V +20%, -10%)

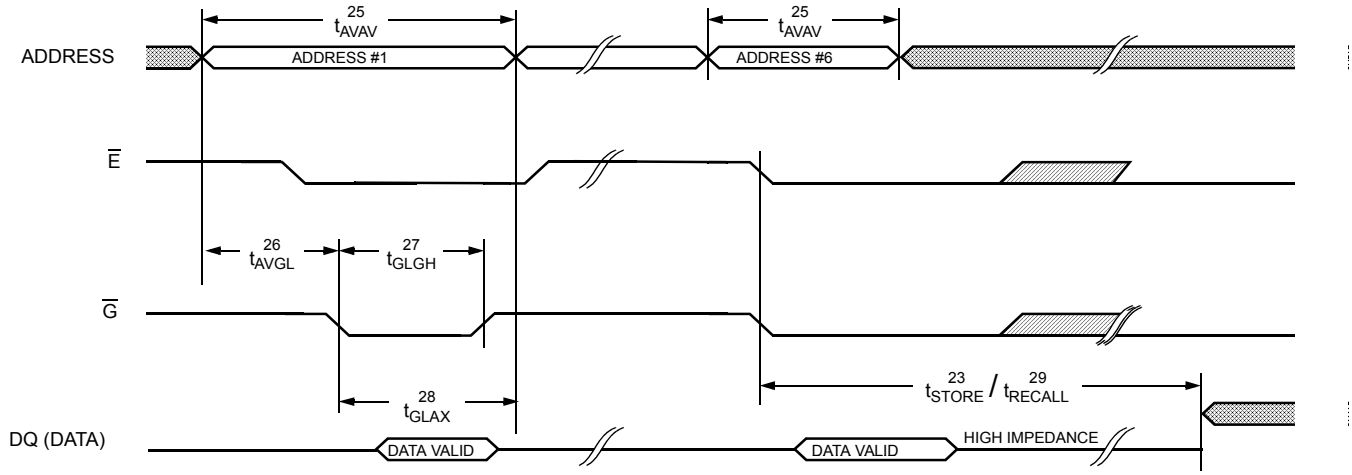
NO.	SYMBOLS			PARAMETER	STK16CA8-25		STK16CA8-35		STK16CA8-45		UNITS	NOTES
	$\overline{E}$ cont	$\overline{G}$ cont	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
25	t_{AVAV}	t_{AVAV}	t_{RC}	*STORE*/*RECALL* Initiation Cycle Time	25		35		45		ns	q
26	t_{AVEL}	t_{AVGL}	t_{AS}	Address Set-up Time	0		0		0		ns	
27	t_{ELEH}	t_{GLGH}	t_{CW}	Clock Pulse Width	20		25		30		ns	
28	t_{ELAX}	t_{GLAX}		Address Hold Time	20		20		20		ns	
29	t_{RECALL}	t_{RECALL}		*RECALL* Duration		20		20		20	µs	

Note p: The software sequence is clocked with $\overline{E}$ controlled READs or $\overline{G}$ controlled READs.
Note q: The six consecutive addresses must be in the order listed in the Mode Selection Table: (4E38, B1C7, 83E0, 7C1F, 703F, 8FC0) for a *STORE* cycle or (4E38, B1C7, 83E0, 7C1F, 703F, 4C63) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE*/*RECALL* CYCLE: $\overline{E}$ CONTROLLED[q]



SOFTWARE *STORE*/*RECALL* CYCLE: $\overline{G}$ CONTROLLED[q]



DEVICE OPERATION

The STK16CA8 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to the nonvolatile elements (the *STORE* operation) or from the nonvolatile elements to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

SRAM READ

The STK16CA8 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The address specified on pins A_{0-16} determines which of the 131,072 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until new output data appears or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

AutoStorePlus™ OPERATION

The STK16CA8's automatic *STORE* on power-down is completely transparent to the system. The *AutoStore*™ initiation takes less than 500ns when power is lost (V_{CC} < V_{SWITCH}) at which point the part depends only on its internal capacitor for *STORE* completion.

In order to prevent unneeded *STORE* operations, automatic *STORE*s will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software initiated *STORE* cycles are performed regardless of whether or not a WRITE operation has taken place.

POWER-UP *RECALL*

During power up, or after any low-power condition (V_{CCX} < V_{SWITCH}), an internal *RECALL* request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK16CA8 is in a WRITE state at the end of power-up *RECALL*, the WRITE will be inhibited and $\overline{E}$ or $\overline{W}$ must be brought high and then low for a write to initiate.

SOFTWARE NONVOLATILE *STORE*

The STK16CA8 software *STORE* cycle is initiated by executing sequential $\overline{E}$ controlled READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	8FC0 (hex)	Initiate *STORE* cycle

The software sequence must be clocked with $\overline{E}$ controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, and it is necessary that $\overline{G}$ be low for the sequence to be

valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE *RECALL*

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of $\overline{E}$ controlled READ operations must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	4C63 (hex)	Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

HARDWARE PROTECT

The STK16CA8 offers hardware protection against inadvertent *STORE* operation and SRAM WRITEs during low-voltage conditions. When $V_{CCX} < V_{SWITCH}$, all externally initiated *STORE* operations and SRAM WRITEs will be inhibited.

PREVENTING STORES

The *AutoStore*™ function can be disabled on the fly by initiating an *AutoStore Inhibit* sequence. A sequence of read operations is performed in a manner similar to the software *STORE* initiation. To initiate the *AutoStore Inihibit* sequence, the following sequence of $\overline{E}$ controlled read operations must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	8B45 (hex)	*AutoStore Inhibit*

Once the *AutoStore*™ inhibit has been initiated, it will remain active until an *AutoStore*™ inhibit off sequence has been performed, regardless of device power cycles.

The *AutoStore Inhibit* can be disabled by initiating an *AutoStore Inhibit Off* sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the *AutoStore Inhibit Off* sequence, the following sequence of E controlled read operations must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	4B46 (hex)	*AutoStore Inhibit Off*

LOW AVERAGE ACTIVE POWER

The STK16CA8 draws significantly less current when it is cycled at times longer than 50ns. Figure 3 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 3.6V, 100% duty cycle on chip enable). Figure 4 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK16CA8 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{CC} level; and 7) I/O loading.

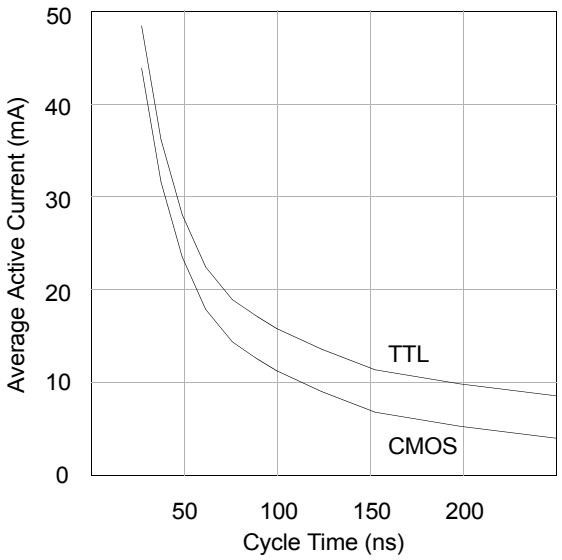


Figure 3: I_{CC} (max) Reads

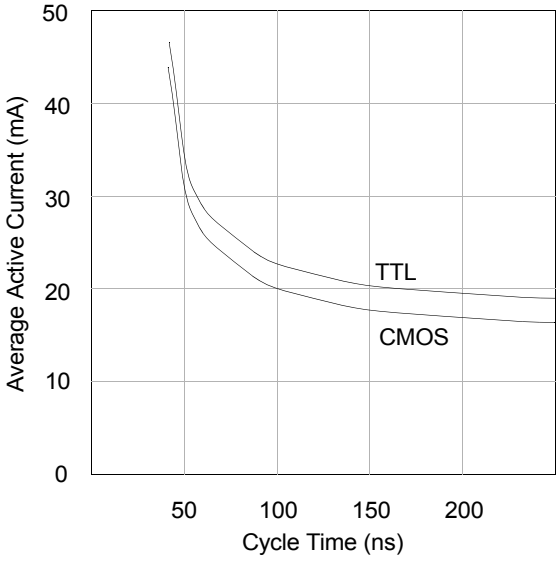
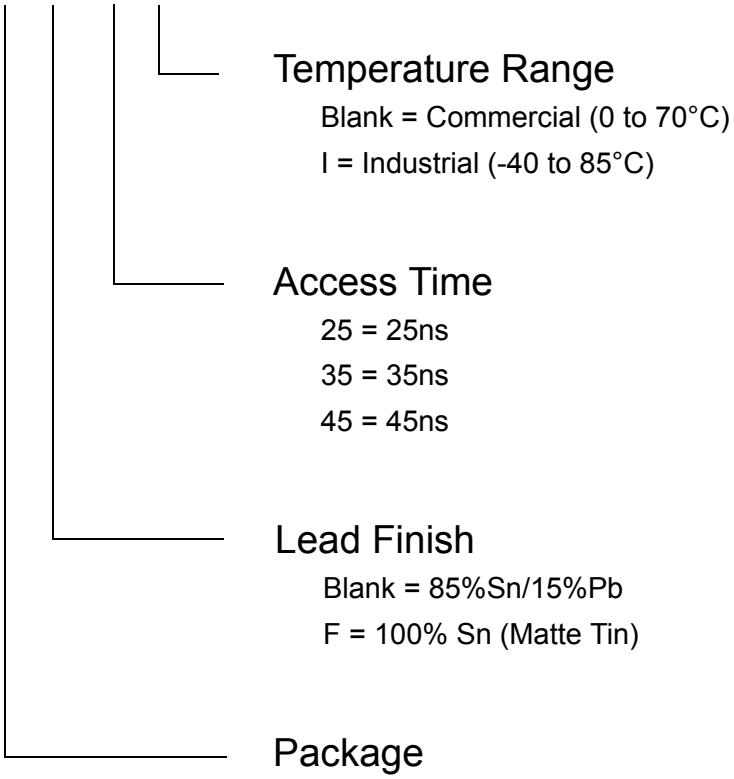


Figure 4: I_{CC} (max) Writes

ORDERING INFORMATION

STK16CA8 - W F 45 I



Temperature Range

Blank = Commercial (0 to 70°C)

I = Industrial (-40 to 85°C)

Access Time

25 = 25ns

35 = 35ns

45 = 45ns

Lead Finish

Blank = 85%Sn/15%Pb

F = 100% Sn (Matte Tin)

Package

W = Plastic 32-pin 600 mil DIP

Document Revision History

Revision	Date	Summary
0.0	May 2003	Publish new datasheet
0.1	September 2003	Added lead-free lead finish