CMOS SERIAL E^2PROM S-93A86A

The S-93A86A is a high-temperature operation, high speed, low current consumption, 16 K-bit serial E^2PROM with a wide operating voltage range. It is organized as 1024-word × 16-bit. It is capable of sequential read, at which time addresses are automatically incremented in 16-bit blocks. The instruction code is compatible with the NM93CS86.

■ Features

- Low current consumption — Standby: 3.0 μA Max. (V_{CC} = 5.5 V)
  Operating: 1.0 mA Max. (V_{CC} = 5.5 V)
  0.6 mA Max. (V_{CC} = 2.7 V)
- Wide operating voltage range — Read: 2.7 to 5.5 V
  Write: 2.7 to 5.5 V
- Sequential read capable
- Write disable function when power supply voltage is low
- Function to protect against write due to erroneous instruction recognition
- CMOS schmitt input (CS, SK)
- Endurance: 10^6 cycles/word* (at +85°C)
  1.5×10^5 cycles/word* (at +125°C)
  * For each address (Word: 16 bits)
- Data retention: 15 years (after rewriting 1.5×10^5 cycles/word at +125°C)
- High-temperature operation: +125°C Max.
- Lead-free products

■ Packages

Package name	Drawing code		
	Package	Tape	Reel
8-Pin SOP (JEDEC)	FJ008-A	FJ008-D	FJ008-D

Caution Before using the product in medical equipment or automobile equipment including car audios, keyless entries and engine control units, contact to SII is indispensable.

■ Pin Assignment

8-Pin SOP (JEDEC)
Top view

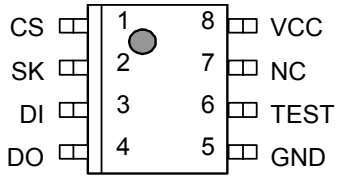


Figure 1

S-93A86AD0A-J8T2GB (Dynamic burn-in)

S-93A86AD0A-J8T2GD (Wafer burn-in)

Table 1

Pin No.	Pin name	Pin description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or VCC.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

Remark Refer to the "**Package drawings**" for the details.

■ Block Diagram

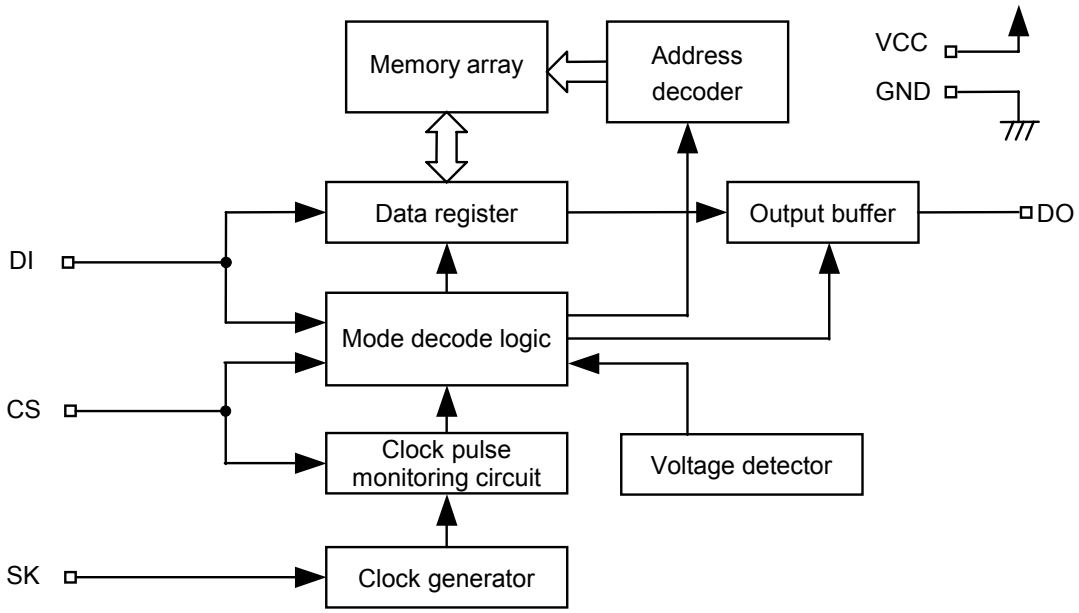


Figure 2

■ Instruction Sets

Table 2

Instruction	Start Bit	Operation Code		Address										Data
SK input clock	1	2	3	4	5	6	7	8	9	10	11	12	13	14 to 29
READ (Read data)	1	1	0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Output*1
WRITE (Write data)	1	0	1	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Input
ERASE (Erase data)	1	1	1	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—
WRAL (Write all)	1	0	0	0	1	x	x	x	x	x	x	x	x	D15 to D0 Input
ERAL (Erase all)	1	0	0	1	0	x	x	x	x	x	x	x	x	—
EWEN (Write enable)	1	0	0	1	1	x	x	x	x	x	x	x	x	—
EWDS (Write disable)	1	0	0	0	0	x	x	x	x	x	x	x	x	—

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

Remark x: Doesn't matter

■ Absolute Maximum Ratings

Table 3

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}	V
Operating ambient temperature	T_{opr}	−40 to +125	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 4

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	READ/EWDS	2.7	—	5.5	V
		WRITE/ERASE/ WRAL/ERAL/EWEN	2.7	—	5.5	V
High level input voltage	V_{IH}	—	0.8 × V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}	—	0.0	—	0.2 × V_{CC}	V

■ Pin Capacitance

Table 5

(Ta = 25°C, f = 1.0 MHz, V_{CC} = 5.0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	—	—	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	—	—	10	pF

■ Endurance

Table 6

Item	Symbol	Operating temperature	Min.	Typ.	Max.	Unit
Endurance	N_W	−40 to +125°C	1.5×10^5	—	—	cycles/word*1

***1.** For each address (Word: 16 bits)

■ DC Electrical Characteristics

Table 7

Item	Symbol	Condition	V_{CC} = 4.5 to 5.5 V			V_{CC} = 2.7 to 4.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	DO no load	—	—	1.0	—	—	0.6	mA

Table 8

Item	Symbol	Condition	V_{CC} = 4.5 to 5.5 V			V_{CC} = 2.7 to 4.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (WRITE)	I_{CC2}	DO no load	—	—	2.0	—	—	1.5	mA

Table 9

Item	Symbol	Condition	V_{CC} = 4.5 to 5.5 V			V_{CC} = 2.7 to 4.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	CS = GND, DO = Open, Other inputs to V_{CC} or GND	—	—	3.0	—	—	3.0	µA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	0.1	2.0	—	0.1	2.0	µA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	0.1	2.0	—	0.1	2.0	µA
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	—	—	0.6	—	—	—	V
		I_{OL} = 100 µA	—	—	0.2	—	—	0.2	V
High level output voltage	V_{OH}	I_{OH} = −400 µA	2.4	—	—	—	—	—	V
		I_{OH} = −100 µA	V_{CC}− 0.3	—	—	V_{CC}− 0.3	—	—	V
		I_{OH} = −10 µA	V_{CC}− 0.2	—	—	V_{CC}− 0.2	—	—	V
Write enable latch data hold voltage	V_{DH}	Only when write disable mode	1.5	—	—	1.5	—	—	V

■ AC Electrical Characteristics

Table 10 Test Conditions

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100 pF

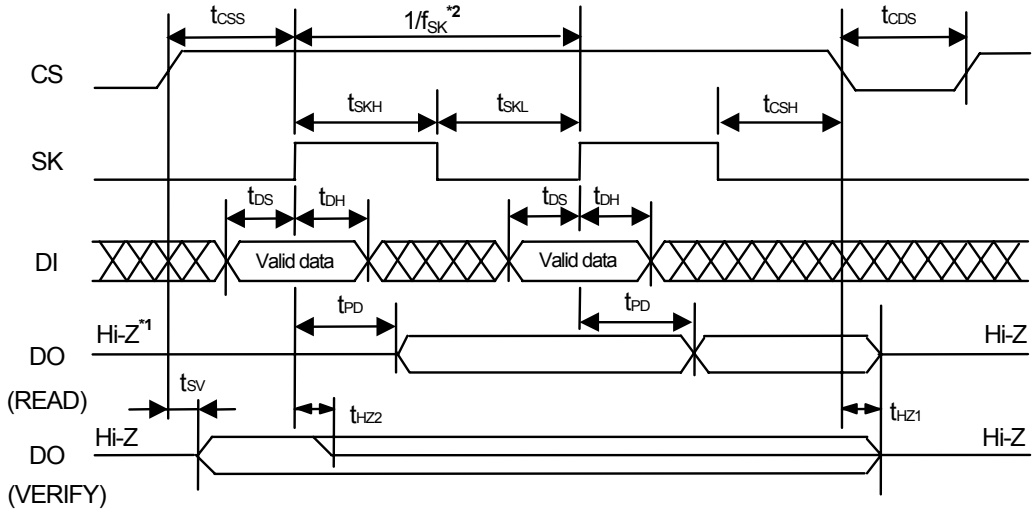
Table 11

Item	Symbol	V_{CC} = 4.5 to 5.5 V			V_{CC} = 2.7 to 4.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
CS setup time	t_{CSS}	0.2	—	—	0.4	—	—	µs
CS hold time	t_{CSH}	0	—	—	0	—	—	µs
CS deselect time	t_{CDS}	0.2	—	—	0.2	—	—	µs
Data setup time	t_{DS}	0.1	—	—	0.2	—	—	µs
Data hold time	t_{DH}	0.1	—	—	0.2	—	—	µs
Output delay time	t_{PD}	—	—	0.4	—	—	1.2	µs
Clock frequency*1	f_{SK}	0	—	2.0	0	—	0.5	MHz
Clock pulse width	t_{SKH}, t_{SKL}	0.1	—	—	0.5	—	—	µs
Output disable time	t_{HZ1}, t_{HZ2}	0	—	0.2	0	—	0.5	µs
Output enable time	t_{SV}	0	—	0.15	0	—	0.5	µs

***1.** The clock cycle of the SK clock (frequency: f_{SK}) is $1/f_{SK}$ µs. This clock cycle is determined by a combination of several AC characteristics, so be aware that even if the SK clock cycle time is minimized, the clock cycle ($1/f_{SK}$) cannot be made to equal t_{SKL}(Min.) + t_{SKH}(Min.).

Table 12

Item	Symbol	V_{CC} = 2.7 to 5.5 V			Unit
		Min.	Typ.	Max.	
Write time	t_{PR}	—	2.0	5.0	ms



***1.** Indicates high impedance.
***2.** $1/f_{SK}$ is the SK clock cycle. This clock cycle is determined by a combination of several AC characteristics, so be aware that even if the SK clock cycle time is minimized, the clock cycle ($1/f_{SK}$) cannot be made to equal t_{SKL}(Min.) + t_{SKH}(Min.).

Figure 3 Timing Chart

■ Operation

All instructions are executed by inputting DI in synchronization with the rising edge of SK after CS goes high. An instruction set is input in the order of start bit, instruction, address, and data.
Instruction input finishes when CS goes low. A low level must be input to CS between commands during t_{CDS}. While a low level is being input to CS, the S-93A86A is in standby mode, so the SK and DI inputs are invalid and no instructions are allowed.

■ Start Bit

A start bit is recognized when the DI pin goes high at the rise of SK after CS goes high. After CS goes high, a start bit is not recognized even if the SK pulse is input as long as the DI pin is low.

1. Dummy Clock

SK clocks input while the DI pin is low before a start bit is input are called dummy clocks. Dummy clocks are effective when aligning the number of instruction sets (clocks) sent by the CPU with those required for serial memory operation. For example, when the CPU instruction set is 16 bits, the number of instruction set clocks can be adjusted by inserting the 3-bit dummy clock in S-93A86A.

2. Start Bit input Failure

- When the output status of the DO pin is high during the verify period after a write operation, if a high level is input to the DI pin at the rising edge of SK, the S-93A86A recognizes that a start bit has been input. To prevent this failure, input a low level to the DI pin during the verify operation period (Refer to "**4.1 Verify Operation**").

- When a 3-wire interface is configured by connecting the DI input pin and DO output pin, a period in which the data output from the CPU and the serial memory collide may be generated, preventing successful input of the start bit. Take the measures described in "**■ 3-Wire Interface (Direct Connection between DI and DO)**".

3. Reading (READ)

The READ instruction reads data from a specified address.
After CS has gone high, input an instruction in the order of the start bit, read instruction, and address. Since the last input address (A_0) has been latched, the output status of the DO pin changes from high impedance (Hi-Z) to low, which is held until the next rise of SK. 16-bit data starts to be output in synchronization with the next rise of SK.

3.1 Sequential Read

After the 16-bit data at the specified address has been output, inputting SK while CS is high automatically increments the address, and causes the 16-bit data at the next address to be output sequentially. The above method makes it possible to read the data in the whole memory space. The last address (A_n ••• A_1 A_0 = 1 ••• 1 1) rolls over to the top address (A_n ••• A_1 A_0 = 0 ••• 0 0).

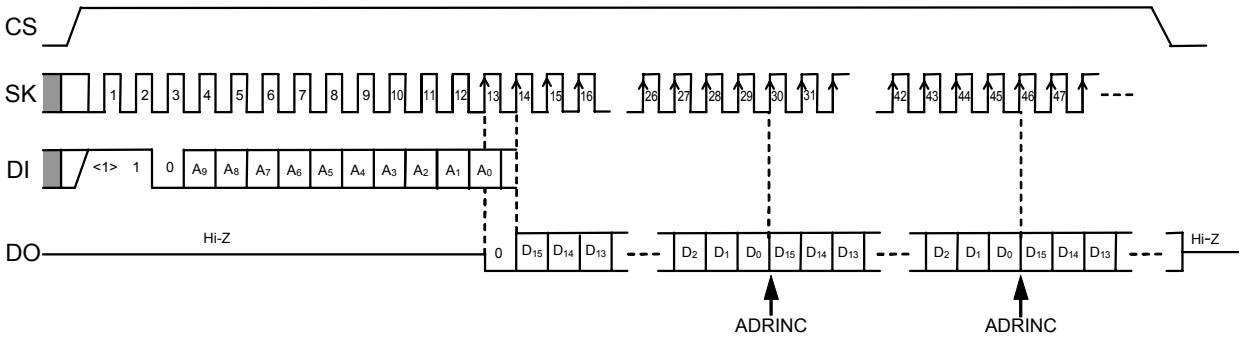


Figure 4 Read Timing

4. Writing (WRITE, ERASE, WRAL, ERAL)

A write operation includes four write instructions: data write (WRITE), data erase (ERASE), chip write (WRAL), and chip erase (ERAL).
A write instruction (WRITE, ERASE, WRAL, ERAL) starts a write operation to the memory cell when a low level is input to CS after a specified number of clocks have been input. The SK and DI inputs are invalid during the write period, so do not input an instruction.
Input an instruction while the output status of the DO pin is high or high impedance (Hi-Z).
A write operation is valid only in program enable mode (refer to "**5. Write Enable (EWEN) and Write Disable (EWDS)**").

4.1 Verify Operation

A write operation executed by any instruction is completed within 5 ms (write time t_{PR}: typically 2 ms), so if the completion of the write operation is recognized, the write cycle can be minimized. A sequential operation to confirm the status of a write operation is called a verify operation.

(1) Operation

After the write operation has started (CS = low), the status of the write operation can be verified by confirming the output status of the DO pin by inputting a high level to CS again. This sequence is called a verify operation, and the period that a high level is input to the CS pin after the write operation has started is called the verify operation period.
The relationship between the output status of the DO pin and the write operation during the verify operation period is as follows.

- DO pin = low: Writing in progress (busy)
- DO pin = high: Writing completed (ready)

(2) Operation Example

There are two methods to perform a verify operation: Waiting for a change in the output status of the DO pin while keeping CS high, or suspending the verify operation (CS = low) once and then performing it again to verify the output status of the DO pin. The latter method allows the CPU to perform other processing during the wait period, allowing an efficient system to be designed.

Caution 1. Input a low level to the DI pin during a verify operation.
2. If a high level is input to the DI pin at the rise of SK when the output status of the DO pin is high, the S-93A86A latches the instruction assuming that a start bit has been input. In this case, note that the DO pin immediately enters a high-impedance (Hi-Z) state.

4.2 Writing Data (WRITE)

To write 16-bit data to a specified address, change CS to high and then input the WRITE instruction, address, and 16-bit data following the start bit. The write operation starts when CS goes low. There is no need to set the data to 1 before writing. When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the WRITE instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

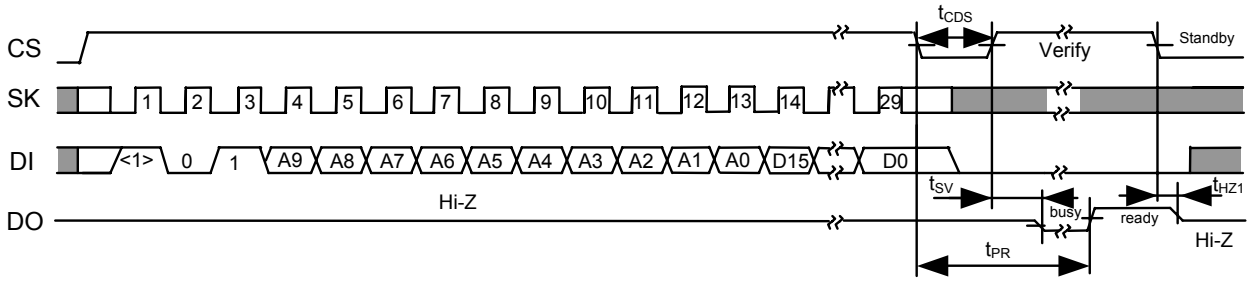


Figure 5 Data Write Timing

4.3 Erasing Data (ERASE)

To erase 16-bit data at a specified address, set all 16 bits of the data to 1, change CS to high, and then input the ERASE instruction and address following the start bit. There is no need to input data. The data erase operation starts when CS goes low. When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the ERASE instruction. For details of the clock pulse monitoring circuit, refer to **"■ Function to Protect Against Write due to Erroneous Instruction Recognition**".

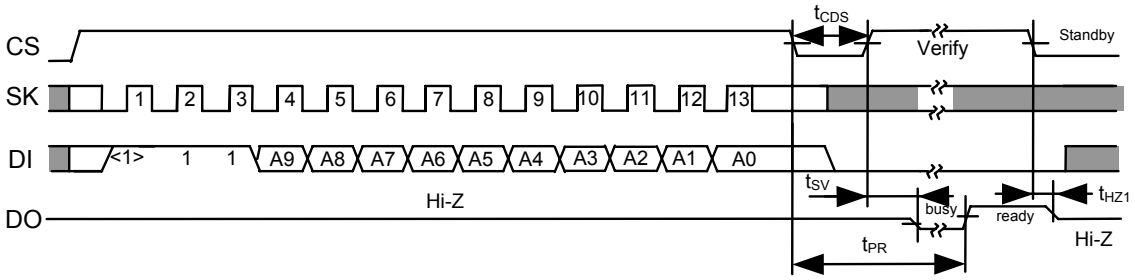


Figure 6 Data Erase Timing

4.4 Writing to Chip (WRAL)

To write the same 16-bit data to the entire memory address space, change CS to high, and then input the WRAL instruction, an address, and 16-bit data following the start bit. Any address can be input. The write operation starts when CS goes low. There is no need to set the data to 1 before writing. When the clocks more than the specified number been input, the clock pulse monitoring circuit cancels the WRAL instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

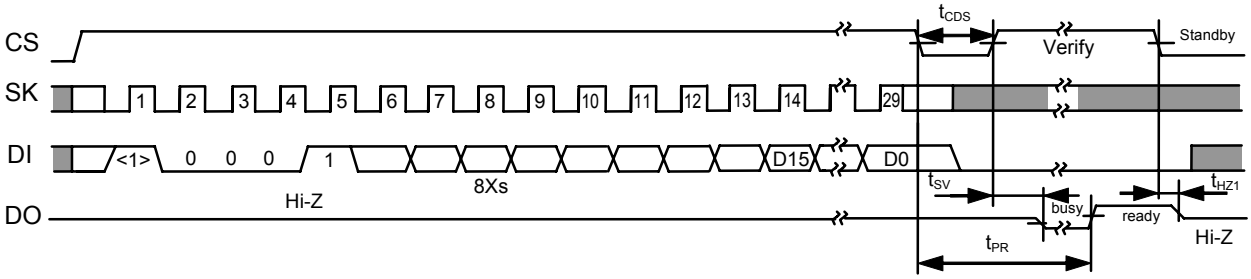


Figure 7 Chip Write Timing

4.5 Erasing Chip (ERAL)

To erase the data of the entire memory address space, set all the data to 1, change CS to high, and then input the ERAL instruction and an address following the start bit. Any address can be input. There is no need to input data. The chips erase operation starts when CS goes low. When the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the ERAL instruction. For details of the clock pulse monitoring circuit, refer to **"■ Function to Protect Against Write due to Erroneous Instruction Recognition**".

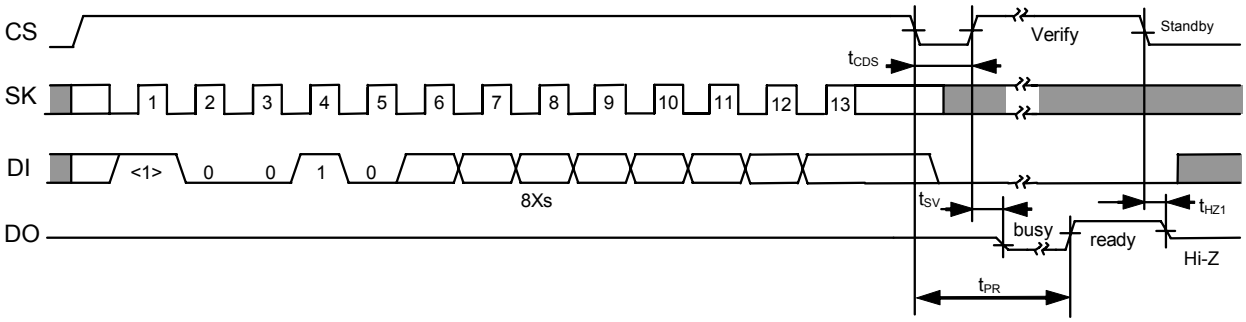


Figure 8 Chip Erase Timing

5. Write Enable (EWEN) and Write Disable (EWDS)

The EWEN instruction is an instruction that enables a write operation. The status in which a write operation is enabled is called the program enable mode.
The EWDS instruction is an instruction that disables a write operation. The status in which a write operation is disabled is called the program disable mode.
After CS goes high, input an instruction in the order of the start bit, EWEN or EWDS instruction, and address (optional). Each mode becomes valid by inputting a low level to CS after the last address (optional) has been input.

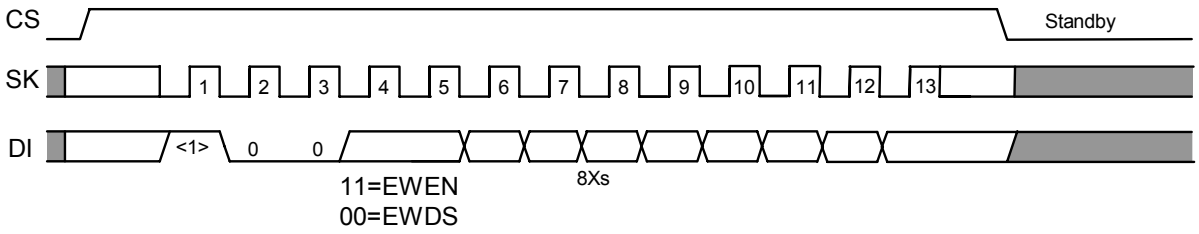


Figure 9 Write Enable/Disable Timing

(1) Recommendation for write operation disable instruction

It is recommended to implement a design that prevents an incorrect write operation when a write instruction is erroneously recognized by executing the write operation disable instruction when executing instructions other than write instruction, and immediately after power-on and before power off.

■ Write Disable Function when Power Supply Voltage is Low

The S-93A86A provides a built-in detector to detect a low power supply voltage and disable writing. When the power supply voltage is low or at power application, the write instructions (WRITE, ERASE, WRAL, and ERAL) are cancelled, and the write disable state (EWDS) is automatically set. The detection voltage is 1.20 V typ., the release voltage is 1.35 V typ., and there is a hysteresis of about 0.15 V (Refer to **Figure 10**). Therefore, when a write operation is performed after the power supply voltage has dropped and then risen again up to the level at which writing is possible, a write enable instruction (EWEN) must be sent before a write instruction (WRITE, ERASE, WRAL, or ERAL) is executed.
When the power supply voltage drops during a write operation, the data being written to an address at that time is not guaranteed.

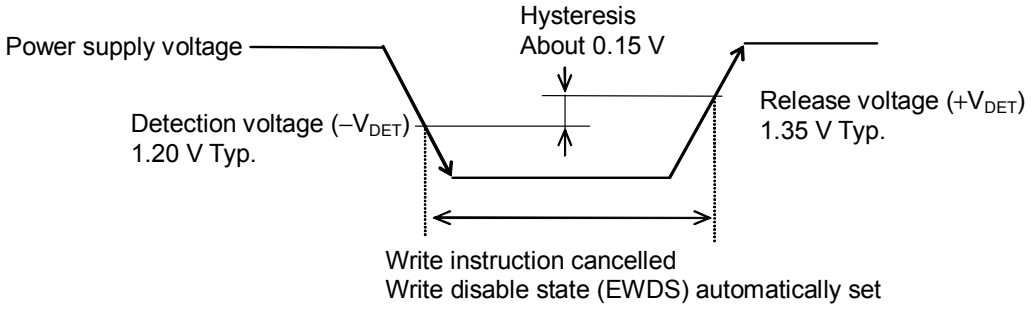
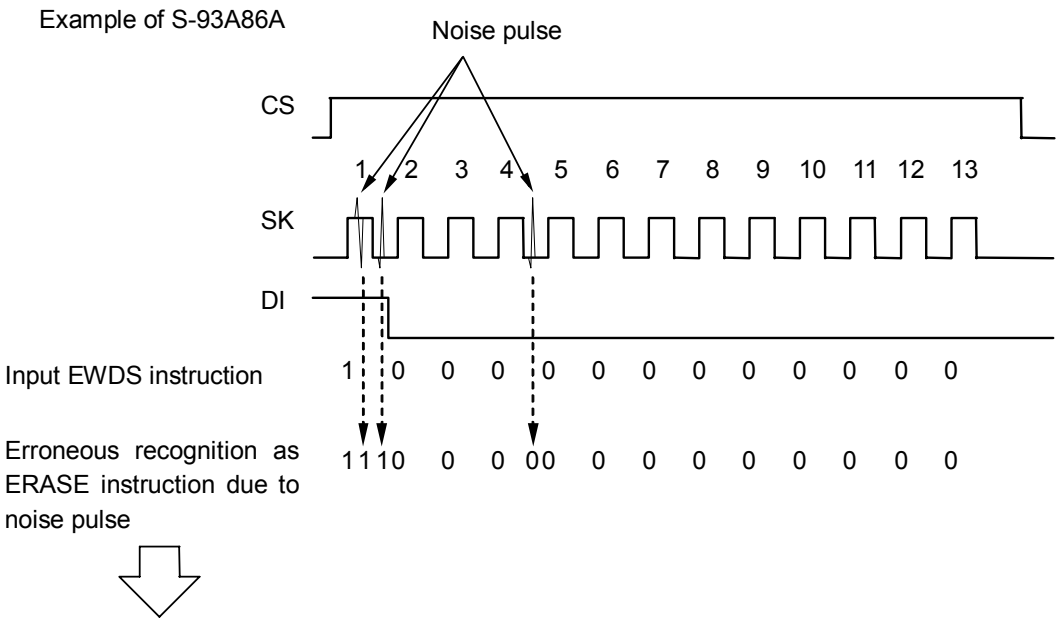


Figure 10 Operation when Power Supply Voltage is Low

■ Function to Protect Against Write due to Erroneous Instruction Recognition

The S-93A86A provides a built-in clock pulse monitoring circuit which is used to prevent an erroneous write operation by canceling write instructions (WRITE, ERASE, WRAL, and ERAL) recognized erroneously due to an erroneous clock count caused by the application of noise pulses or double counting of clocks.
Instructions are cancelled if a clock pulse whose count other than the one specified for each write instruction (WRITE, ERASE, WRAL, or ERAL) is detected.

<Example> Erroneous Recognition of Program Disable Instruction (EWDS) as Erase Instruction (ERASE)



In products that do not incorporate a clock pulse monitoring circuit, FFFF is mistakenly written to address 00h. However the S-93A86A detects the over count and cancels the instruction without performing a write operation.

Figure 11 Example of Clock Pulse Monitoring Circuit Operation

■ 3-Wire Interface (Direct Connection between DI and DO)

There are two types of serial interface configurations: a 4-wire interface configured using the CS, SK, DI, and DO pins, and a 3-wire interface that connects the DI input pin and DO output pin.
When the 3-wire interface is employed, a period in which the data output from the CPU and the data output from the serial memory collide may occur, causing a malfunction. To prevent such a malfunction, connect the DI and DO pins of the S-93A86A via a resistor (10 kΩ to 100 kΩ) so that the data output from the CPU takes precedence in being input to the DI pin (Refer to "**Figure 12 Connection of 3-Wire Interface**").

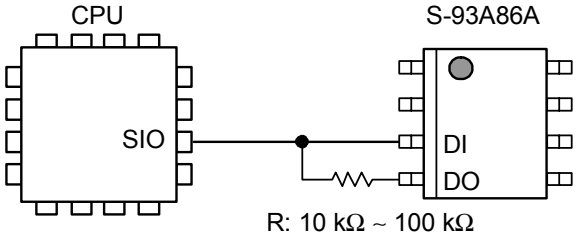


Figure 12 Connection of 3-Wire Interface

■ I/O Pins

1. Connection of Input Pins

All the input pins of the S-93A86A employ a C-MOS structure, so design the equipment so that high impedance will not be input while the S-93A86A is operating. Especially, deselect the CS input (a low level) when turning on/off power and during standby. When the CS pin is deselected (a low level), incorrect data writing will not occur. Connect the CS pin to GND via a resistor (10 kΩ to 100 kΩ pull-down resistor). To prevent malfunction, it is recommended to use equivalent pull-down resistors for pins other than the CS pin.

2. Input and Output Pin Equivalent Circuits

The following shows the equivalent circuits of input pins of the S-93A86A. None of the input pins incorporate pull-up and pull-down elements, so special care must be taken when designing to prevent a floating status.
Output pins are high-level/low-level/high-impedance tri-state outputs. The TEST pin is disconnected from the internal circuit by a switching transistor during normal operation. As long as the absolute maximum rating is satisfied, the TEST pin and internal circuit will never be connected.

2.1 Input Pin

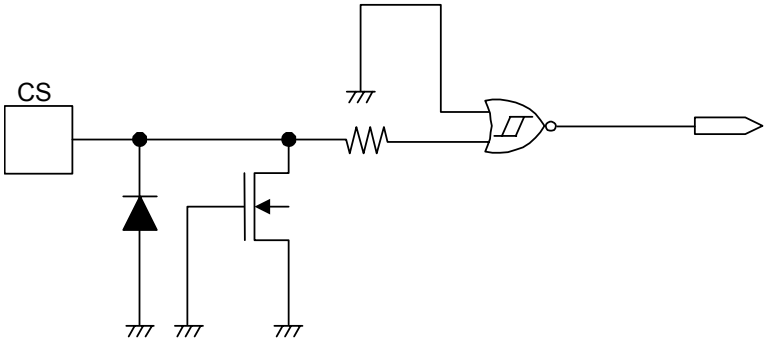


Figure 13 CS Pin

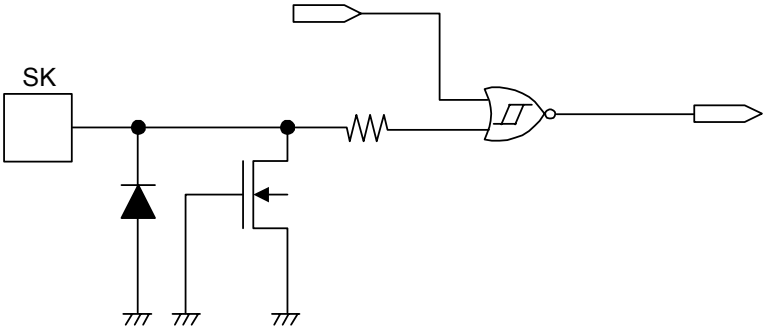


Figure 14 SK Pin

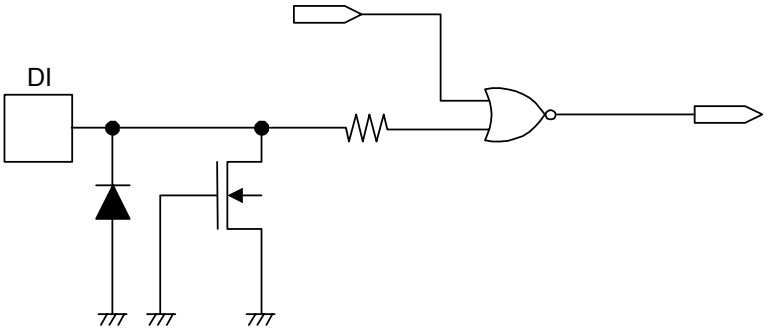


Figure 15 DI Pin

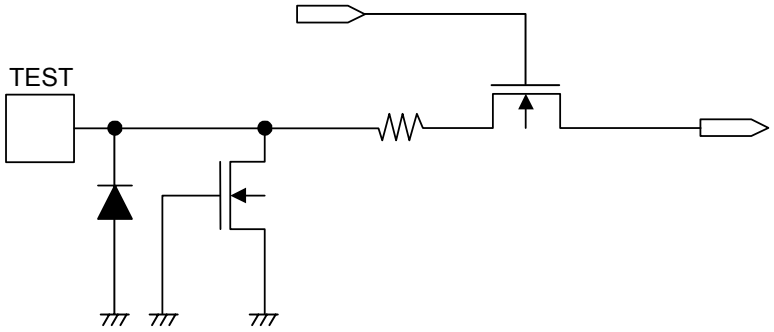


Figure 16 TEST Pin

2.2 Output Pin

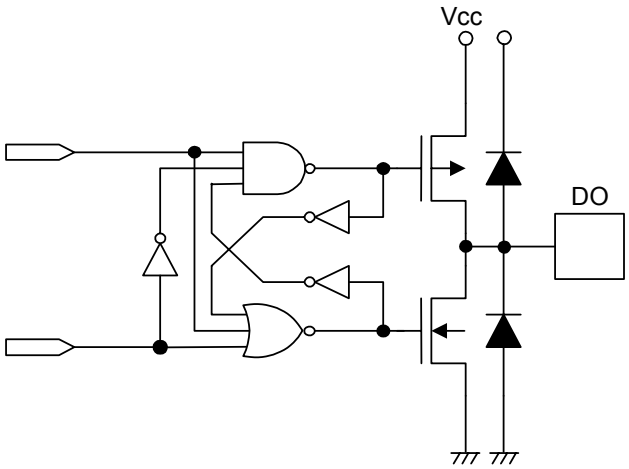


Figure 17 DO Pin

3. Input Pin Noise Elimination Time

The S-93A86A includes a built-in low-pass filter to eliminate noise at the SK, DI, and CS pins. This means that if the supply voltage is 5.0 V (at room temperature), noise with a pulse width of 20 ns or less can be eliminated.
Note, therefore, that noise with a pulse width of more than 20 ns will be recognized as a pulse if the voltage exceeds V_{IH}/V_{IL}.

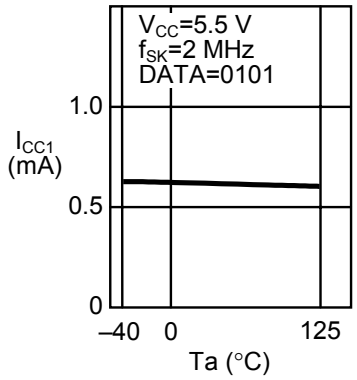
■ Precaution

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

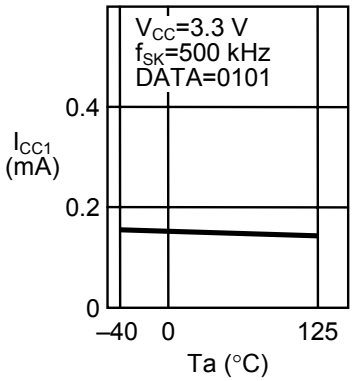
■ Characteristics

1. DC Characteristics

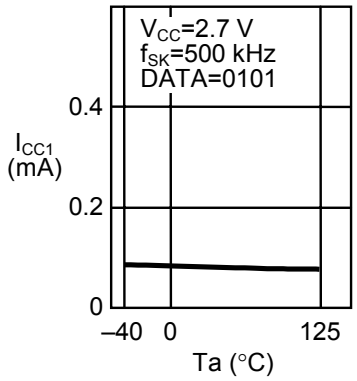
1.1 Current consumption (READ) I_{CC1} vs. ambient temperature Ta



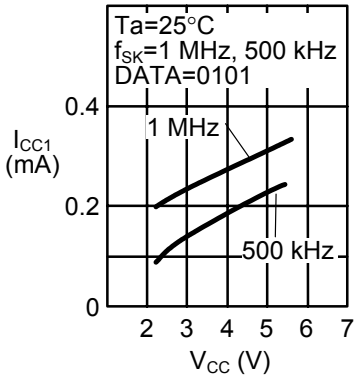
1.2 Current consumption (READ) I_{CC1} vs. ambient temperature Ta



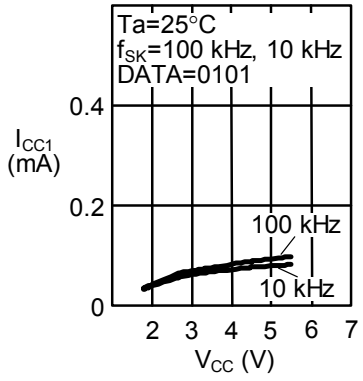
1.3 Current consumption (READ) I_{CC1} vs. ambient temperature Ta



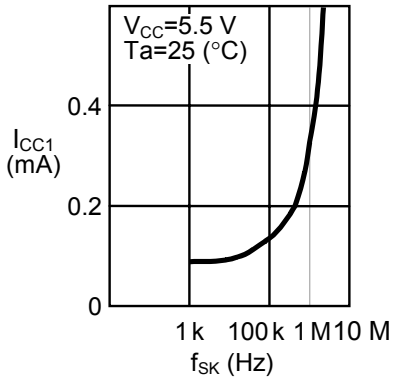
1.4 Current consumption (READ) I_{CC1} vs. power supply voltage V_{CC}



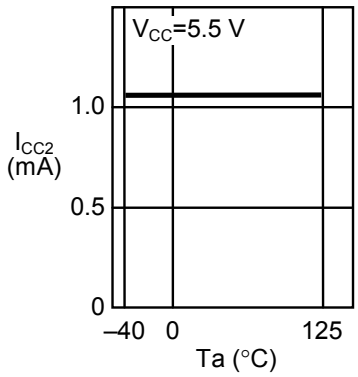
1.5 Current consumption (READ) I_{CC1} vs. power supply voltage V_{CC}



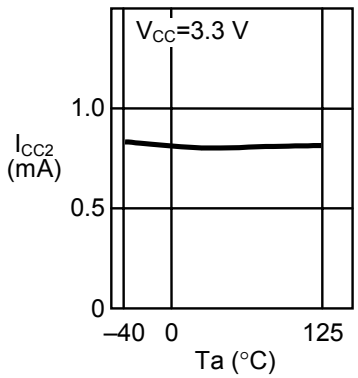
1.6 Current consumption (READ) I_{CC1} vs. Clock frequency f_{SK}



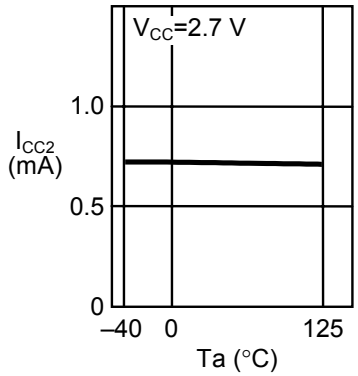
1.7 Current consumption (WRITE) I_{CC2} vs. ambient temperature Ta



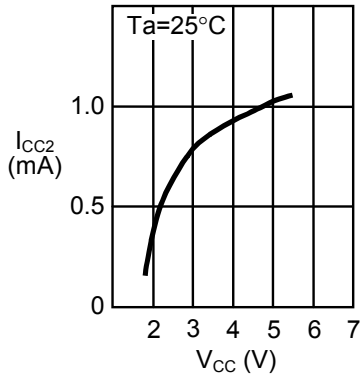
1.8 Current consumption (WRITE) I_{CC2} vs. ambient temperature Ta



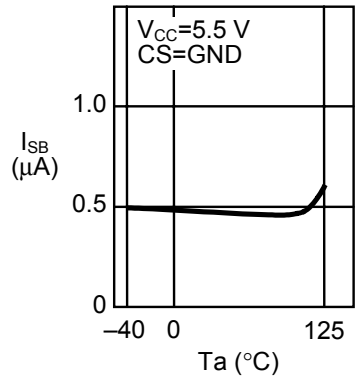
1.9 Current consumption (WRITE) I_{CC2} vs. ambient temperature Ta



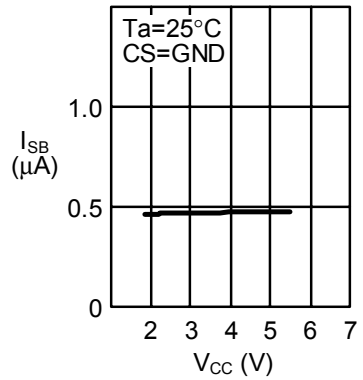
1.10 Current consumption (WRITE) I_{CC2} vs. power supply voltage V_{CC}



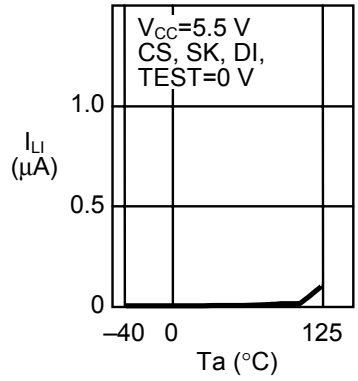
1.11 Current consumption in standby mode I_{SB} vs. ambient temperature Ta



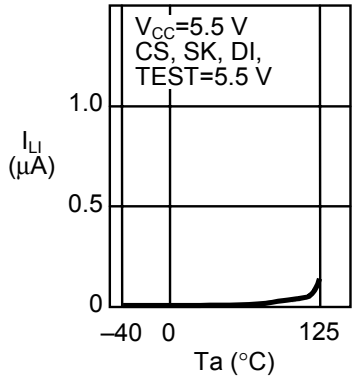
1.12 Current consumption in standby mode I_{SB} vs. power supply voltage V_{CC}



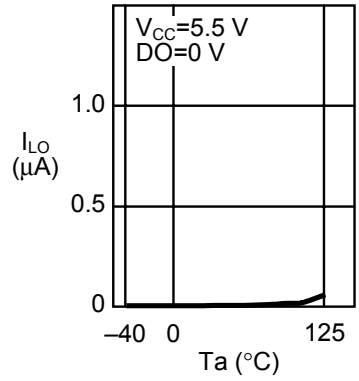
1.13 Input leakage current I_{LI} vs. ambient temperature Ta



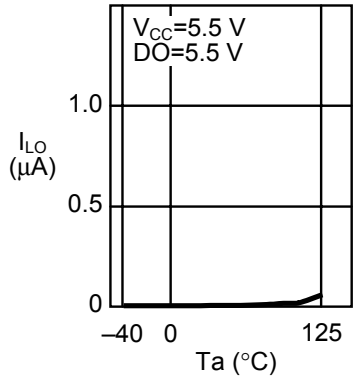
1.14 Input leakage current I_{LI} vs. ambient temperature Ta



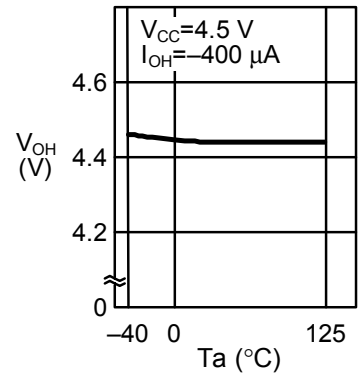
1.15 Output leakage current I_{LO} vs. ambient temperature Ta



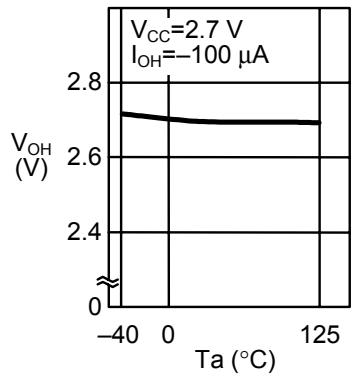
1.16 Output leakage current I_{LO} vs. ambient temperature Ta



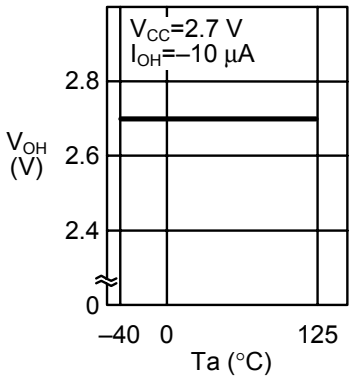
1.17 High-level output voltage V_{OH} vs. ambient temperature Ta



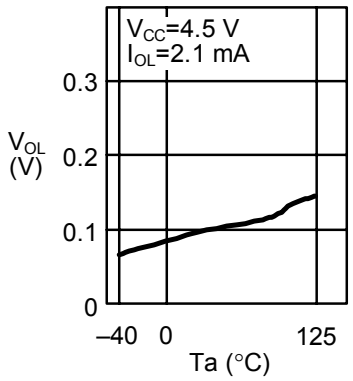
1.18 High-level output voltage V_{OH} vs. ambient temperature Ta



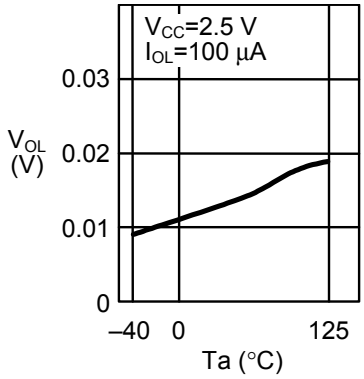
1.19 High-level output voltage V_{OH} vs. ambient temperature Ta



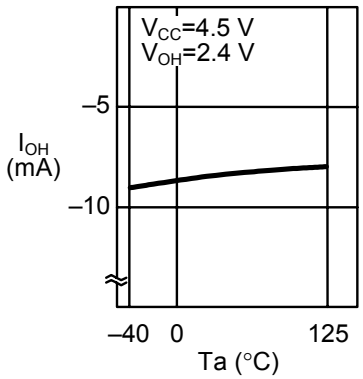
1.20 Low-level output voltage V_{OL} vs. ambient temperature Ta



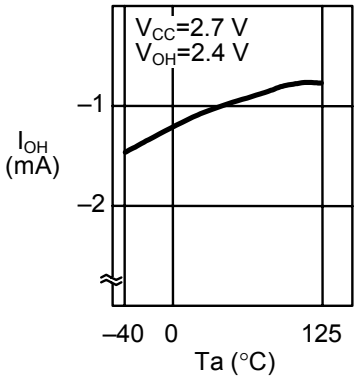
1.21 Low-level output voltage V_{OL} vs. ambient temperature Ta



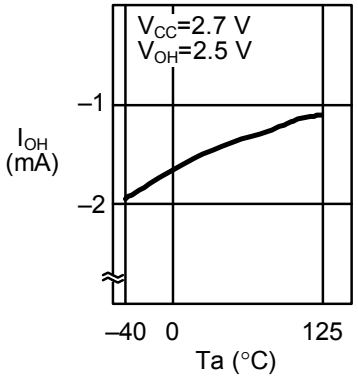
1.22 High-level output current I_{OH} vs. ambient temperature Ta



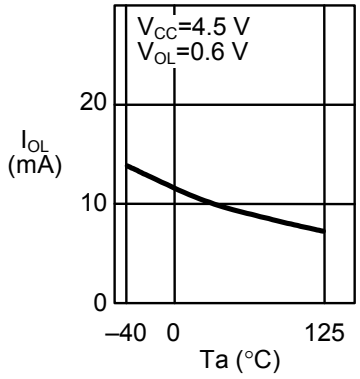
1.23 High-level output current I_{OH} vs. ambient temperature Ta



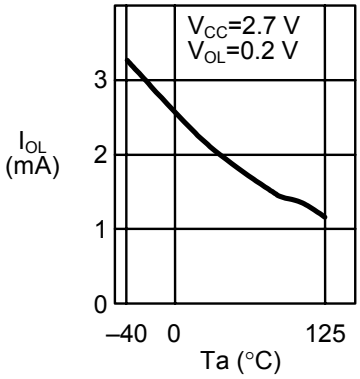
1.24 High-level output current I_{OH} vs. ambient temperature Ta



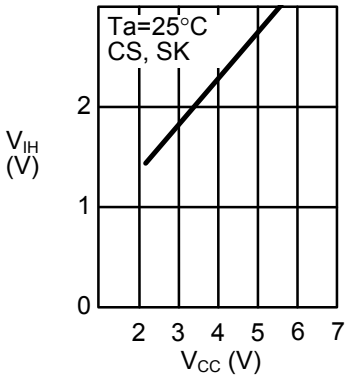
1.25 Low-level output current I_{OL} vs. ambient temperature Ta



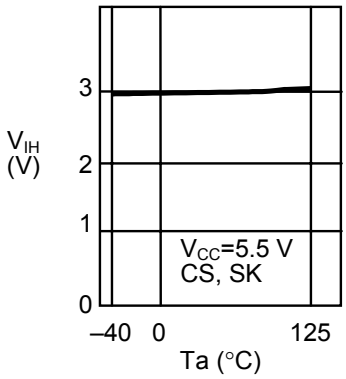
1.26 Low-level output current I_{OL} vs. ambient temperature Ta



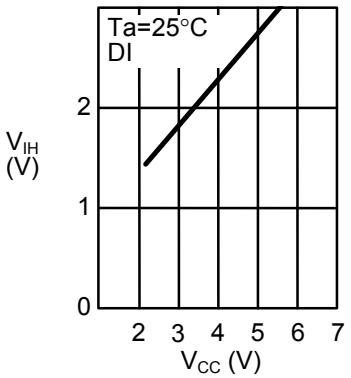
1.27 High-level input voltage V_{IH} vs. power supply voltage V_{CC}



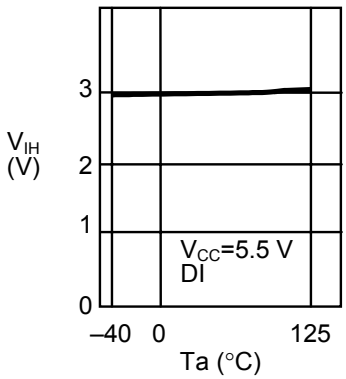
1.28 High-level input voltage V_{IH} vs. ambient temperature Ta



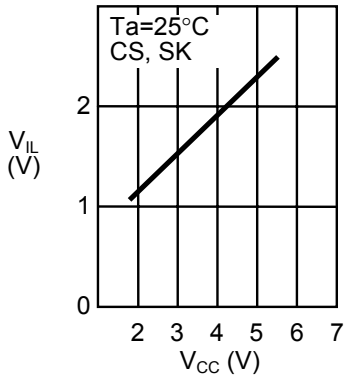
1.29 High-level input voltage V_{IH} vs. power supply voltage V_{CC}



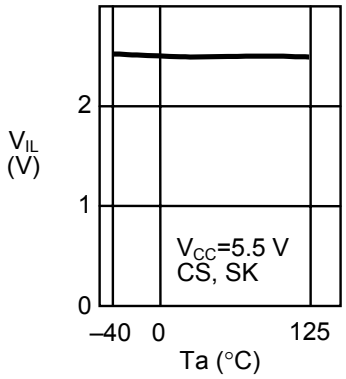
1.30 High-level input voltage V_{IH} vs. ambient temperature Ta



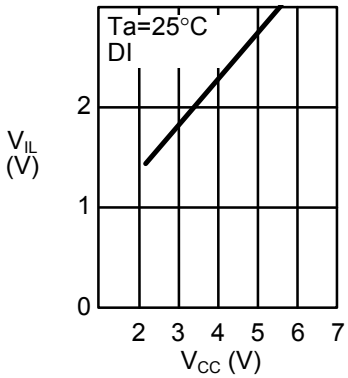
1.31 Low-level input voltage V_{IL} vs. power supply voltage V_{CC}



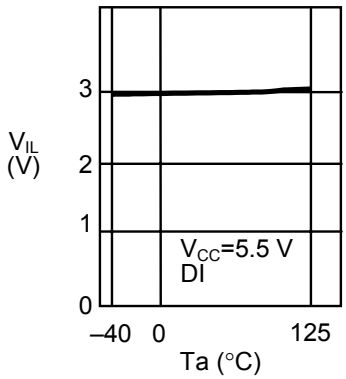
1.32 Low-level input voltage V_{IL} vs. ambient temperature Ta



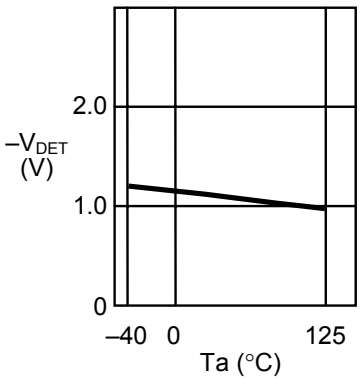
1.33 Low-level input voltage V_{IL} vs. power supply voltage V_{CC}



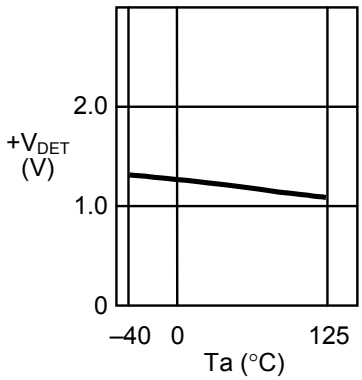
1.34 Low-level input voltage V_{IL} vs. ambient temperature Ta



1.35 Low supply voltage detection voltage $-V_{DET}$ vs. ambient temperature Ta

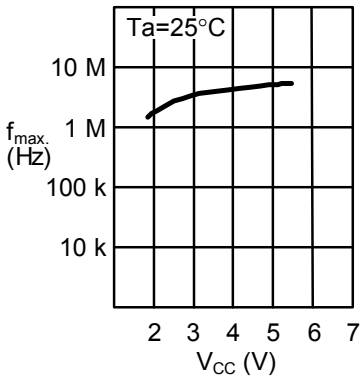


1.36 Low supply voltage release voltage $+V_{DET}$ vs. ambient temperature Ta

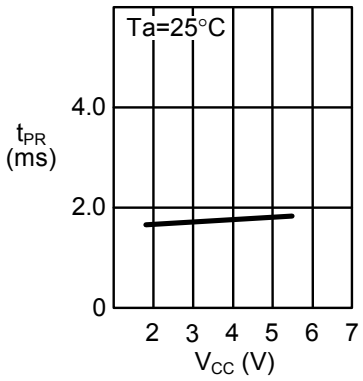


2. AC Characteristics

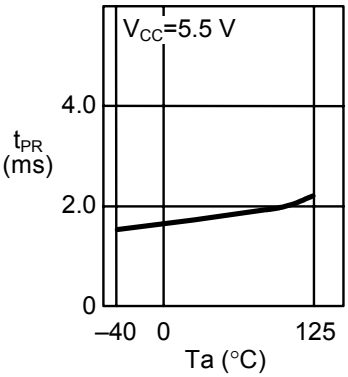
2.1 Maximum operating frequency $f_{max.}$ vs. power supply voltage V_{CC}



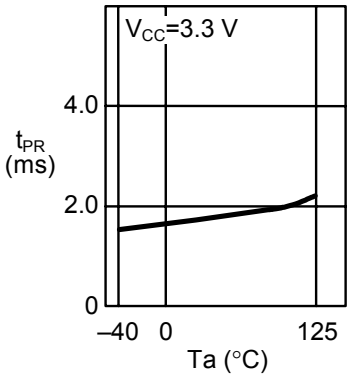
2.2 Write time t_{PR} vs. power supply voltage V_{CC}



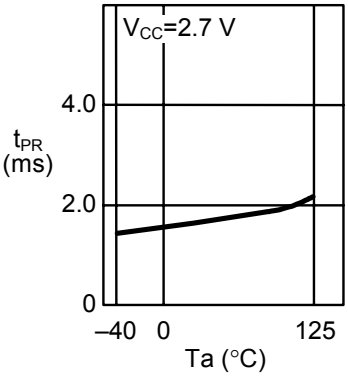
2.3 Write time t_{PR} vs. ambient temperature Ta



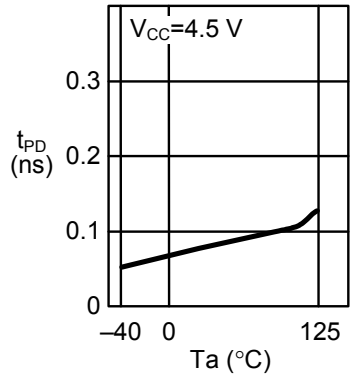
2.4 Write time t_{PR} vs. ambient temperature Ta



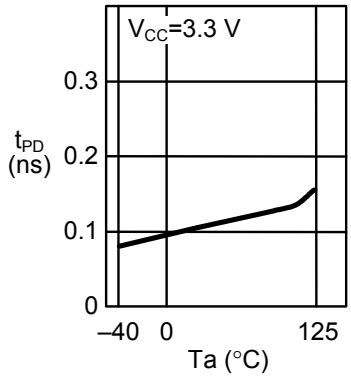
2.5 Write time t_{PR} vs. ambient temperature Ta



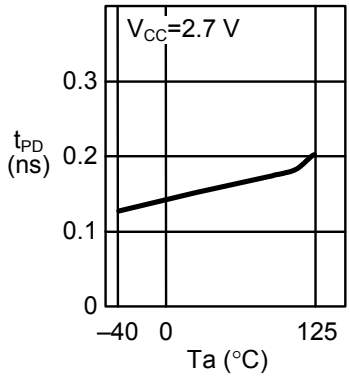
2.6 Data output delay time t_{PD} vs. ambient temperature Ta



2.7 Data output delay time t_{PD} vs. ambient temperature Ta



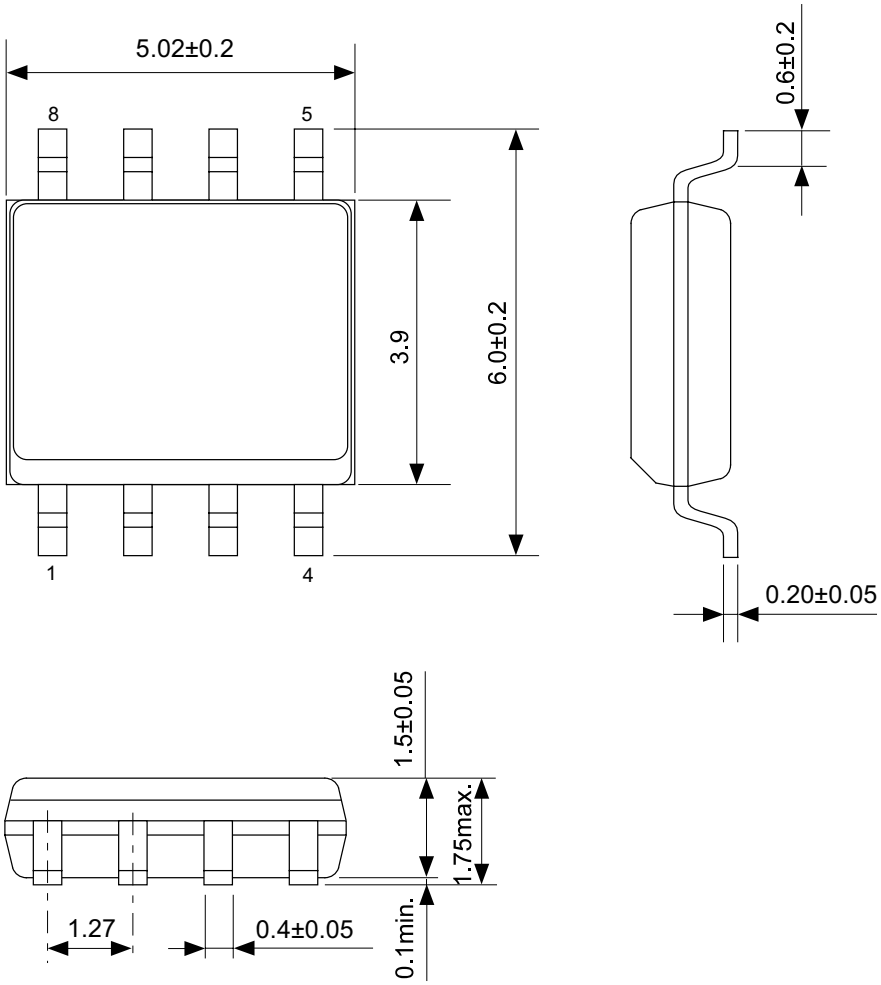
2.8 Data output delay time t_{PD} vs. ambient temperature Ta



■ Product Name Structure

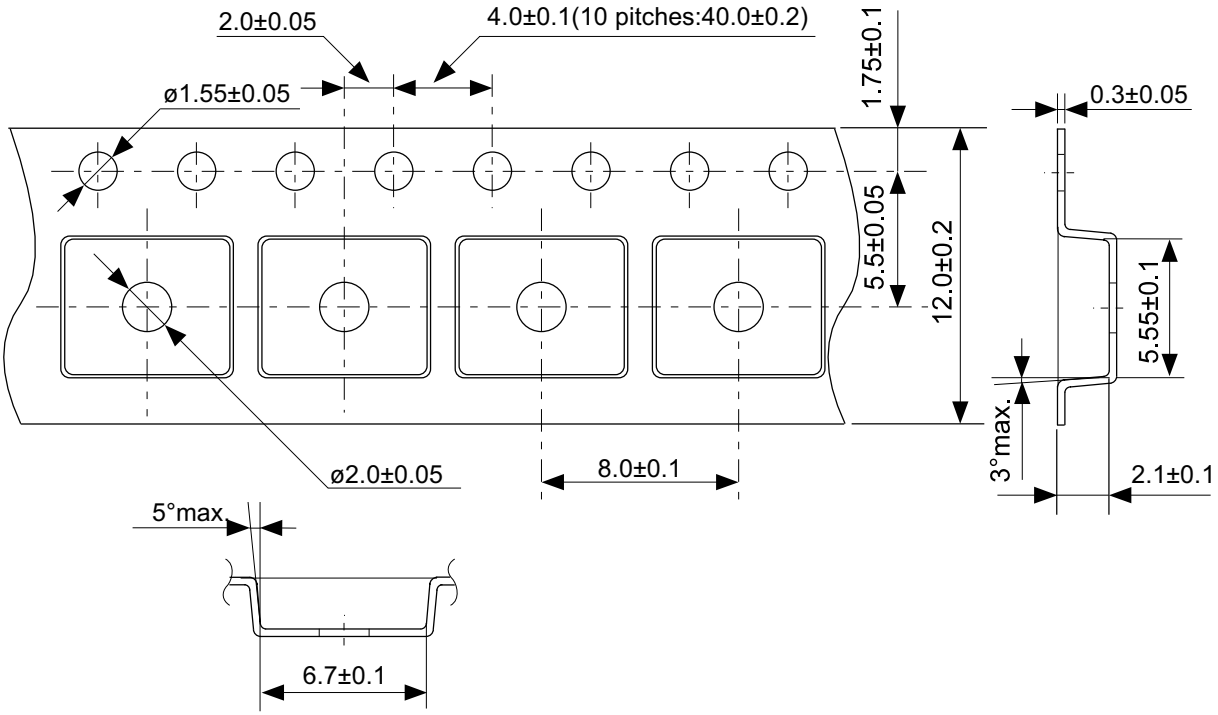
S-93A86A D 0 A – J8T2 G x

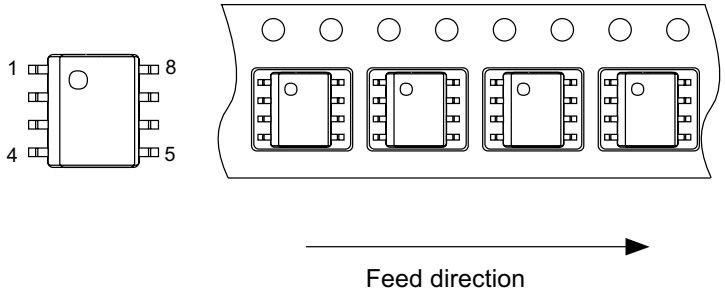
- Burn-in specification
  - B: Dynamic burn-in
  - D: Wafer burn-in
- Package code and IC packing specifications
  - J8T2: 8-Pin SOP (JEDEC), Tape
- Operation temperature
  - A: –40 ~ +125°C
- Fixed
- Pin assignment
- Product name
  - S-93A86A: 16 K-bit



No. FJ008-A-P-SD-2.1

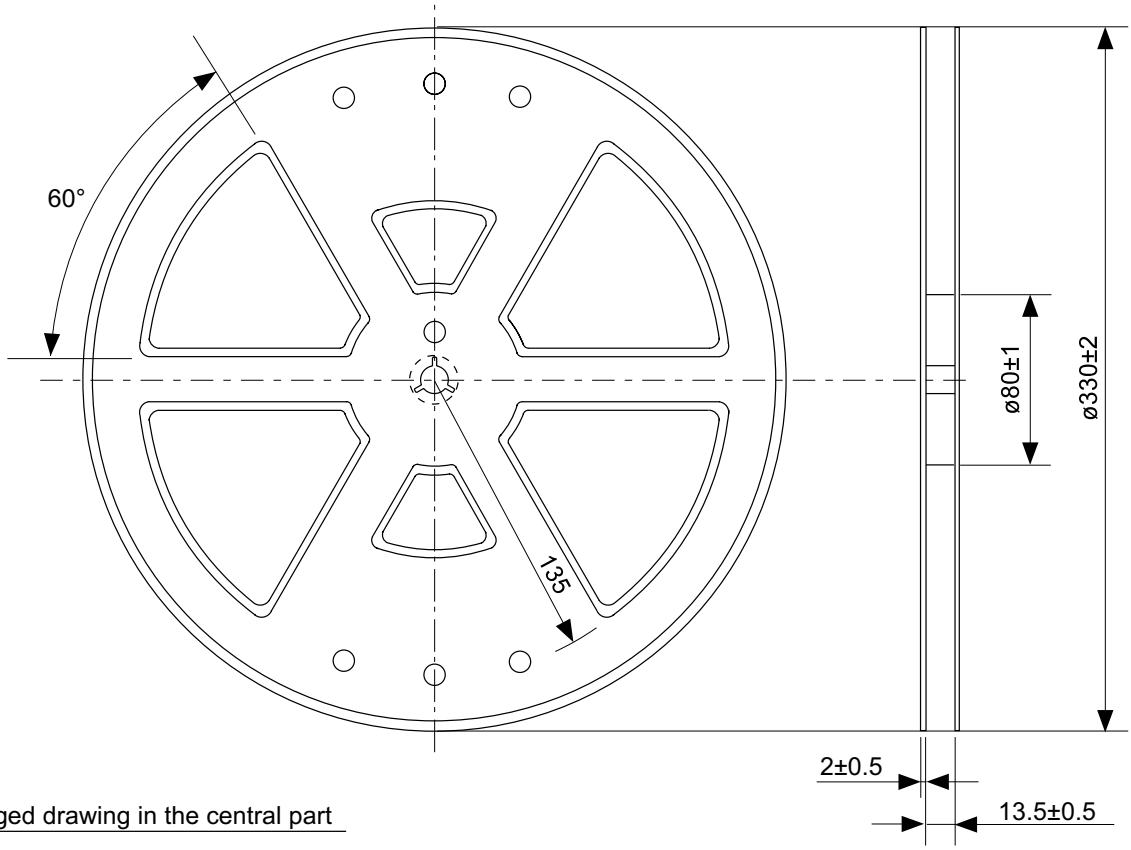
TITLE	SOP8J-D-PKG Dimensions
No.	FJ008-A-P-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



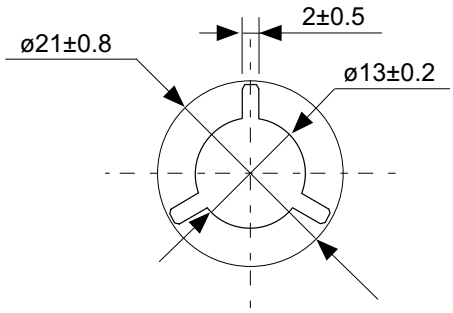


No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FJ008-D-R-SD-1.1

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-SD-1.1		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			

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