2-WIRE CMOS SERIAL E^2PROM S-24C04BPHAL

The S-24C04BPHAL is a 2-wire, low-power, wide-range-operation 4K-bit serial E^2PROM organized as 512 words × 8 bits. Page write and sequential read are possible.

■ Features

- Low power consumption — Standby: 1.0 µA max. (V_{CC} = 5.5 V); Operating: 0.8 mA max. (V_{CC} = 5.5 V), 0.3 mA max. (V_{CC} = 3.3 V)
- Wide operating voltage range: Reading: 1.6 to 5.5 V; Writing: 1.7 to 5.5 V
- Page write: 16 bytes/page
- Sequential read
- Operating frequency: 400 kHz (V_{CC} = 5 V ±10%)
- Endurance: 10^6 cycles/word[*1]
  ***1.** For each address (Word: 8 bits)
- Data retention: 10 years
- Write protection 100%
- Lead-free products

■ Package

Package Name	Drawing Code		
	Package	Tape	Reel
WLP	Please contact our sales office regarding the product with WLP package.		

Caution This product is intended for use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry, and engine control units, be sure to contact SII.

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■ Pin Configuration

WLP
Bottom view

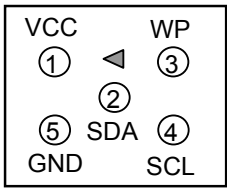

Figure 1

S-24C04BPHAL

Table 1

Pin No.	Symbol	Description
1	VCC	Power supply
2	SDA	Serial data input/output
3	WP	Write protection input pin Connected to Vcc: Protection valid Connected to GND: Protection invalid
4	SCL	Serial clock input
5	GND	Ground

Remark Please contact our sales office regarding the product with WLP package.

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■ Block Diagram

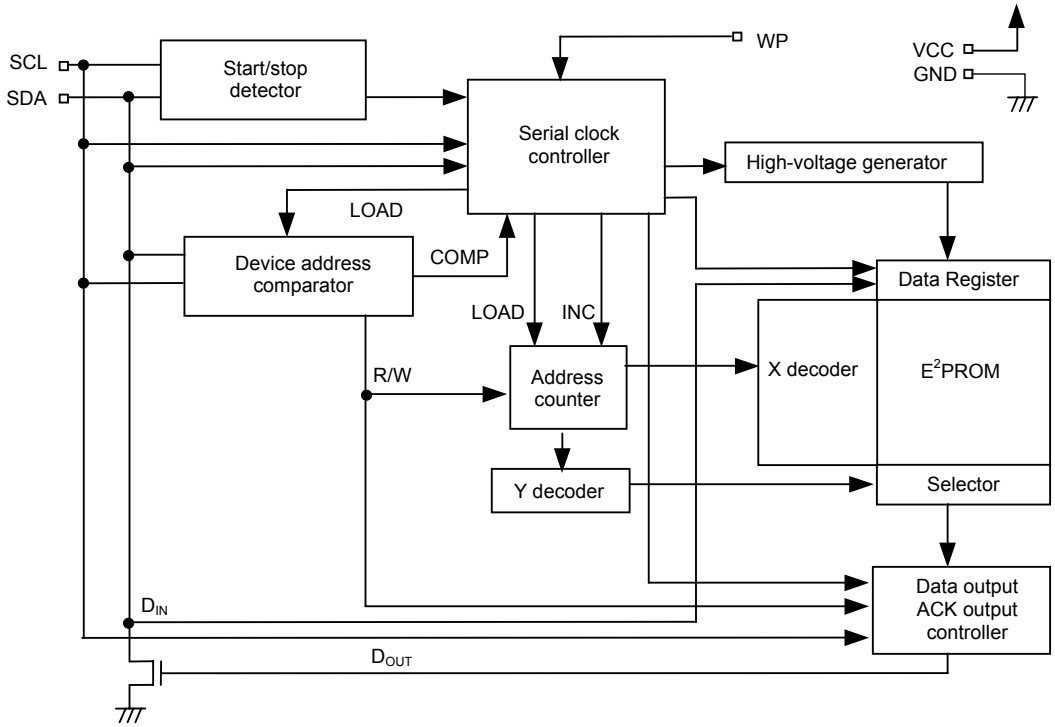

Figure 2

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■ Absolute Maximum Ratings

Table 2

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}	V
Operating ambient temperature	T_{opr}	−40 to + 85	°C
Storage temperature	T_{stg}	−65 to + 150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any condition.

■ Recommended Operating Conditions

Table 3

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Reading	1.6	–	5.5	V
		Writing	1.7	–	5.5	V
High-level input voltage	V_{IH}	V_{CC} = 2.5 to 5.5 V	0.7 × V_{CC}	–	V_{CC}	V
		V_{CC} = 1.6 to 2.5 V	0.8 × V_{CC}	–	V_{CC}	V
Low-level input voltage	V_{IL}	V_{CC} = 2.5 to 5.5 V	0.0	–	0.3 × V_{CC}	V
		V_{CC} = 1.6 to 2.5 V	0.0	–	0.2 × V_{CC}	V

■ Pin Capacitance

Table 4

(Ta = 25°C, f = 1.0 MHz, Vcc = 5 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V (SCL, WP)	–	–	10	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V (SDA)	–	–	10	pF

■ Endurance

Table 5

Item	Symbol	Operating Temperature	Min.	Typ.	Max.	Unit
Endurance	N_W	−40 to +85°C	10^6	–	–	Cycles/word*1

***1.** For each address (Word: 8 bits)

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■ DC Electrical Characteristics

Table 6

Item	Symbol	Conditions	V_{CC} = 4.5 to 5.5 V			V_{CC} = 2.5 to 4.5 V			V_{CC} = 1.6 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	f = 100 kHz	–	–	0.8*1	–	–	0.3	–	–	0.2	mA
Current consumption (PROGRAM)	I_{CC2}	f = 100 kHz	–	–	4.0	–	–	1.5	–	–	1.5*2	mA

***1.** f = 400 kHz

***2.** V_{CC} = 1.7 to 2.5 V

Table 7

Item	Symbol	Conditions	V_{CC} = 4.5 to 5.5 V			V_{CC} = 2.5 to 4.5 V			V_{CC} = 1.6 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	V_{IN} = V_{CC} or GND	–	–	1.0	–	–	0.6	–	–	0.4	µA
Input current leakage	I_{LI}	V_{IN} = GND to V_{CC}	–	0.1	1.0	–	0.1	1.0	–	0.1	1.0	µA
Output current leakage	I_{LO}	V_{OUT} = GND to V_{CC}	–	0.1	1.0	–	0.1	1.0	–	0.1	1.0	µA
Low-level output voltage	V_{OL}	I_{OL} = 3.2 mA	–	–	0.4	–	–	0.4	–	–	–	V
		I_{OL} = 1.5 mA	–	–	0.3	–	–	0.3	–	–	0.5	V
Current address hold voltage	V_{AH}	–	1.5	–	5.5	1.5	–	4.5	1.5	–	2.5	V

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■ AC Electrical Characteristics

Table 8 Measurement Conditions

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Input pulse rise/fall time	20 ns
Output judgment voltage	$0.5 \times V_{CC}$
Output load	100 pF + pull-up resistor 1.0 kΩ

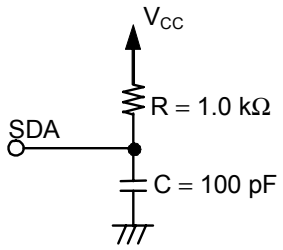

Figure 3 Output Load Circuit

Table 9

Item	Symbol	V_{CC} = 4.5 to 5.5 V			V_{CC} = 1.6 to 4.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	–	400	0	–	100	kHz
SCL clock time "L"	t_{LOW}	1.0	–	–	4.7	–	–	µs
SCL clock time "H"	t_{HIGH}	0.9	–	–	4.0	–	–	µs
SDA output delay time	t_{AA}	0.1	–	0.9	0.1	–	3.5	µs
SDA output hold time	t_{DH}	50	–	–	100	–	–	ns
Start condition setup time	$t_{SU.\ STA}$	0.6	–	–	4.7	–	–	µs
Start condition hold time	$t_{HD.\ STA}$	0.6	–	–	4.0	–	–	µs
Data input setup time	$t_{SU.\ DAT}$	100	–	–	200	–	–	ns
Data input hold time	$t_{HD.\ DAT}$	0	–	–	0	–	–	ns
Stop condition setup time	$t_{SU.\ STO}$	0.6	–	–	4.7	–	–	µs
SCL, SDA rise time	t_R	–	–	0.3	–	–	1.0	µs
SCL, SDA fall time	t_F	–	–	0.3	–	–	0.3	µs
Bus release time	t_{BUF}	1.3	–	–	4.7	–	–	µs
Noise suppression time	t_I	–	–	50	–	–	100	ns

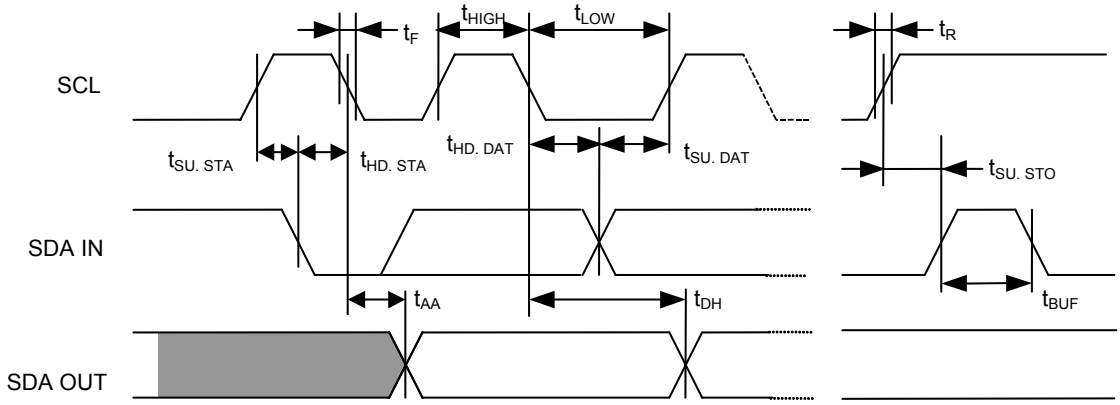

Figure 4 Bus Timing

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Table 10

Item	Symbol	Min.	Typ.	Max.	Unit
Write time	t_{WR}	—	4.0	10.0	ms

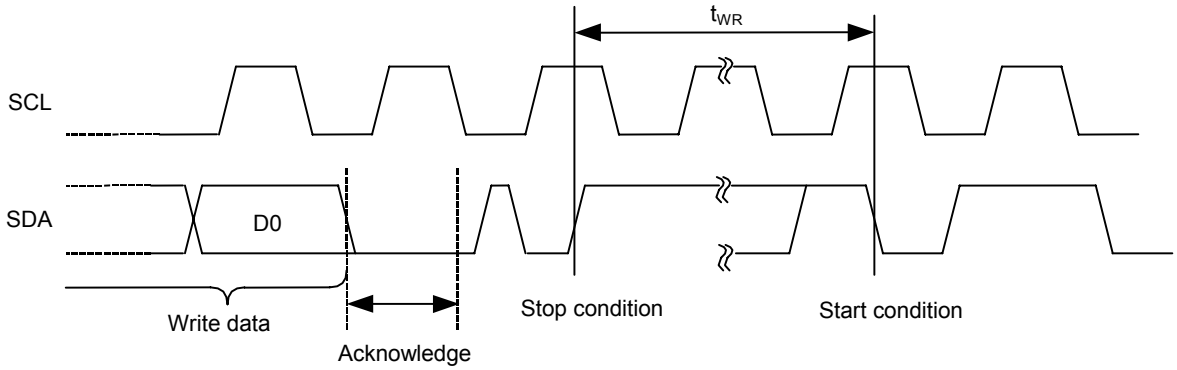

Figure 5 Write Cycle Timing

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■ Pin Functions

1. SDA (Serial Data Input/Output) Pin

The SDA pin is used for bidirectional transfer of serial data. It consists of a signal input pin and an Nch open-drain transistor output pin. Usually pull up the SDA line to V_{CC} via a resistor, and use it with other open-drain or open-collector output devices connected in a wired-OR configuration.

2. SCL (Serial Clock Input) Pin

The SCL pin is used for serial clock input. It is capable of processing signals at the rising and falling edges of the SCL clock input signal. Make sure the rise time and fall time conform to the specifications.

3. WP (Write Protection Input) Pin

The WP pin is used for write protection. When there is no need for write protection, connect the pin to GND; when there is a need for write protection, connect the pin to V_{CC}.

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■ Operation

1. Start condition

When the SDA line changes from “H” to “L” with the SCL line at “H”, the device is in the start condition. All operations begin from the start condition.

2. Stop condition

When the SDA line changes from “L” to “H” with the SCL line at “H”, the device is in the stop condition.
When the device receives the stop condition signal during a read sequence, the read operation is interrupted, and the device enters standby mode.
When the device receives the stop condition signal during a write sequence, the retrieval of write data is halted, and rewriting the E^{2}PROM starts.

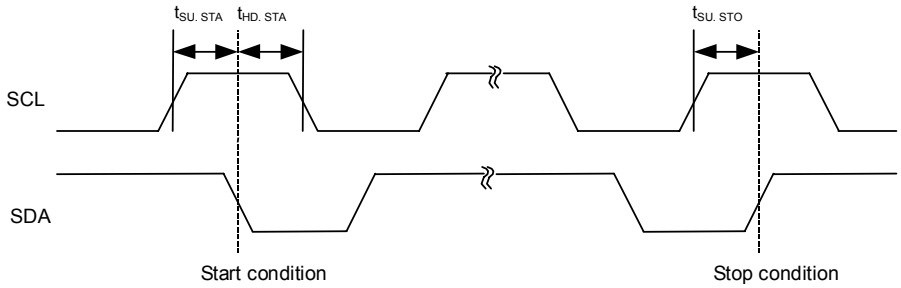

Figure 6 Start/Stop Condition

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3. Data transfer

Changing the SDA line while the SCL line is “L” allows the data to be transferred.
A start or stop condition is recognized when the SDA line changes while the SCL line is “H”.

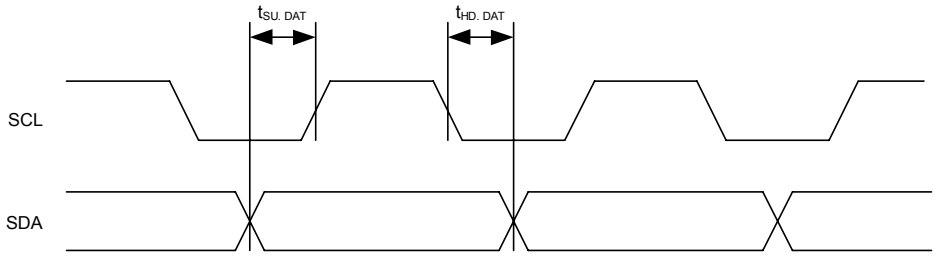

Figure 7 Data Transfer Timing

4. Acknowledgment

8 bits of data are transferred in succession. The device on the system bus that receives the data changes the SDA line to “L” during the 9th clock cycle and outputs the acknowledge signal to inform that it has received the data.
The device does not output the acknowledge signal while the E^{2}PROM is being rewritten.

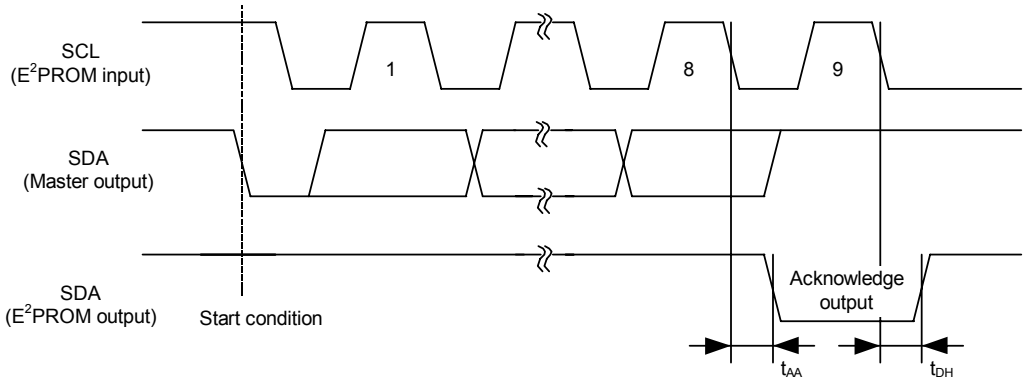

Figure 8 Acknowledge Output Timing

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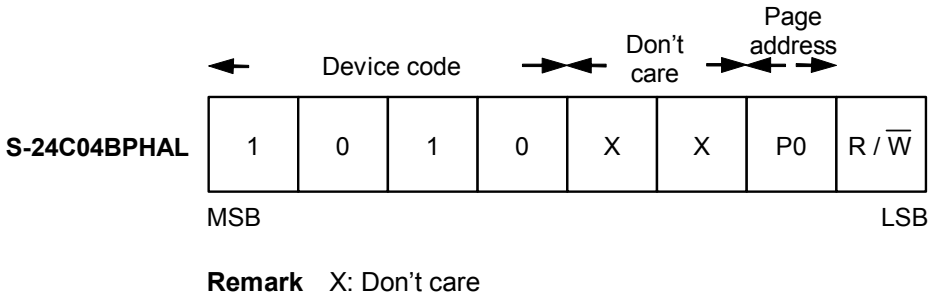
5. Device addressing

To perform data communications, the master device mounted on the system outputs the start condition signal to the slave device. Next, the master device outputs a 7-bit device address and a 1-bit read/write instruction code onto the SDA bus.
The higher 4 bits of the device address are called the “Device Code”, and are fixed to “1010”. The following 2 bits are “don’t care” bits.
When the comparison results match, the slave device outputs the acknowledge signal during the 9th clock cycle.



Remark X: Don’t care

Figure 9 Device Address

In the S-24C04BPHAL, the 7th bit is a page address bit.
Accordingly, when P0 = 0, the first half of the memory area (2 Kb: addresses 000h to 0FFh) is selected; when P0 = 1, the second half of the memory area (2 Kb; addresses 100h to 1FFh) are selected.

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6. Write operation

6.1 Byte write

When the E^{2}PROM receives a 7-bit device address and the 1-bit read/write instruction code “0”, following the start condition signal, it outputs the acknowledge signal.
Next, when the E^{2}PROM receives an 8-bit word address, it outputs the acknowledge signal.
After the E^{2}PROM receives 8-bit write data and outputs the acknowledge signal, it receives the stop condition signal. Next, rewriting the specified memory address of the E^{2}PROM starts.
While the E^{2}PROM is being rewritten, all operations are prohibited and the acknowledge signal is not output.

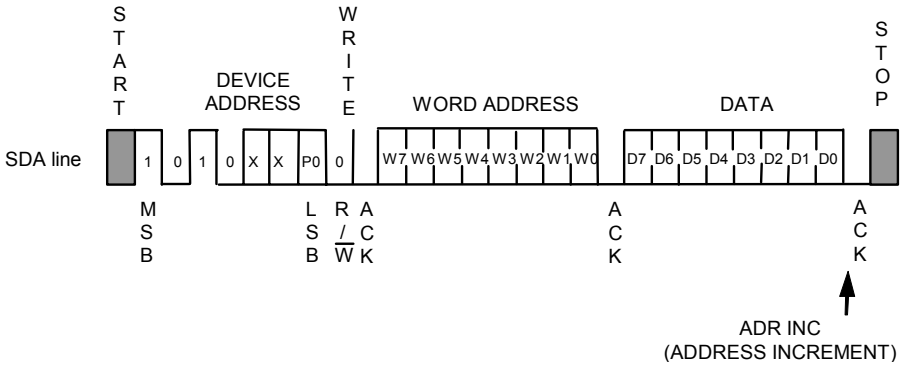

Figure 10 Byte Write

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6.2 Page write

Up to 16 bytes per page can be written in the S-24C04BPHAL.
Basic data transfer procedures are the same as those in “Byte write”. The S-24C04BPHAL performs page write by successively receiving 8-bit write data sized pages.
When the E^{2}PROM receives a 7-bit device address and the 1-bit read/write instruction code “0” following the start condition signal, it outputs the acknowledge signal. When the E^{2}PROM receives an 8-bit word address, it outputs the acknowledge signal. After the E^{2}PROM receives 8-bit write data and outputs the acknowledge signal, it receives 8-bit write data corresponding to the next word address, and outputs the acknowledge signal. The E^{2}PROM repeats reception of 8-bit write data and output of the acknowledge signal in succession and can receive write data corresponding to the maximum page size. When the stop condition signal is received, E^{2}PROM corresponding to the size of the page on which write data starting from the specified memory address is received starts to be rewritten.

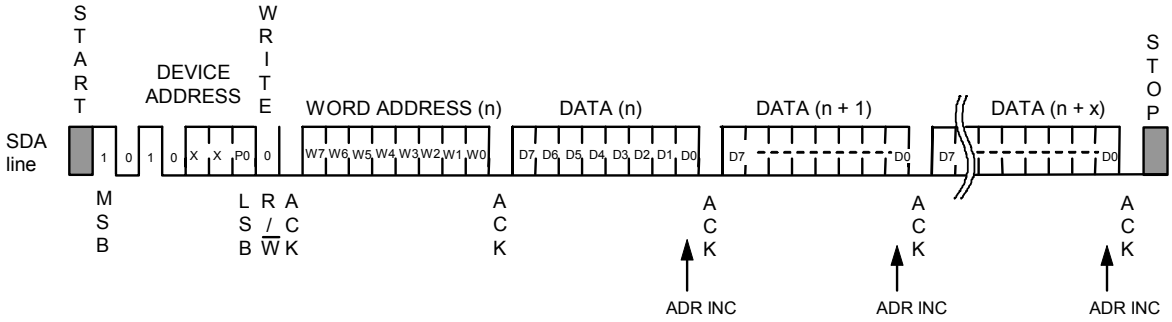

Figure 11 Page Write

The lower 4 bits of the word address are automatically incremented each time when the E^{2}PROM receives 8-bit write data. Even when the write data exceeds 16 bytes, the higher 4 bits of the word address and page address P0 remain unchanged, and the lower 4 bits are rolled over and overwritten.

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6.3 Write Protection

Write protection is available in the S-24C04BPHAL. When the WP pin is connected to the V_{CC}, write operation to memory area is forbidden at all.
When the WP pin is connected to the GND, the write protection is invalid, and write operation in all memory area is available.
Fix the level of the WP pin from the rising edge of SCL for loading the last write data (D0) until the end of the write time (10 ms max.). If the WP pin changes during this time, the address data being written at this time is not guaranteed.
There is no need for using write protection, the WP pin should be connected to the GND. The write protection is valid in the operating voltage range.

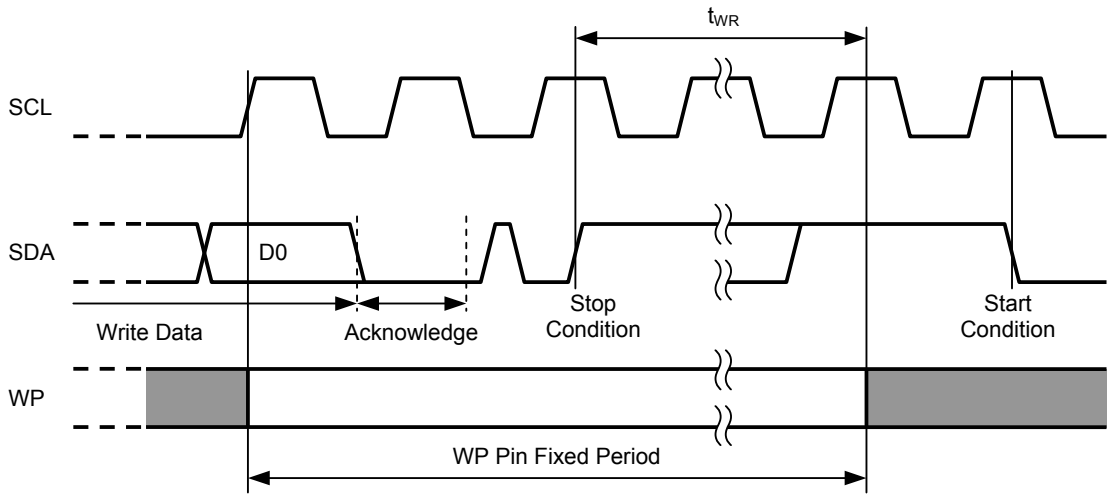

Figure 12 WP Pin Fixed Period

6.4 Acknowledge Polling

Acknowledge polling is used to know the completion of the write cycle in the E^{2}PROM.
After the E^{2}PROM receives a stop condition and once starts the write cycle, all operations are forbidden and no response is made to the signal transmitted by the master device.
Accordingly the master device can recognize the completion of the write cycle in the E^{2}PROM by detecting a response from the slave device after transmitting the start condition, the device address and the read/write instruction code to the E^{2}PROM, namely to the slave devices.
That is, if the E^{2}PROM does not generate an acknowledge, the write cycle is in progress and if the E^{2}PROM generates an acknowledge, the write cycle has been completed.
Keep the level of the WP pin fixed until acknowledge is confirmed.
It is recommended to use the read instruction "1" as the read/write instruction code transmitted by the master device.

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7. Read

7.1 Current address read

The E²PROM holds the last accessed memory address during both writing and reading. The memory address is retained as long as the power voltage is the retention voltage V_{AH} or more. Accordingly, when the master device recognizes the position of the address pointer inside the E²PROM, data can be read from the memory address of the current address pointer without specifying a word address. This is called "Current Address Read".

"Current Address Read" is explained for when the address counter inside the E²PROM is address "n".

When the E²PROM receives a 7-bit device address and the 1-bit read/write instruction code "1", following the start condition signal, it outputs the acknowledge signal.

Next, 8-bit data at address "n" is output from the E²PROM, in synchronization with the SCL clock.

The address counter is incremented to address n + 1 at the falling edge of the SCL clock at which the 8th bit of data is output. The master device does not output the acknowledge signal and transmits the stop condition signal to finish reading.

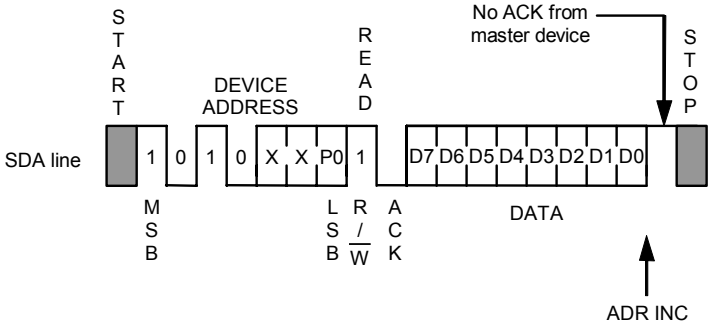

Figure 13 Current Address Read

For recognition of the address pointer inside the E²PROM, take into consideration the following:

The memory address counter inside the E²PROM is automatically incremented for every falling edge of the SCL clock at which the 8th bit of data is output during reading. During writing, the higher bits of the memory address (higher 4 bits of the word address) are left unchanged and are not incremented at any falling of the SCL clock when the 8th bit of the write data is received.

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7.2 Random read

Random read is a mode used when data is read from arbitrary memory addresses.
To load a memory address into the address counter inside the E^{2}PROM, first perform a dummy write following the procedure below.
When the E^{2}PROM receives a 7-bit device address and the 1-bit read/write instruction code “0” following the start condition signal, it outputs the acknowledge signal.
Next, the E^{2}PROM receives an 8-bit word address and outputs the acknowledge signal. The memory address has now been loaded into the address counter of the E^{2}PROM.
Following this, the E^{2}PROM receives the write data during byte or page writing. However, data reception is not performed during dummy write.
The memory address is loaded into the memory address counter inside the E^{2}PROM during dummy write. After that, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition signal and performing the same operation as that in the “Current Address Read”.
That is, when the E^{2}PROM receives a 7-bit device address and the 1-bit read/write instruction code “1” following the start condition signal, it outputs the acknowledge signal.
Next, 8-bit data is output from the E^{2}PROM in synchronization with the SCL clock. The master device does not output an acknowledge signal and transmits the stop condition signal instead. Reading is then complete.

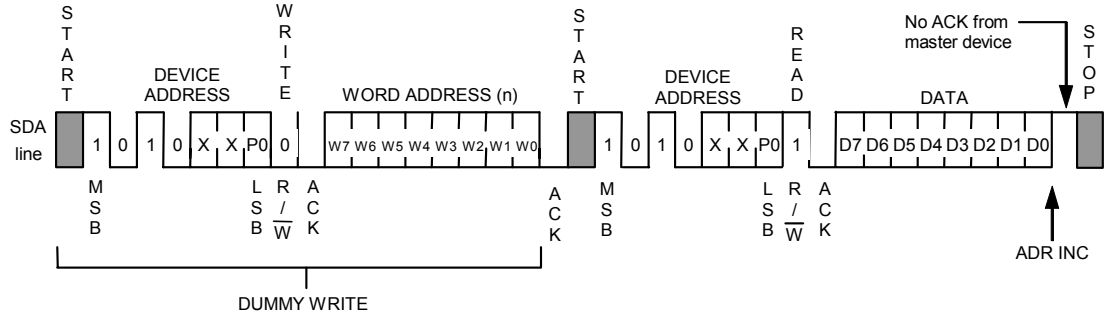

Figure 14 Random Read

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7.3 Sequential read

When the E^{2}PROM receives a 7-bit device address and the 1-bit read/write instruction code “1” in both current and random read operations following the start condition signal, it outputs the acknowledge signal.
When 8-bit data is output from the E^{2}PROM, in synchronization with the SCL clock, the memory address counter inside the E^{2}PROM is automatically incremented at the falling edge of the SCL clock at which the 8th data is output.
When the master device transmits the acknowledge signal, the next memory address data is output.
When the master device transmits the acknowledge signal, the memory address counter inside the E^{2}PROM is incremented and data can be read in succession. This is called “Sequential Read”.
When the master device does not output an acknowledge signal and transmits the stop condition signal, the read operation is finished.
Data can be read in the “Sequential Read” mode in succession. When the memory address counter reaches the last word address, it rolls over to the first memory address.

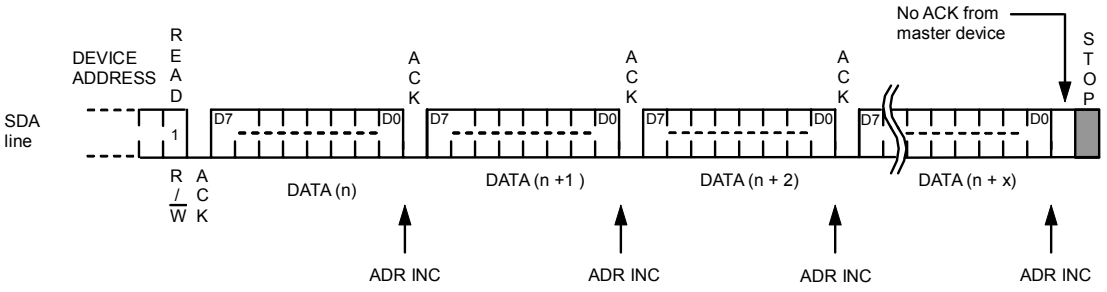

Figure 15 Sequential Read

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8. Address increment timing

The address increment timing is as follows. During a read operation, the memory address counter is automatically incremented at the falling edge of the SCL clock (where the 8th bit of read data is output).
During a write operation, the memory address counter is also automatically incremented at the falling edge of the SCL clock when the 8th bit of write data is fetched.

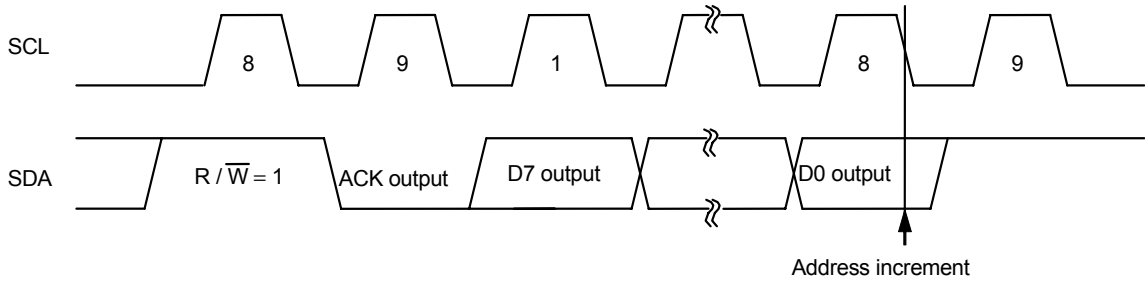

Figure 16 Address Increment Timing in Read Operation

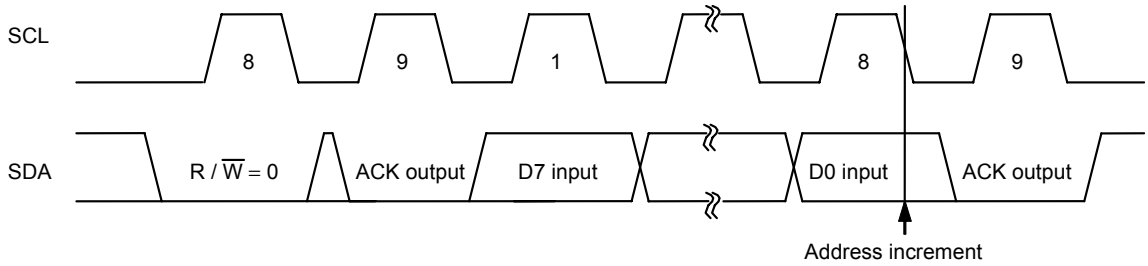

Figure 17 Address Increment Timing in Write Operation

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■ Using S-24C04BPHAL

1. Adding a pull-up resistor to SDA I/O pin and SCL input pin

Add a 1 kΩ to 5 kΩ pull-up resistor to the SCL input pin*1 and the SDA I/O pin in order to enable the functions of the I^{2}C-bus protocol. Normal communication cannot be provided without a pull-up resistor.

***1.** When the SCL input pin of the E^{2}PROM is connected to a tri-state output pin of the microprocessor, connect the same pull-up resistor to prevent a high impedance status from being input to the SCL input pin.
This protects the E^{2}PROM from malfunction due to an undefined output (high impedance) from the tri-state pin when the microprocessor is reset when the voltage drops.

2. Slave address

The S-24C04BPHAL does not have slave address pins (A0, A1, A2). Therefore two or more of this IC cannot be used on the same bus.
However, slave addresses can be used without changing the communication software because they are arbitrary addresses in communication with the master device.

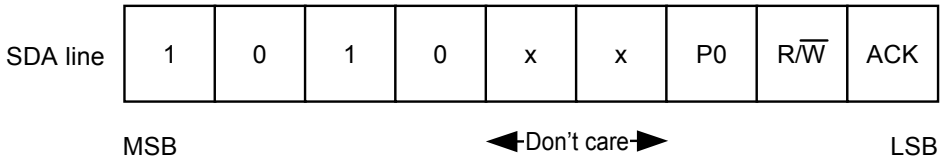

Figure 18

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3. I/O pin equivalent circuit

The I/O pins of this IC do not include pull-up and pull-down resistors. The SDA pin is an open-drain output. The following shows the equivalent circuits.

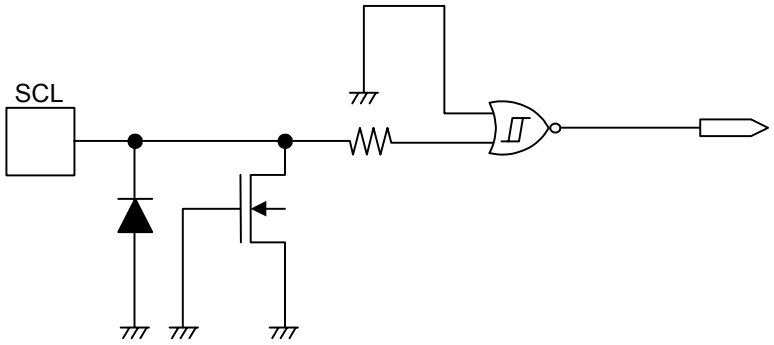

Figure 19 SCL Pin

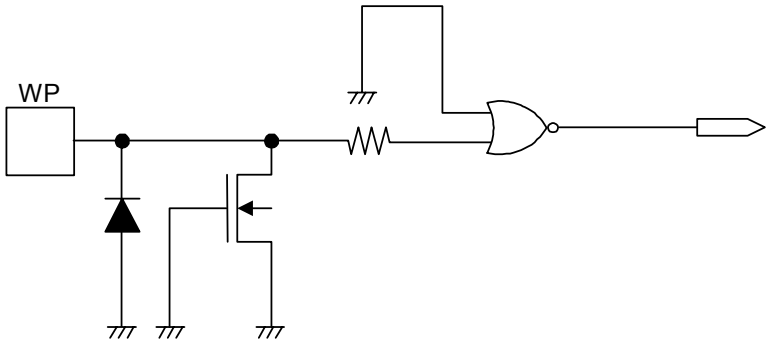

Figure 20 WP Pin

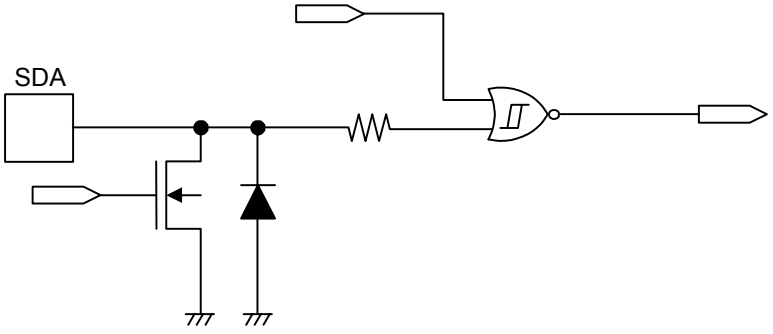

Figure 21 SDA Pin

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4. Maximum effectiveness of write protection

The following conditions must be satisfied to prevent erroneous writing at power-on due to write protection.

(1) Set the WP pin to high level at a time other than when the write instruction is being executed, including during power-on or off.
(2) Adjust the phase after power-on.

Pulling up the WP pin to V_{CC} to always enable the WP pin at the absolute maximum rated voltage or lower prohibits writing all the time regardless of the conditions of the VCC, SDA, and SCL pins.

5. Matching phases while E²PROM is accessed

The S-24C04BPHAL does not have a pin for resetting (the internal circuit), therefore, the E²PROM cannot be forcibly reset externally. If a communication interruption occurs in the E²PROM, it must be reset by software.
For example, even if a reset signal is input to the microprocessor, the internal circuit of the E²PROM is not reset as long as the stop condition is not input to the E²PROM. In other words, the E²PROM retains the same status and cannot shift to the next operation. This symptom applies to the case when only the microprocessor is reset when the power supply voltage drops. With this status, if the power supply voltage is restored, reset the E²PROM (after matching the phase with the microprocessor) and input an instruction. The following shows this reset method.

[How to reset E²PROM]

The E²PROM can be reset by the start and stop instructions. When the E²PROM is reading data "0" or is outputting the acknowledge signal, 0 is output to the SDA line. In this status, the microprocessor cannot output an instruction to the SDA line. In this case, terminate the acknowledge output operation or read operation, and then input a start instruction. **Figure 22** shows this procedure.
First, input the condition. Then transmit 9 clocks (dummy clocks) of SCL. During this time, the microprocessor sets the SDA line to high level. By this operation, the E²PROM interrupts the acknowledge output operation or data output, so input the start condition*1. When a start condition is input, the E²PROM is reset. To make doubly sure, input the stop condition to the E²PROM. Normal operation is then possible.

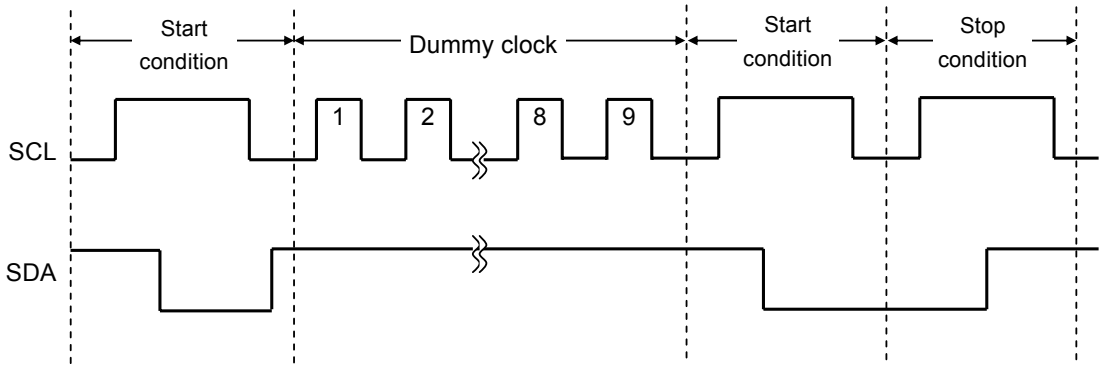

Figure 22 Resetting E²PROM

***1.** After 9 clocks (dummy clocks), if the SCL clock continues to be output without a start condition being input, a write operation may be started upon receipt of a stop condition. To prevent this, input a start condition after 9 clocks (dummy clocks).

Remark It is recommended to perform the above reset using dummy clocks when the system is initialized after the power supply voltage has been raised.

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6. Acknowledge check

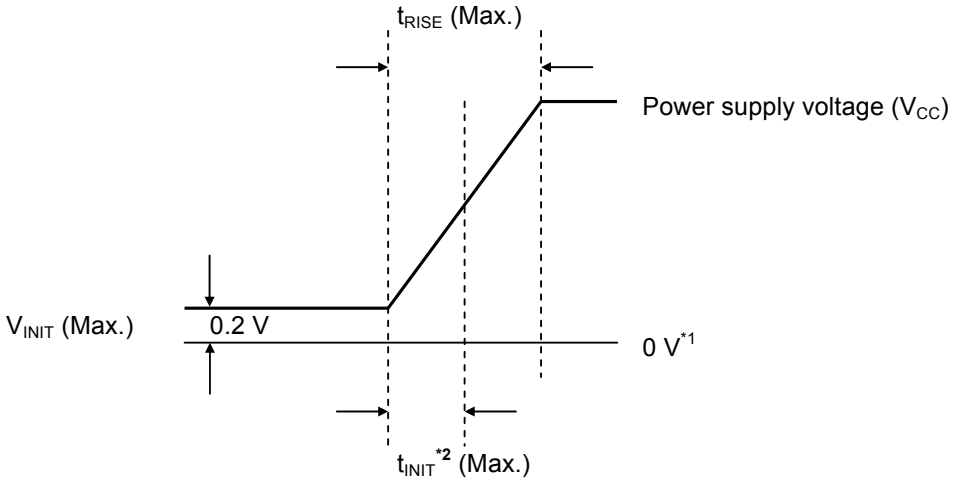
The I²C-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the microprocessor and E²PROM. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check on the microprocessor side.

7. Built-in power-on-clear circuit

E²PROMs have a built-in power-on-clear circuit that initializes the E²PROM. Unsuccessful initialization may cause a malfunction. For the power-on-clear circuit to operate normally, the following conditions must be satisfied for raising the power supply voltage.

7.1 Raising power supply voltage

Raise the power supply voltage, starting at 0.2 V maximum, so that the voltage reaches the power supply voltage to be used within the time defined by t_{RISE} as shown in **Figure 23**.
For example, when the power supply voltage to be used is 5.0 V, t_{RISE} is 200 ms as shown in **Figure 24**.
The power supply voltage must be raised within 200 ms.



***1.** 0 V means there is no difference in potential between the V_{CC} pin and the GND pin of the E²PROM.

***2.** t_{INIT} is the time required to initialize the E²PROM. No instructions are accepted during this time.

Figure 23 Raising Power Supply Voltage

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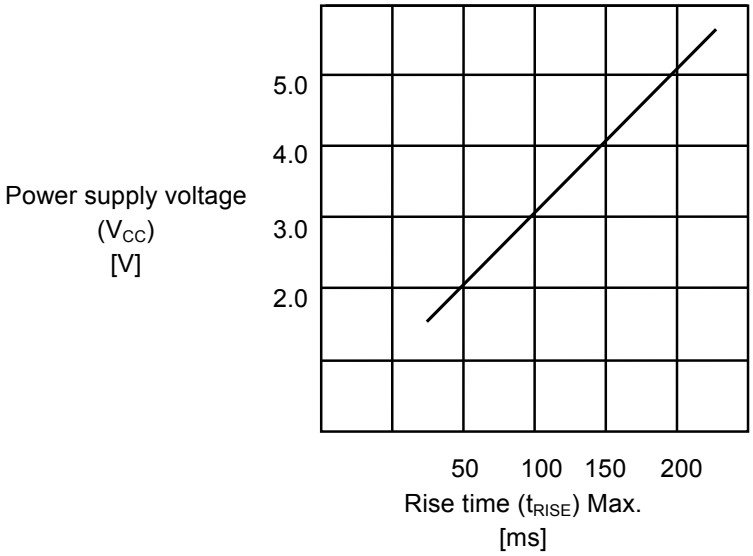

For example:
If your E^{2}PROM supply voltage = 5.0 V, raise the power supply voltage to 5.0 V within 200 ms.

Figure 24 Raising Time of Power Supply Voltage

When initialization is successfully completed via the power-on-clear circuit, the E^{2}PROM enters the standby status.

If the power-on-clear circuit does not operate, the following are the possible causes.

(1) Because the E^{2}PROM has not been initialized, an instruction formerly input is valid or an instruction may be inappropriately recognized. In this case, writing may be performed.
(2) The voltage may have dropped due to power off while the E^{2}PROM is being accessed. Even if the microprocessor is reset due to the low power voltage, the E^{2}PROM may malfunction unless the power-on-clear operation conditions of E^{2}PROM are satisfied. For the power-on-clear operation conditions of E^{2}PROM, refer to **7.1 Raising power supply voltage**.

If the power-on-clear circuit does not operate, match the phase (reset) so that the internal E^{2}PROM circuit is normally reset. The statuses of the E^{2}PROM immediately after the power-on-clear circuit operates and when phase is matched (reset) are the same.

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7.2 Wait for the initialization sequence to end

The E^{2}PROM executes initialization during the time that the supply voltage is increasing to its normal value. All instructions must wait until after initialization. The relationship between the initialization time (t_{INIT}) and rise time (t_{RISE}) is shown in **Figure 25**.

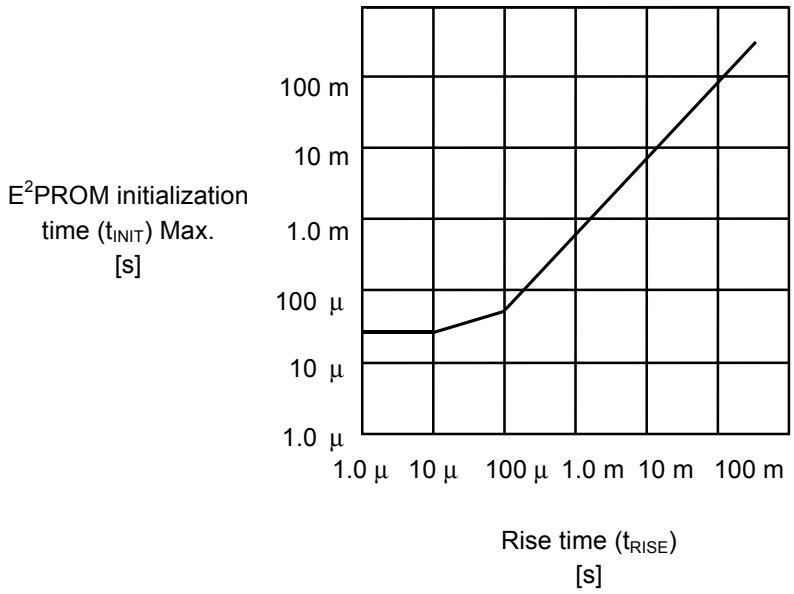

Figure 25 Initialization Time of E^{2}PROM

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8. Data hold time ($t_{HD.\ DAT}$ = 0 ns)

If SCL and SDA of the E^{2}PROM are changed at the same time, it is necessary to prevent the start/stop condition from being mistakenly recognized due to the effect of noise. If a start/stop condition is mistakenly recognized during communication, the E^{2}PROM enters the standby status.
It is recommended that SDA is delayed from the falling edge of SCL by 0.3 µs minimum in the S-24C04BPHAL. This is to prevent time lag caused by the load of the bus line from generating the stop (or start) condition.

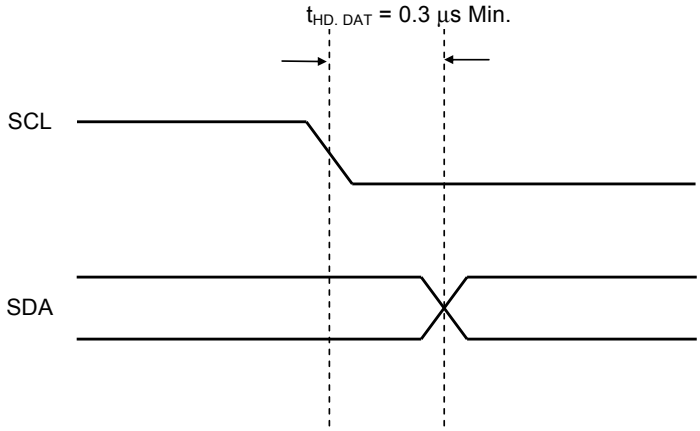

Figure 26 E^{2}PROM Data Hold Time

9. SDA pin and SCL pin noise suppression time

The S-24C04BPHAL includes a built-in low-pass filter to suppress noise at the SDA and SCL pins. This means that if the power supply voltage is 5.0 V (at room temperature), noise with a pulse width of 150 ns or less can be suppressed.
The guaranteed for details, refer to noise suppression time (t_I) in **Table 9**.

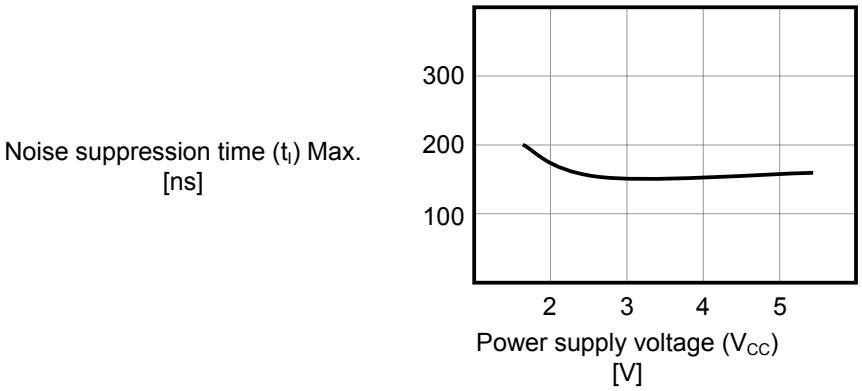

Figure 27 Noise Suppression Time for SDA and SCL Pins

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10. Trap: E^{2}PROM operation in case that the stop condition is received during write operation before receiving the defined data value (less than 8-bit) to SCL pin

When the E^{2}PROM receives the stop condition signal compulsorily, during receiving 1 byte of write data, "write" operation is aborted.
When the E^{2}PROM receives the stop condition signal after receiving 1 byte or more of data for "page write", 8-bit of data received normally before receiving the stop condition signal can be written.

11. Trap: E^{2}PROM operation and write data in case that write data is input more than defined page size at "page write"

When write data is input more than defined page size at page write operation, for example, S-24C04BPHAL (which can be executed 16-byte page write) is received data more than 17 byte, 8-bit data of the 17th byte is over written to the first byte in the same page. Data over the capacity of page address cannot be written.

12. Trap: Severe environments

- Absolute maximum ratings: Do not operate these ICs in excess of the absolute max ratings, as listed on the data sheet. Exceeding the supply voltage rating can cause latch-up.

- Operations with moisture on the E^{2}PROM pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking the E^{2}PROM up from low temperature tank during the evaluation. Be sure that not remain frost on E^{2}PROM pin to prevent malfunction by short-circuit.
  Also attention should be paid in using on environment, which is easy to dew for the same reason.

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■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

■ Precautions for WLP package

- The side of device silicon substrate is exposed to the marking side of device package. Since this portion has lower strength against the mechanical stress than the standard plastic package, chip, crack, etc should be careful of the handing of a package enough. Moreover, the exposed side of silicon has electrical potential of device substrate, and needs to be kept out of contact with the external potential.
- In this package, the overcoat of the resin of translucence is carried out on the side of device area. Keep it mind that it may affect the characteristic of a device when exposed a device in the bottom of a high light source.

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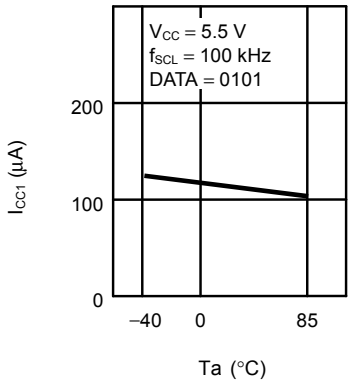
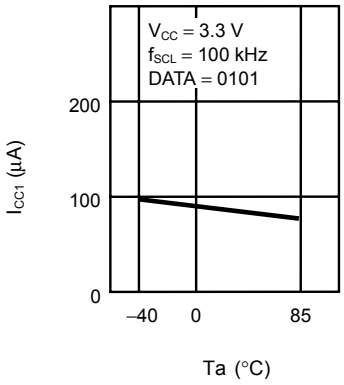
■ Characteristics (Typical Data)

1. DC Characteristics

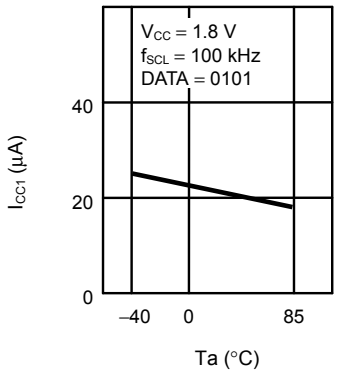
1.1 Current consumption (READ) I_{CC1} – Ambient temperature Ta



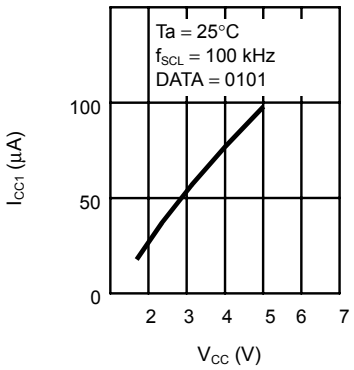
1.2 Current consumption (READ) I_{CC1} – Ambient temperature Ta



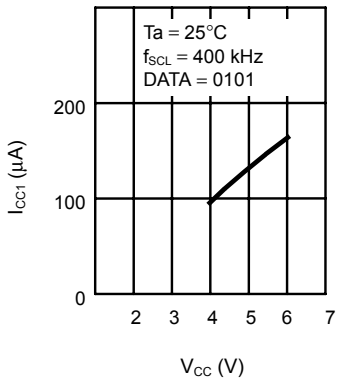
1.3 Current consumption (READ) I_{CC1} – Ambient temperature Ta



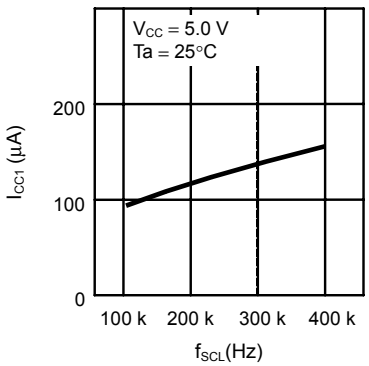
1.4 Current consumption (READ) I_{CC1} – Power supply voltage V_{CC}



1.5 Current consumption (READ) I_{CC1} – Power supply voltage V_{CC}



1.6 Current consumption (READ) I_{CC1} – Clock frequency f_{SCL}



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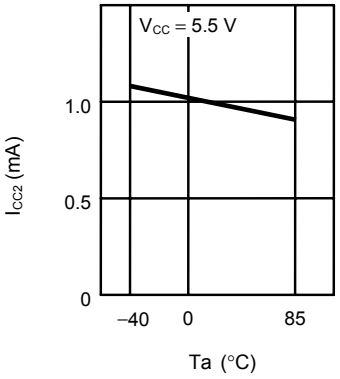
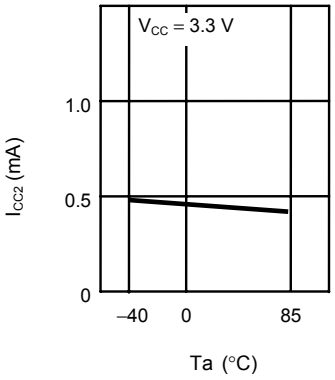
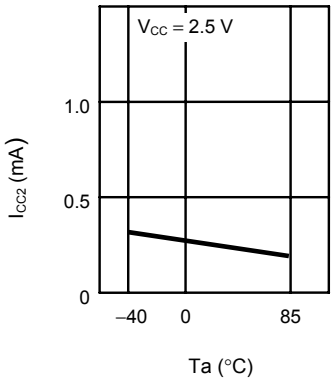
1.7 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



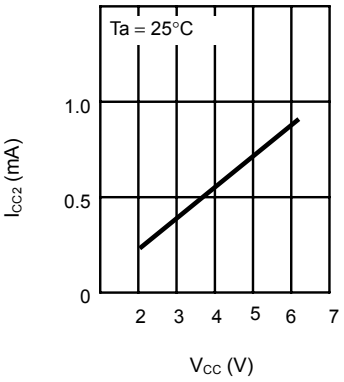
1.8 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



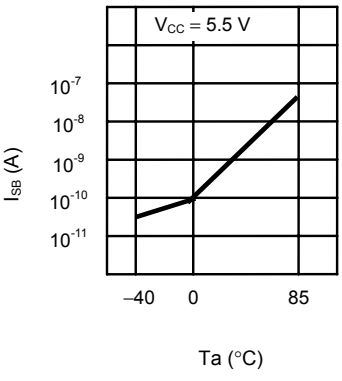
1.9 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



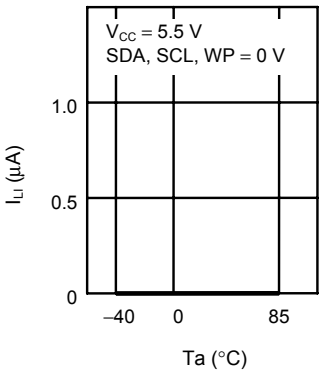
1.10 Current consumption (PROGRAM) I_{CC2} – Power supply voltage V_{CC}



1.11 Standby current consumption I_{SB} – Ambient temperature Ta



1.12 Input current leakage I_{LI} – Ambient temperature Ta



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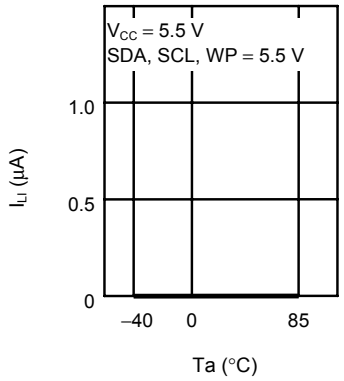
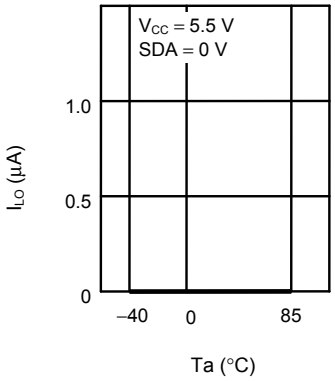
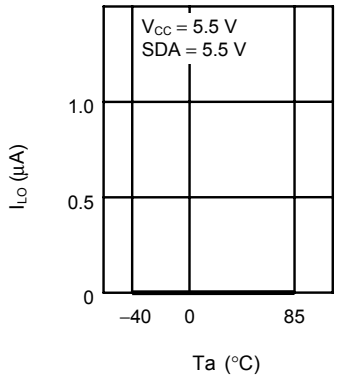
1.13 Input current leakage I_{LI} – Ambient temperature Ta



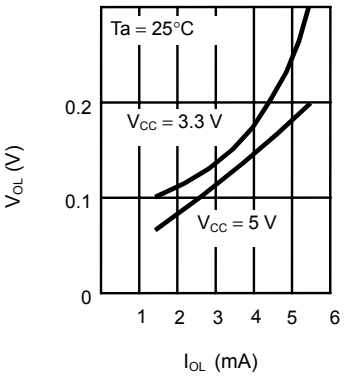
1.14 Output current leakage I_{LO} – Ambient temperature Ta



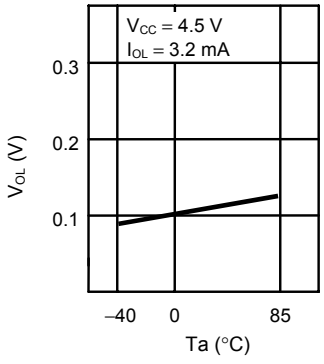
1.15 Output current leakage I_{LO} – Ambient temperature Ta



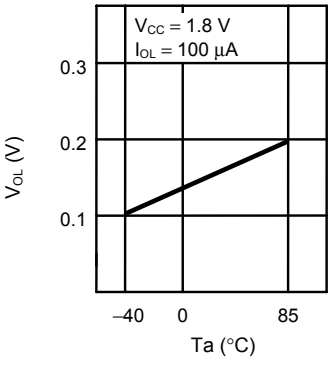
1.16 Low-level output voltage V_{OL} – Low-level output current I_{OL}



1.17 Low-level output voltage V_{OL} – Ambient temperature Ta



1.18 Low-level output voltage V_{OL} – Ambient temperature Ta



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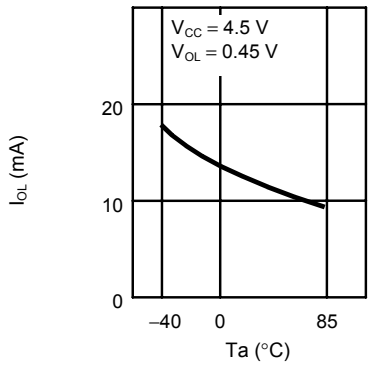
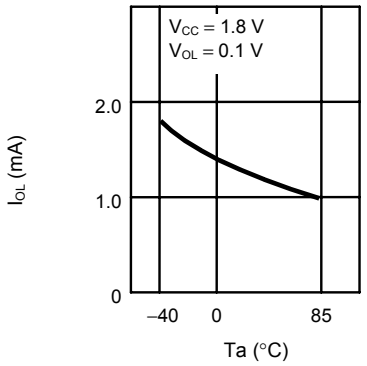
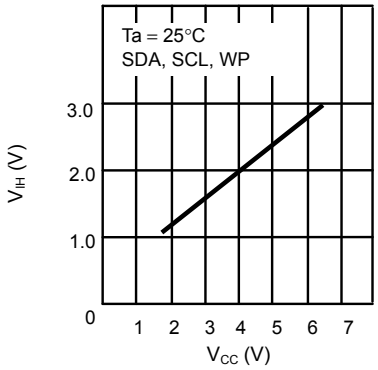
1.19 Low-level output current I_{OL} – Ambient temperature Ta



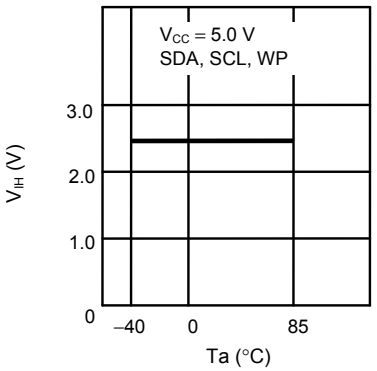
1.20 Low-level output current I_{OL} – Ambient temperature Ta



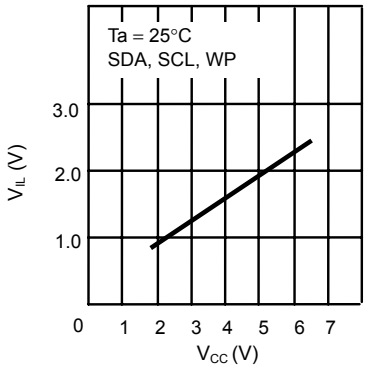
1.21 High input inversion voltage V_{IH} – Power supply voltage V_{CC}



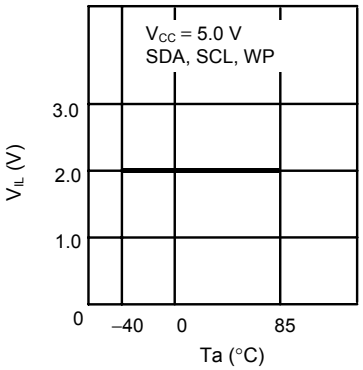
1.22 High input inversion voltage V_{IH} – Ambient temperature Ta



1.23 Low input inversion voltage V_{IL} – Power supply voltage V_{CC}



1.24 Low input inversion voltage V_{IL} – Ambient temperature Ta



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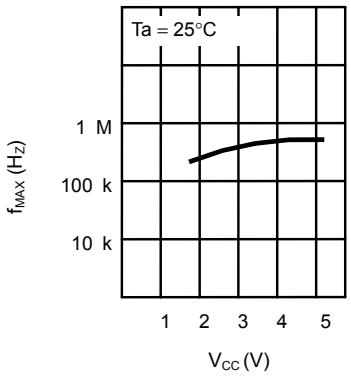
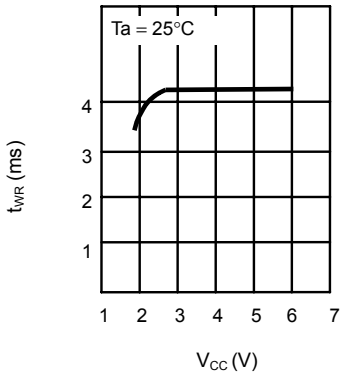
2. AC Characteristics

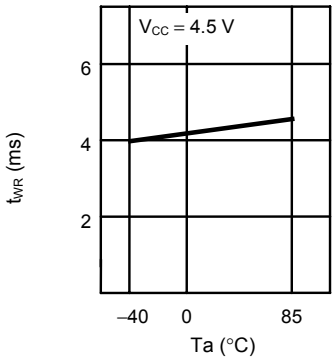
2.1 Maximum operating frequency f_{MAX} – Power supply voltage V_{CC}



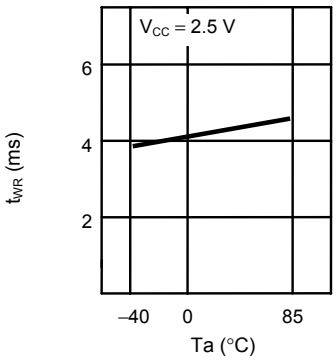
2.2 Write time t_{WR} – Power supply voltage V_{CC}



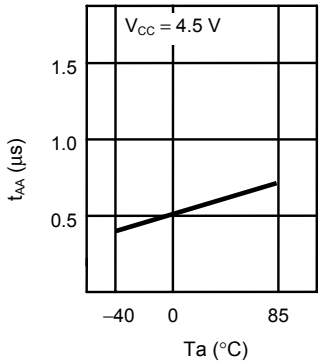
2.3 Write time t_{WR} – Ambient temperature Ta



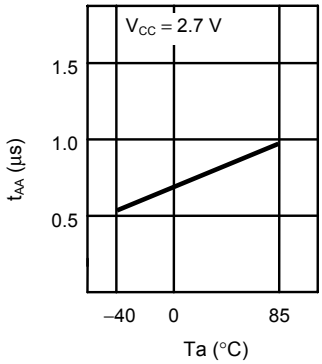
2.4 Write time t_{WR} – Ambient temperature Ta



2.5 SDA output delay time t_{AA} – Ambient temperature Ta



2.6 SDA output delay time t_{AA} – Ambient temperature Ta



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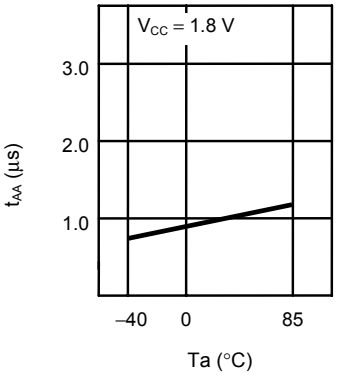
2.7 SDA output delay time t_{AA} – Ambient temperature Ta



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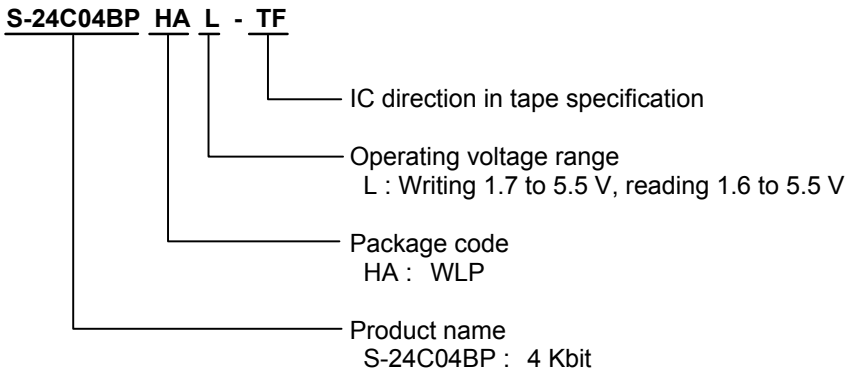
■ Product Name Structure



Remark Please contact our sales office regarding the product with WLP package.

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