

NCP4671

400 mA, Dual Rail Ultra Low Dropout Linear Regulator

The NCP4671 is a CMOS Dual Supply Rail Linear Regulator designed to provide very low output voltages. The Dual Rail architecture which separates the power for the LDO control circuitry (provided via the Vbias pin) from the main power path (VIN) offers ultra-low dropout performance, allowing the device to operate from input voltages down to 0.9 V and to generate a fixed high accuracy output voltage as low as 0.6 V.

The NCP4671 offers excellent transient response with very low quiescent currents. The family is available in a variety of packages: SC-70, SOT23 and a small, ultra thin 1.2 x 1.2 x 0.4mm XDFN.

Features

- Bias Supply Voltage Range : 2.4 V to 5.25 V ($V_{OUT} < 0.8$ V)
Set $V_{OUT} + 1.6$ V to 5.25 V ($V_{OUT} \geq 0.8$ V)
- Power Input Voltage Range : 0.9 V to V_{BIAS} ($V_{OUT} < 0.8$ V)
Set $V_{OUT} + 0.1$ V to V_{BIAS} ($V_{OUT} \geq 0.8$ V)
- Output Voltage Range: 0.6 to 1.5 V (available at 0.1 steps)
- Very Low Dropout: 180 mV Typ. at 400 mA
- Quiescent Current: 28 μ A
- Standby Current: 0.1 μ A
- ± 15 mV Output Voltage Accuracy ($T_A = 25^\circ\text{C}$)
- High PSRR: 80 dB at 1 kHz (Ripple at VIN)
50 dB at 1 kHz (Ripple at VBIAS)
- Current Fold Back Protection Typ. 120 mA
- Available in XDFN, SC-70, SOT23 Package
- These are Pb-Free Devices

Typical Applications

- Battery Powered Equipments
- Portable Communication Equipments
- Cameras, VCRs and Camcorders

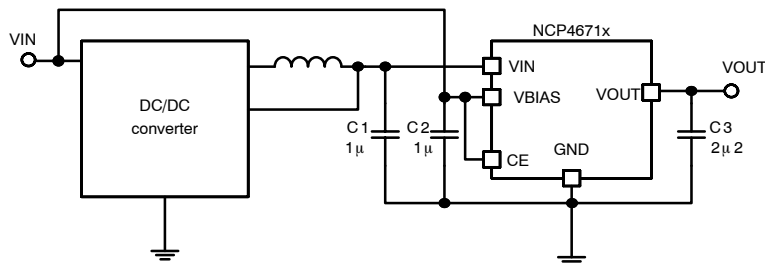


Figure 1. Typical Application Schematic



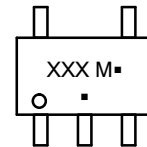
ON Semiconductor™

<http://onsemi.com>

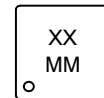
MARKING DIAGRAMS



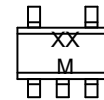
SC-70
CASE 419A
(In Development)



XDFN6
CASE 711AA



SOT-23-5
CASE 1212



XX, XXX= Specific Device Code
M, MM = Date Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NCP4671

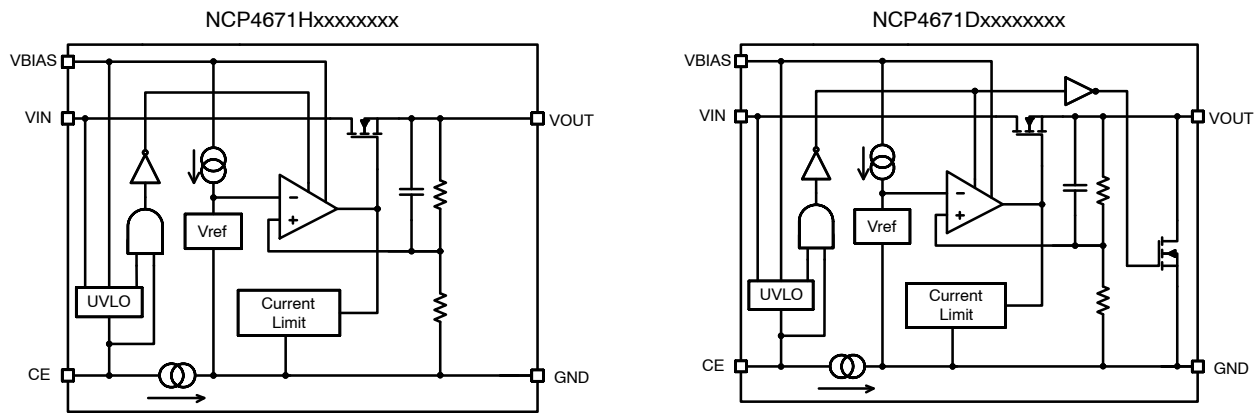


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. XDFN	Pin No. SC-70	Pin No. SOT23	Pin Name	Description
1	1	4	VBIAS	Input Pin 1
2	2	2	GND	Ground Pin
3	5	3	CE	Chip Enable Pin ("H" Active)
4	4	1	VIN	Input Pin 2
5	-	-	NC	Not connected
6	3	5	VOUT	Output Pin

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Bias Supply Input Voltage (Note 1)	V_{BIAS}	6.0	V
Power Supply Input Voltage (for Driver) (Note 1)	V_{IN}	-0.3 to $V_{BIAS} + 0.3$	V
Output Voltage	V_{OUT}	-0.3 to $V_{IN} + 0.3$	V
Chip Enable Input	V_{CE}	6.0	V
Output Current	I_{OUT}	500	mA
Power Dissipation XDFN	P_D	400	mW
Power Dissipation SC-70		380	
Power Dissipation SOT23		420	
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	-55 to 125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
 ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)
 Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

NCP4671

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	250	$^{\circ}\text{C}/\text{W}$
Thermal Characteristics, SOT23 Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	238	$^{\circ}\text{C}/\text{W}$
Thermal Characteristics, SC-70 Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	263	$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{BIAS} = V_{CE} = 3.6\text{ V}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{BIAS} = C_{IN} = 1.0\text{ }\mu\text{F}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C}$.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Supply Input Voltage (Note 3)	$V_{OUT} < 0.8\text{ V}$	V_{BIAS}	2.4		5.25	V
	$V_{OUT} \geq 0.8\text{ V}$		$V_{OUT} + 1.6$	5.25		
Operating Power Input Voltage (Note 3)	$V_{OUT} < 0.8\text{ V}$	V_{IN}	0.9		V_{BIAS}	V
	$V_{OUT} \geq 0.8\text{ V}$		$V_{OUT} + 0.1$	V_{BIAS}		
Output Voltage	$T_A = +25^{\circ}\text{C}$	V_{OUT}	-15		+15	mV
	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		-20	+20		
Output Voltage Temp. Coefficient	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			± 50		ppm/ $^{\circ}\text{C}$
Line Regulation	$V_{BIAS} = 2.4\text{ V}$ to 5.0 V	Line_{Reg}		0.02	0.10	%/ V
	$V_{IN} = V_{OUT} + 0.3\text{ V}$ to 2.4 V			0.02	0.10	
Load Regulation	$I_{OUT} = 1\text{ mA}$ to 400 mA	Load_{Reg}		30	50	mV
Dropout Voltage	Please refer to following detailed table.					
Output Current		I_{OUT}	400			mA
Short Current Limit	$V_{OUT} = 0\text{ V}$	I_{SC}		120		mA
Quiescent Current	$I_{OUT} = 0\text{ mA}$	I_Q		28	40	μA
Standby Current	$V_{CE} = 0\text{ V}$, $T_A = 25^{\circ}\text{C}$	I_{STB}		0.1	3	μA
CE Pin Threshold Voltage	CE Input Voltage "H"	V_{CEH}	0.8			V
	CE Input Voltage "L"	V_{CEL}			0.3	
CE Pull Down Current		I_{PD}		1		μA
V_{IN} Under Voltage Lock Out	$I_{OUT} = 1\text{ }\mu\text{A}$	V_{IN_UVLO}		$V_{OUT} + 0.05$	$V_{OUT} + 0.1$	V
Power Supply Rejection Ratio	$I_{OUT} = 30\text{ mA}$, $f = 1\text{ kHz}$, V_{IN} Ripple 0.2 V_{P-P}	PSRR		80		dB
	$I_{OUT} = 30\text{ mA}$, $f = 1\text{ kHz}$, V_{BIAS} Ripple 0.2 V_{P-P}			50		
Output Noise Voltage	$V_{OUT} = 0.6\text{ V}$, $I_{OUT} = 30\text{ mA}$, $f = 10\text{ Hz}$ to 100 kHz	V_N		70		μV_{rms}
Low Output Nch Tr. On Resistance	D Version only, $V_{BIAS} = 3.6\text{ V}$, $V_{CE} = \text{"L"}$	R_{LOW}		50		Ω

3. If Input Voltage range is between 5.25 V and 5.50 V, the total operational time must be within 500 hrs.

NCP4671

DROPOUT VOLTAGE (V_{DO} [V])

V_{OUT} / V_{BIAS}	V_{DO} [V] @ $I_{OUT} = 200$ mA ($T_A = 25^\circ\text{C}$)						V_{DO} [V] @ $I_{OUT} = 300$ mA		V_{DO} [V] @ $I_{OUT} = 400$ mA	
							$T_A = 25^\circ\text{C}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$T_A = 25^\circ\text{C}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
	2.5 V	3.0 V	3.3 V	3.6 V	4.2 V	5.0 V	3.6 V	3.6 V	3.6 V	3.6 V
0.6 V	0.094	0.093	0.093	0.092	0.092	0.091	0.115	0.180	0.180	0.320
0.7 V	0.094	0.093	0.093	0.092	0.092	0.092	0.120	0.190	0.180	0.320
0.8 V	0.098	0.093	0.093	0.092	0.092	0.092	0.120	0.190	0.180	0.300
0.9 V	0.098	0.094	0.093	0.092	0.092	0.092	0.120	0.190	0.180	0.300
1.0 V	*	0.094	0.093	0.092	0.092	0.092	0.120	0.190	0.180	0.280
1.2 V		0.098	0.096	0.095	0.095	0.094	0.130	0.200	0.180	0.280
1.3 V		0.098	0.096	0.095	0.095	0.095	0.130	0.200	0.180	0.260
1.4 V		0.098	0.096	0.095	0.095	0.095	0.130	0.200	0.180	0.260
1.5 V		*	0.096	0.095	0.095	0.095	0.095	0.130	0.200	0.180

* V_{BIAS} voltage must be equal or more than $V_{OUT(NOM)} + 1.6$ V

APPLICATION INFORMATION

A typical application circuit for the NCP4671 series is shown in Figure 3. The NCP4671 has two independent inputs, VBIAS pin is used for powering control part of the LDO and its value is equal or higher than value of second input pin VIN where voltage that has to be regulated is connected.

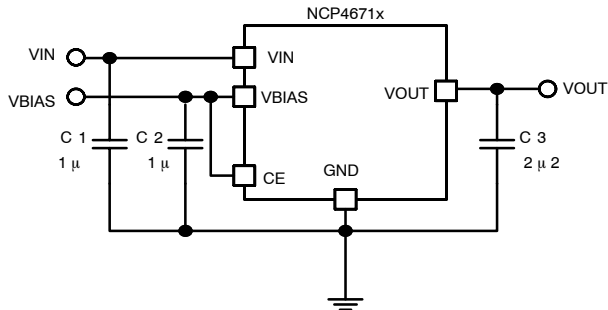


Figure 3. Typical Application Schematic

Dual rail architecture is appropriate when the regulator is connected for example behind a buck DC/DC converter. Bias voltage can be taken from input of the buck DC/DC converter and as input voltage is used output of the buck DC/DC converter as it is shown in Figure 4. Condition that bias voltage must be higher than input voltage can be in this schematic easy fulfilled.

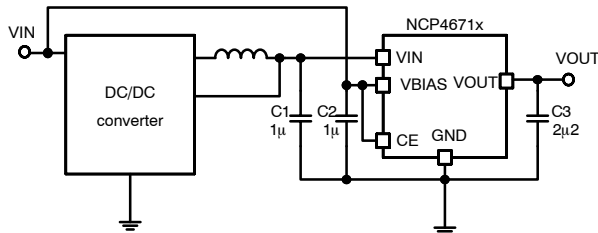


Figure 4. Typical Application Schematic with DC/DC converter

Input Decoupling Capacitors (C1 and C2)

A 1 µF ceramic input decoupling capacitors should be connected as close as possible to the VIN and VBIAS input

and ground pin of the NCP4671. Higher values and lower ESR of capacitor C1 improves line transient response.

Output Decoupling Capacitor (C3)

A 2.2 µF or larger ceramic output decoupling capacitor is sufficient to achieve stable operation of the IC. If a tantalum capacitor is used, and its ESR is high, loop oscillation may result. The capacitors should be connected as close as possible to the output and ground pins. Larger values and lower ESR improves dynamic parameters.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The regulator is switched on when CE pin voltage is above logic high level. The enable pin has an internal pull down current source. If the enable function is not needed connect CE pin to VBIAS.

Output Discharger

The D version includes a transistor between VOUT and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal

As power across the IC increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature rise for the part. That is to say, when the device has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

PCB layout

Make VIN, VBIAS and GND line sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1, C2 and C3 as close as possible to the IC, and make wiring as short as possible.

NCP4671

ORDERING INFORMATION

Device	Marking	Enable	Package	Shipping [†]
NCP4671DSN06T1G	R1A	Auto-Discharge	SOT-23-5 (Pb-Free)	3000 / Tape & Reel
NCP4671DSN09T1G	R1D	Auto-Discharge	SOT-23-5 (Pb-Free)	3000 / Tape & Reel
NCP4671DSN10T1G	R1E	Auto-Discharge	SOT-23-5 (Pb-Free)	3000 / Tape & Reel
NCP4671DSN12T1G	R1F	Auto-Discharge	SOT-23-5 (Pb-Free)	3000 / Tape & Reel
NCP4671DSN13T1G	R1G	Auto-Discharge	SOT-23-5 (Pb-Free)	3000 / Tape & Reel
NCP4671DSN15T1G	R1J	Auto-Discharge	SOT-23-5 (Pb-Free)	3000 / Tape & Reel
NCP4671DMX06TCG	BA	Auto-Discharge	XDFN6 (Pb-Free)	5000 / Tape & Reel
NCP4671DMX09TCG	BD	Auto-Discharge	XDFN6 (Pb-Free)	5000 / Tape & Reel
NCP4671DMX12TCG	BF	Auto-Discharge	XDFN6 (Pb-Free)	5000 / Tape & Reel
NCP4671DMX13TCG	BG	Auto-Discharge	XDFN6 (Pb-Free)	5000 / Tape & Reel
NCP4671DMX15TCG	BJ	Auto-Discharge	XDFN6 (Pb-Free)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

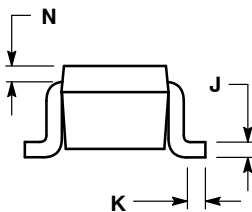
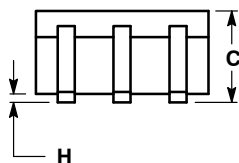
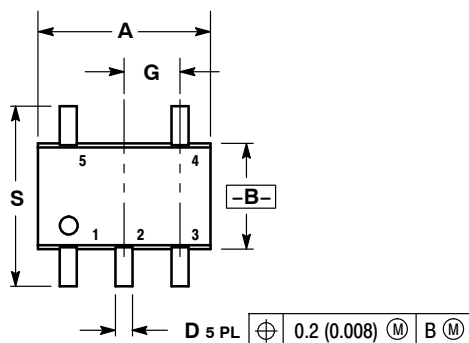
NCP4671

PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)

CASE 419A-02

ISSUE K



NOTES:

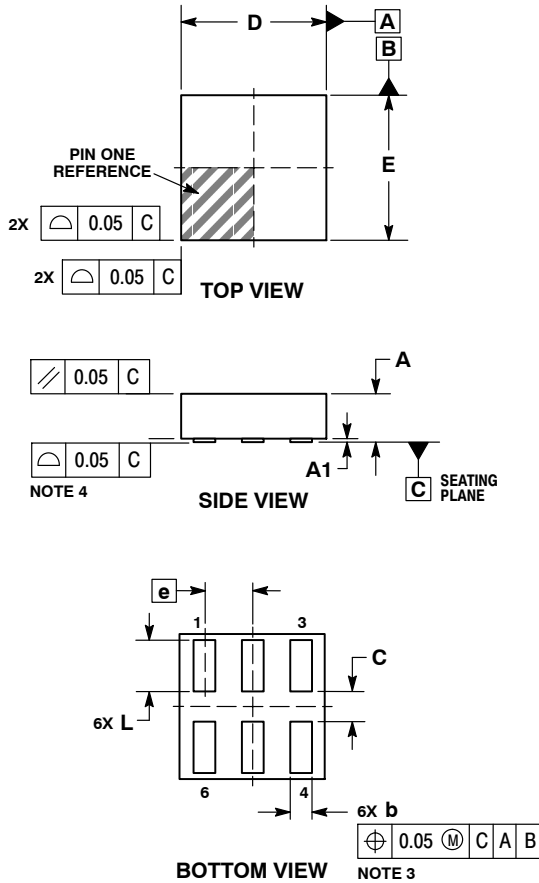
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

NCP4671

PACKAGE DIMENSIONS

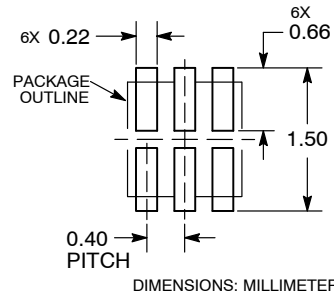
XDFN6 1.2x1.2, 0.4P
CASE 711AA-01
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25mm FROM TERMINAL TIPS.
 4. COPLANARITY APPLIES TO ALL OF THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.13	0.23
C	0.20	0.30
D	1.20 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.37	0.48

RECOMMENDED MOUNTING FOOTPRINT*

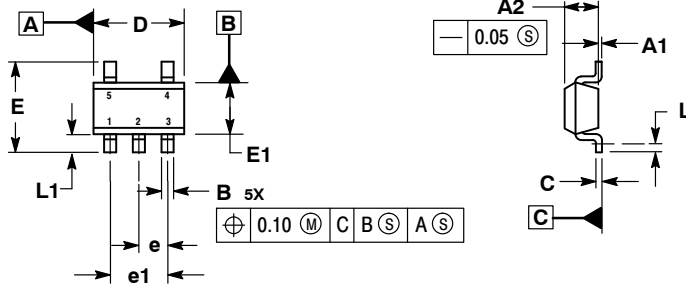


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCP4671

PACKAGE DIMENSIONS

SOT-23
CASE 1212-01
ISSUE O



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM C IS A SEATING PLANE.

MILLIMETERS		
DIM	MIN	MAX
A1	0.00	0.10
A2	1.00	1.30
B	0.30	0.50
C	0.10	0.25
D	2.80	3.00
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
e1	1.90 BSC	
L	0.20	---
L1	0.45	0.75

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

NCP4671/D