256 MBit Synchronous DRAM

- High Performance:

	-6	-7	-7.5	-8	Units
fCK	166	143	133	125	MHz
tCK3	6	7	7.5	8	ns
tAC3	5	5.4	5.4	6	ns
tCK2	7.5	7.5	10	10	ns
tAC2	5.4	5.4	6	6	ns

- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C operating temperature
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{\text{CAS}}$ Latency: 2 & 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  1, 2, 4, 8 and full page
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x4, x8)
- Data Mask for byte control (x16)
- Auto Refresh (CBR) and Self Refresh
- Power Down and Clock Suspend Mode
- 8192 refresh cycles / 64 ms (7,8 µs)
- Random Column Address every CLK
  (1-N Rule)
- Single 3.3V +/- 0.3V Power Supply
- LVTTL Interface versions
- Plastic Packages:
  P-TSOPII-54 400mil width (x4, x8, x16)
- Chipsize Packages:
  54 ball TFBGA (12 mm x 8 mm)
- -6 parts for PC166 3-3-3 operation
  -7 parts for PC133 2-2-2 operation
  -7.5 parts for PC133 3-3-3 operation
  -8 parts for PC100 2-2-2 operation

The HYB39S256400/800/160DT(L) are four bank Synchronous DRAM's organized as 4 banks x 16MBit x4, 4 banks x 8MBit x8 and 4 banks x 4Mbit x16 respectively. These synchronous devices achieve high speed data transfer rates for $\overline{\text{CAS}}$-latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with INFINEON's advanced 0.14 µm 256MBit DRAM process technology.

The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, $\overline{\text{CAS}}$ latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3V +/- 0.3V power supply. All 256Mbit components are available in TSOPII-54 and TFBGA-54 packages.

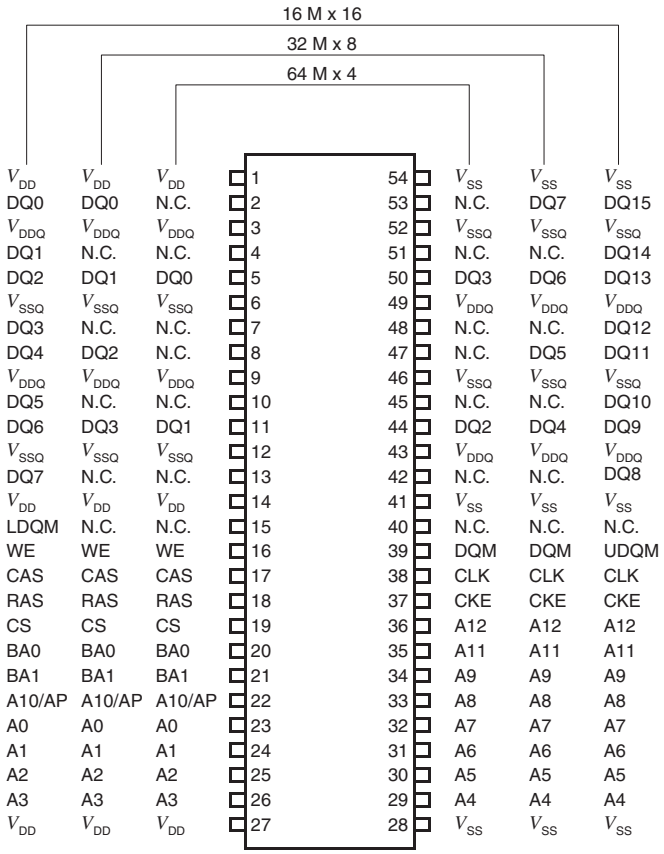
Ordering Information

Type	Speed Grade	Package	Description
HYB 39S256400DT-6	PC166-333-520	P-TSOP-54-2 (400mil)	166MHz 4B x 16M x 4 SDRAM
HYB 39S256400DT-7	PC133-222-520	P-TSOP-54-2 (400mil)	143MHz 4B x 16M x 4 SDRAM
HYB 39S256400DT-7.5	PC133-333-520	P-TSOP-54-2 (400mil)	133MHz 4B x 16M x 4 SDRAM
HYB 39S256400DT-8	PC100-222-620	P-TSOP-54-2 (400mil)	125MHz 4B x 16M x 4 SDRAM
HYB 39S256800DT-6	PC166-333-520	P-TSOP-54-2 (400mil)	166MHz 4B x 8M x 8 SDRAM
HYB 39S256800DT-7	PC133-222-520	P-TSOP-54-2 (400mil)	143MHz 4B x 8M x 8 SDRAM
HYB 39S256800DT-7.5	PC133-333-520	P-TSOP-54-2 (400mil)	133MHz 4B x 8M x 8 SDRAM
HYB 39S256800DT-8	PC100-222-620	P-TSOP-54-2 (400mil)	125MHz 4B x 8M x 8 SDRAM
HYB 39S256160DT-6	PC166-333-520	P-TSOP-54-2 (400mil)	166MHz 4B x 4M x 16 SDRAM
HYB 39S256160DT-7	PC133-222-520	P-TSOP-54-2 (400mil)	143MHz 4B x 4M x 16 SDRAM
HYB 39S256160DT-7.5	PC133-333-520	P-TSOP-54-2 (400mil)	133MHz 4B x 4M x 16 SDRAM
HYB 39S256160DT-8	PC100-222-620	P-TSOP-54-2 (400mil)	125MHz 4B x 4M x 16 SDRAM
HYB39S256800DTL-x		P-TSOP-54-2 (400mil)	4B x 8M x 8 SDRAM Low Power Versions (on request)
HYB39S256160DTL-x		P-TSOP-54-2 (400mil)	4B x 4M x 16 SDRAM Low Power Versions (on request)
HYB39S256xx0DC(L)-x		P-TFBGA-54	(on request)

Pin Description:

CLK	Clock Input	**DQx**	Data Input /Output
CKE	Clock Enable	**DQM, LDQM, UDQM**	Data Mask
$\overline{CS}$	Chip Select	**V_{DD}**	Power (+3.3V)
$\overline{RAS}$	Row Address Strobe	**V_{SS}**	Ground
$\overline{CAS}$	Column Address Strobe	**V_{DDQ}**	Power for DQ's (+ 3.3V)
$\overline{WE}$	Write Enable	**V_{SSQ}**	Ground for DQ's
A0-A12	Address Inputs	**NC**	not connected
BA0, BA1	Bank Select		

Pinouts (TSOP-54)



TSOPII-54 (400 mil x 875 mil, 0.8 mm pitch)

SPP04126

Pinouts (TFBGA-54)

Pin Configuration for x16 devices:

1	2	3		7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
A12	A11	A9	G	BA0	BA1	$\overline{CS}$
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

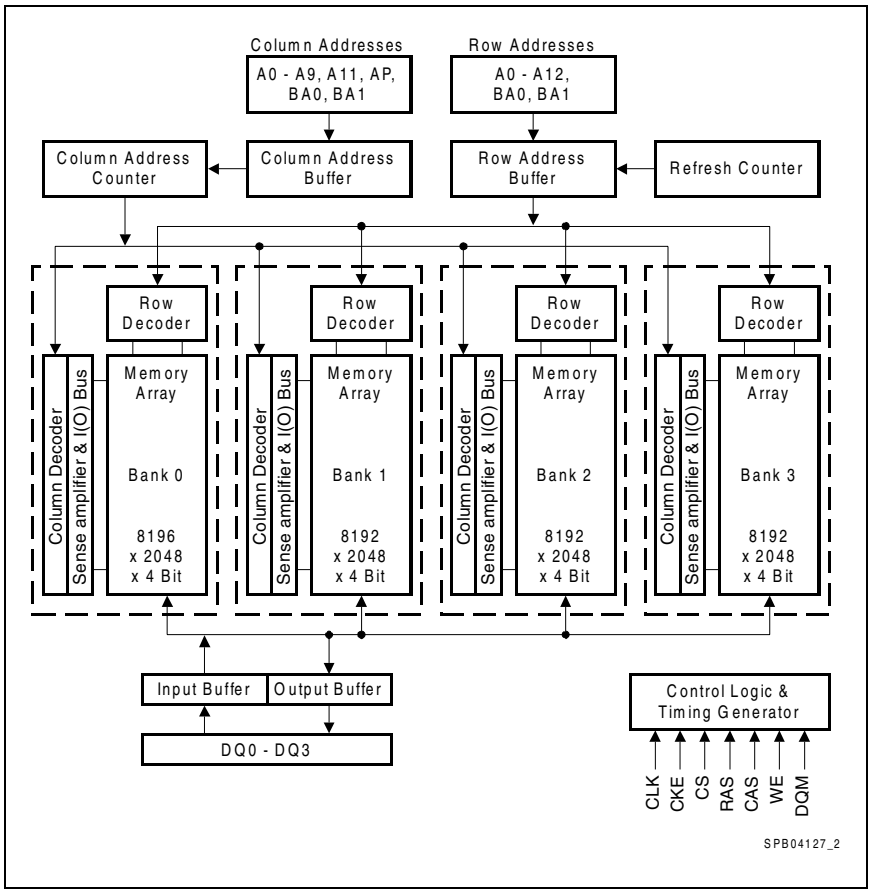
Pin Configuration for x8 devices:

1	2	3		7	8	9
VSS	DQ7	VSSQ	A	VDDQ	DQ0	VDD
NC	DQ6	VDDQ	B	VSSQ	DQ1	NC
NC	DQ5	VSSQ	C	VDDQ	DQ2	NC
NC	DQ4	VDDQ	D	VSSQ	DQ3	NC
NC	NC	VSS	E	VDD	NC	NC
DQM	CLK	CKE	F	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
A12	A11	A9	G	BA0	BA1	$\overline{CS}$
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

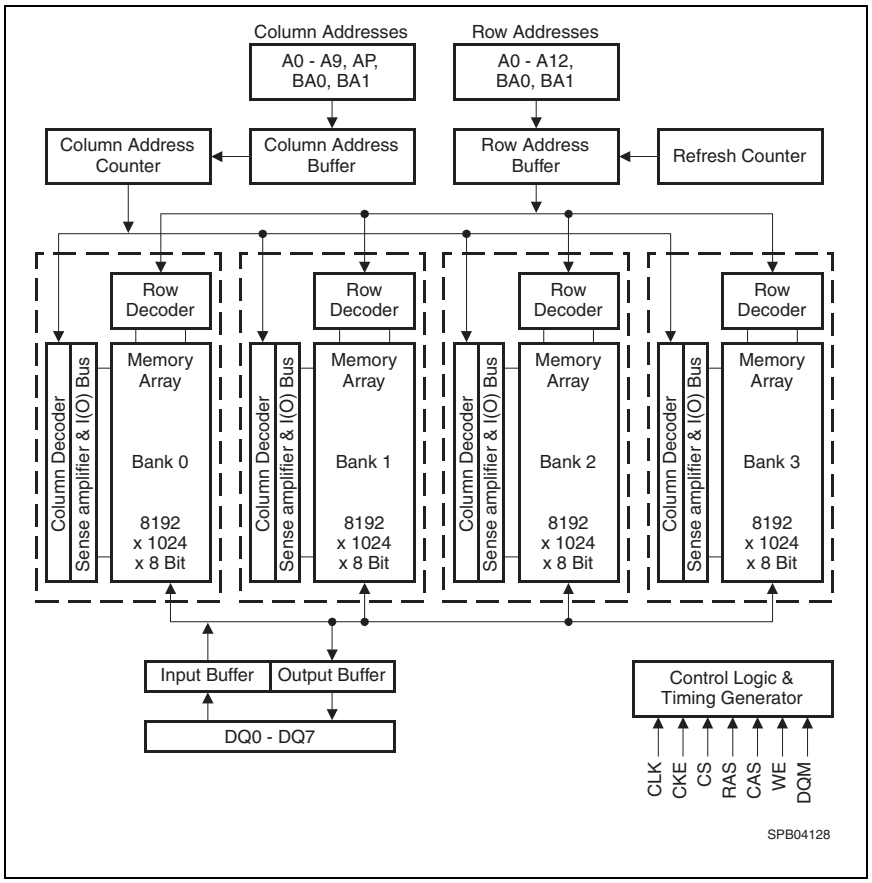
Pin Configuration for x4 devices:

1	2	3		7	8	9
VSS	NC	VSSQ	A	VDDQ	NC	VDD
NC	DQ3	VDDQ	B	VSSQ	DQ0	NC
NC	NC	VSSQ	C	VDDQ	NC	NC
NC	DQ2	VDDQ	D	VSSQ	DQ1	NC
NC	NC	VSS	E	VDD	NC	NC
DQM	CLK	CKE	F	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
A12	A11	A9	G	BA0	BA1	$\overline{CS}$
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

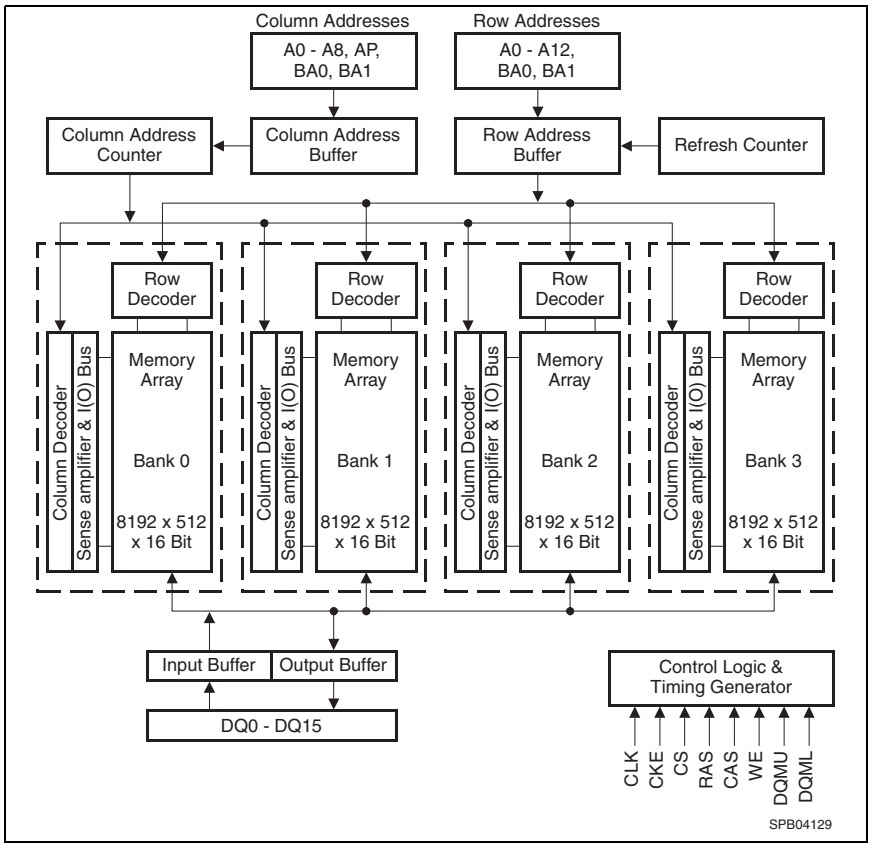
Pinout for x4, x8 & x16 organised 256M-DRAMs



Block Diagram for 64M x 4 SDRAM (13 / 11 / 2 addressing)



Block Diagram for 32M x 8 SDRAM (13 / 10 / 2 addressing)



Block Diagram for 16M x16 SDRAM (13 / 9 / 2 addressing)

Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiating either the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A12	Input	Level	–	During a Bank Activate command cycle, A0-A12 define the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An define the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends upon the SDRAM organization: 64M x4 SDRAM CAn = CA9, CA11 (Page Length = 2048 bits) 32M x8 SDRAM CAn = CA9 (Page Length = 1024 bits) 16M x16 SDRAM CAn = CA8 (Page Length = 512 bits) In addition to the column address, A10(= AP) is used to invoke the autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 (= AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A10 is low, then BA0 and BA1 are used to define which bank to precharge.
BA0, BA1	Input	Level	–	Bank Select Inputs. Bank address inputs selects which of the four banks a command applies to.
DQx	Input Output	Level	–	Data Input/Output pins operate in the same manner as on conventional DRAMs.

Pin	Type	Signal	Polarity	Function
DQM LDQM UDQM	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. One DQM input is present in x4 and x8 SDRAMs, LDQM and UDQM controls the lower and upper bytes in x16 SDRAMs.
V_{DD} V_{SS}	Supply	–	–	Power and ground for the input buffers and the core logic.
V_{DDQ} V_{SSQ}	Supply	–	–	Isolated power supply and ground for the output buffers to provide improved noise immunity.

Operation Definition

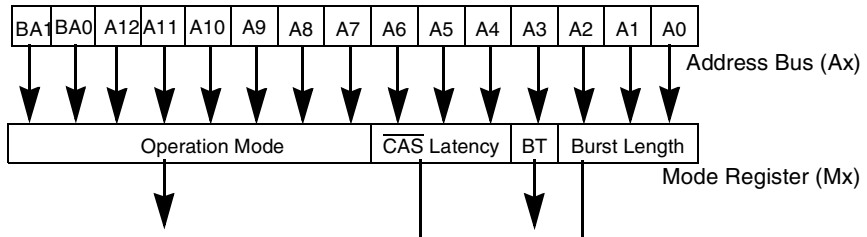
All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

Operation	Device State	CKE n-1	CKE n	DQM	BA0 BA1	AP= A10	Addr.	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Bank Active	Idle[3]	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active[3]	H	X	X	V	L	V	L	H	L	L
Write with Autoprecharge	Active[3]	H	X	X	V	H	V	L	H	L	L
Read	Active[3]	H	X	X	V	L	V	L	H	L	H
Read with Autoprecharge	Active[3]	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refr.)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Clock Suspend Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Entry (Precharge or active standby)	Idle	H	L	X	X	X	X	H	X	X	X
	Active[4]							L	H	H	H
Clock Suspend Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
								L	H	H	L
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes

1. V = Valid, x = Don't Care, L = Low Level, H = High Level
2. CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3. This is the state of the banks designated by BA0, BA1 signals.
4. Power Down Mode can not be entered in a burst cycle. When this command asserted in the burst mode cycle device is in clock suspend mode.

Mode Register Set Table



Operation Mode

M9	Mode
0	burst read / burst write
1	burst read / single write

Burst Type

M3	Type
0	Sequential
1	Interleave

$\overline{\text{CAS}}$ Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	
1	1	0	
1	1	1	

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed VDD+0.3V on any of the input pins or VDD supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

The Mode register designates the operation mode at the read or write cycle. This register is divided into four fields. First, a Burst Length Field which sets the length of the burst, Second, an Addressing Selection bit which programs the column access sequence in a burst cycle (interleaved or sequential). Third, a $\overline{CAS}$ Latency Field to set the access time at clock cycle. Fourth, an Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. After the initial power up, the mode set operation must be done before any activate command. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

Read and Write Operation

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a $\overline{RAS}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{CAS}$ cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, t_{RCD}, from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single $\overline{CAS}$ cycle, serial data read or write operations are allowed at up to a 166 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4 and 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the $\overline{CAS}$ timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organization and column addressing. Full page burst operation does not self

terminate once the burst length has been reached. In other words, unlike burst lengths of 2, 4 and 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAMs, burst read or write accesses on any column address are possible once the $\overline{RAS}$ cycle latches the sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycle is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be performed between different pages.

Burst Length and Sequence:

Burst Length	Starting Address (A2 A1 A0)	Sequential Burst Addressing (decimal)	Interleave Burst Addressing (decimal)
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	001	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	010	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	011	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	100	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	101	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	110	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	111	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page	nnn	Cn, Cn+1, Cn+2	not supported

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ -before-$\overline{RAS}$ refresh of conventional DRAMs. All banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. The mode restores the word lines after $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one tRC delay is required prior to any access command.

DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to "high" at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency t_{CSL}).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (trp) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (tref) of the device. Exit from this mode is performed by taking CKE "high". One clock delay is required for Power Down mode entry and exit.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the $\overline{CAS}$ timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. If CA10 is high when a Write Command is issued, the **Write with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to t_{WR} ("write recovery time") after the last data in.
A burst operation with Auto-Precharge may only be interrupted by a burst start to another bank. It must not be interrupted by a precharge or a burst stop command.

Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for $\overline{CAS}$ latency = 2 and two clocks before the last data out for $\overline{CAS}$ latency = 3. Writes require a time delay twr ("write recovery time") of 2 clocks minimum from the last data out to apply the precharge command.

Bank Selection by Address Bits

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	x	x	all Banks

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

Capacitance

T_A = 0 to 70 °C; V_{DD},V_{DDQ} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Values		Unit
		min.	max.	
Input capacitance (CLK)	C_{I1}	2.5	3.5	pF
Input capacitance (A0-A12, BA0,BA1,$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM)	C_{I2}	2.5	3.8	pF
Input / Output capacitance (DQ)	C_{IO}	4.0	6.0	pF

Note: Capacitance values are shown for TSOP-54 packages. Capacitance values for TFBGA packages are lower by 0.5 pF.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	– 1.0	4.6	V
Power supply voltage	V_{DD}, V_{DDQ}	– 1.0	4.6	V
Operating Temperature	T_A	0	+70	°C
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation per SDRAM component	P_D	–	1	W
Data out current (short circuit)	I_{OS}	–	50	mA

Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded.
Functional operation should be restricted to recommended operation conditions.
Exposure to higher than recommended voltage for extended periods of time affect device reliability

Recommended Operation Conditions and DC Eletrical Characteristics

T_A = 0 to 70 °C;

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply Voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1, 2
Input low voltage	V_{IL}	– 0.3	0	0.8	V	1, 2
Output high voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	–	V	1
Output low voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	–	0.4	V	1
Input leakage current, any input (0 V < V_{IN} < V_{DD}, all other inputs = 0 V)	I_{IL}	– 5	–	5	mA	
Output leakage current (DQs are disabled, 0 V < V_{OUT} < V_{DDQ})	I_{OL}	– 5	–	5	mA	

Notes:
1. All voltages are referenced to V_{SS}.
2. Vih may overshoot to V_{DDQ} + 2.0 V for pulse width of < 4ns with 3.3V. Vil may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

Operating Currents

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V

Parameter & Test Condition		Symb.	-6	-7	-7.5	-8		Note
			max.					
Operating Current One bank active, Burst length = 1	t_{RC} = $t_{RC(min)}$, Io = 0 mA	IDD1	100	80	80	80	mA	3, 4
Precharge Standby Current in Power Down Mode	$\overline{CS}$ =VIH (min.), CKE<=Vil(max)	IDD2P	2	2	2	2	mA	3
Precharge Standby Current in Non-Power Down Mode	$\overline{CS}$ = VIH (min.), CKE>=Vih(min)	IDD2N	35	30	30	25	mA	3
No Operating Current	$\overline{CS}$ = VIH(min), CKE>=VIH(min.)	IDD3N	40	35	35	30	mA	3
active state (max. 4 banks)	$\overline{CS}$ = VIH(min), CKE<=VIL(max.)	IDD3P	5	5	5	5	mA	3
Burst Operating Current Read command cycling		IDD4	110	90	90	70	mA	3, 4
Auto Refresh Current	t_{RFC}= $t_{RFC(min)}$	IDD5	220	190	190	160	mA	5
Auto Refresh command cycling	t_{RFC}= 7.8 µs		3	3	3	3	mA	
Self Refresh Current (standard components) Self Refresh Mode, CKE=0.2V, tck=infinity	x4, x8 x16	IDD6	3 1.5	3 1.5	3 1.5	3 1.5	mA mA	
Self Refresh Current (low power components) Self Refresh Mode, CKE=0.2V, tck=infinity	x8, x16	IDD6	0.85	0.85	0.85	0.85	mA	

Notes:
3. These parameters depend on the cycle rate. All values are measured at 166 MHz for "-6", at 133 MHz for "-7" and "-7.5" and at 100 MHz for "-8" components with the outputs open. Input signals are changed once during tck.
4. These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the VDDQ current is excluded.
5. t_{RFC}= $t_{RFC(min)}$ "burst refresh", t_{RFC}= 7.8 µs "distributed refresh".

AC Characteristics 1)2)

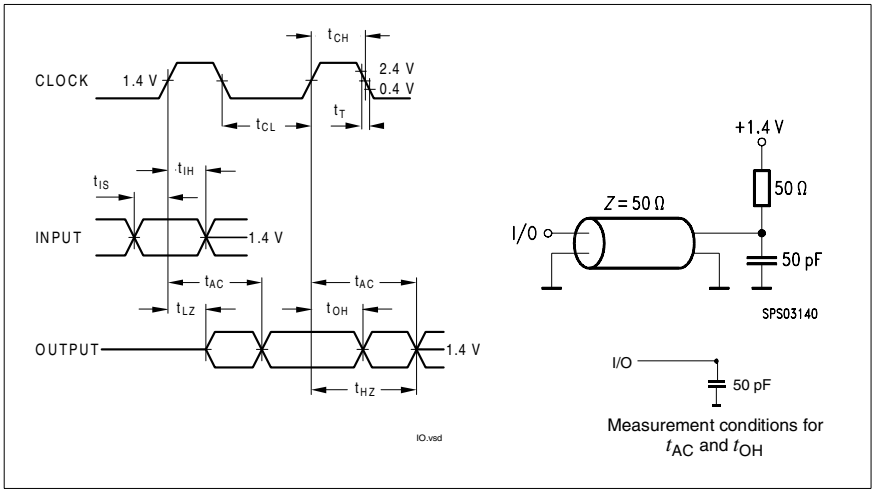
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V, tT = 1 ns

Parameter	Symbol	Limit Values								Unit	
		-6 PC166-333		-7 PC133-222		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.	min.	max.	min.	max.		
Clock and Clock Enable											
Clock Cycle Time											
CAS Latency = 3	t_{CK}	6	–	7	–	7.5	–	8	–	ns	
CAS Latency = 2		7.5	–	7.5	–	10	–	10	–	ns	
Clock Frequency											
CAS Latency = 3	t_{CK}	–	166	–	143	–	133	–	125	MHz	
CAS Latency = 2		–	133	–	133	–	100	–	100	MHz	
Access Time from Clock											
CAS Latency = 3	t_{AC}	–	5	–	5.4	–	5.4	–	6	ns	2, 3, 6
CAS Latency = 2		–	5.4	–	5.4	–	6	–	6	ns	
Clock High Pulse Width	t_{CH}	2	–	2.5	–	2.5	–	3	–	ns	
Clock Low Pulse Width	t_{CL}	2	–	2.5	–	2.5	–	3	–	ns	
Transition time	t_T	0.3	1.2	0.3	1.2	0.3	1.2	0.5	10	ns	
Setup and Hold Times											
Input Setup Time	t_{IS}	1.5	–	1.5	–	1.5	–	2	–	ns	4
Input Hold Time	t_{IH}	0.8	–	0.8	–	0.8	–	1	–	ns	4
CKE Setup Time	t_{CKS}	1.5	–	1.5	–	1.5	–	2	–	ns	4
CKE Hold Time	t_{CKH}	0.8	–	0.8	–	0.8	–	1	–	ns	4
Mode Register Set-up to Active delay	t_{RSC}	2	–	2	–	2	–	2	–	CLK	
Power Down Mode Entry Time	t_{SB}	0	6	0	7	0	7.5	0	8	ns	
Common Parameters											
Row to Column Delay Time	t_{RCD}	15	–	15	–	20	–	20	–	ns	5
Row Precharge Time	t_{RP}	15	–	15	–	20	–	20	–	ns	5
Row Active Time	t_{RAS}	36	100k	37	100k	45	100k	48	100k	ns	5
Row Cycle Time	t_{RC}	60	–	60	–	67	–	70	–	ns	5

Parameter	Symbol	Limit Values								Unit	
		-6 PC166-333		-7 PC133-222		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.	min.	max.	min.	max.		
Row Cycle Time during Auto Refresh	t_{RFC}	60		63		67		70		ns	
Activate(a) to Activate(b) Command period	t_{RRD}	12	–	14	–	15	–	16	–	ns	5
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command period	t_{CCD}	1	–	1	–	1	–	1	–	CLK	
Refresh Cycle											
Refresh Period (8192 cycles)	t_{REF}	–	64	–	64	–	64	–	64	ms	
Self Refresh Exit Time	t_{SREX}	1	–	1	–	1	–	1		CLK	
Read Cycle											
Data Out Hold Time	t_{OH}	2.5	–	3	–	3	–	3	–	ns	2, 6
Data Out to Low Impedance Time	t_{LZ}	0	–	0	–	0	–	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	6	3	7	3	7	3	8	ns	
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	–	2	–	2	CLK	
Write Cycle											
Last Data Input to Precharge (Write without AutoPrecharge)	t_{WR}	12	–	14	–	15	–	15	–	ns	7
Last Data Input to Activate (Write with AutoPrecharge)	$t_{DAL,min}$	(twr/tck) + (trp/tck)								CLK	8
DQM Write Mask Latency	t_{DQW}	0	–	0	–	0	–	0	–	CLK	

Notes

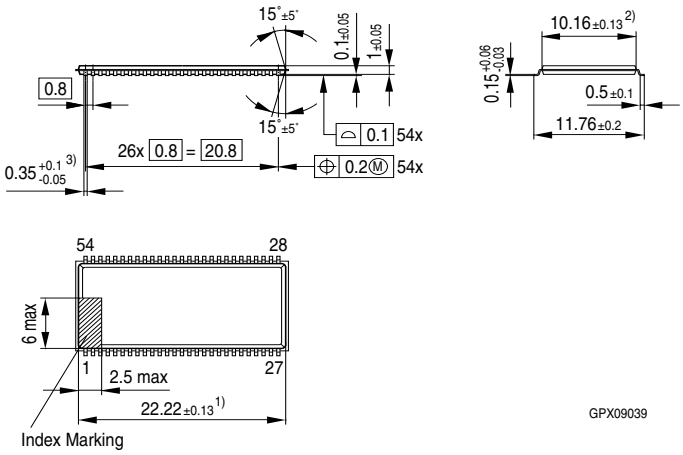
1. For proper power-up see the operation section of this data sheet.
2. AC timing tests for LV-TTL versions have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown in figure below. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with an input signal of 1V / ns edge rate between 0.8 V and 2.0 V.



3. If clock rising time is longer than 1 ns, a time (t_T/2 – 0.5) ns has to be added to this parameter.
4. If t_T is longer than 1 ns, a time (t_T – 1) ns has to be added to this parameter.
5. These parameter account for the number of clock cycles and depend on the operating frequency of the clock, as follows:
   the number of clock cycles = specified value of timing period (counted in fractions as a whole number)
6. Access time from clock t_{AC} is 4.6 ns for PC133 components with no termination and 0 pF load, Data out hold time t_{OH} is 1.8 ns for PC133 components with no termination and 0 pF load.
7. It is recommended to use two clock cycles between the last data-in and the precharge command in case of a write command without Auto-Precharge. One clock cycle between the last data-in and the precharge command is also supported, but restricted to cycle times tck greater or equal the specified twr value, where tck is equal to the actual system clock time
8. When a Write command with AutoPrecharge has been issued, a time of tdal(min) has be fullfilled before the next Activate Command can be applied. For each of the terms, if not already an integer, round up to the next highest integer. tck is equal to the actual system clock time.

Package Outlines - TSOP

Plastic Package P-TSOPII-54
(400 mil, 0.8 mm lead pitch)
Thin Small Outline Package, SMD



1) Does not include plastic or metal protrusion of 0.15 max per side
2) Does not include plastic protrusion of 0.25 max per side
3) Does not include dambar protrusion of 0.13 max per side

Package Outlines- TFBGA

TFBGA-54 package
(12 mm x 8 mm, 54 balls)