Digital Output Temperature Sensor with On-board SPD EEPROM

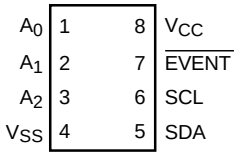
FEATURES

- **Class B (JC42.4) Temperature Sensor**
- **Supply Range: 3.0V to 3.6V**
- **I^2C /SMBus Interface**
- **DDR3 DIMM compliant SPD EEPROM**
- **Schmitt Triggers and Noise Suppression Filters on SCL and SDA Inputs**
- **Low Power CMOS Technology**
- **RoHS-compliant 2 x 3 x 0.75mm TDFN package**
- **Operates over the Extended Industrial Temperature Range**

For Ordering Information details, see page 19.

PIN CONFIGURATION

TDFN (VP2)
(2 x 3 x 0.75mm)



Note: For the location of Pin 1, please consult the corresponding package drawing.

PIN FUNCTIONS

Name	Description
A_0, A_1, A_2	Device Address Input
SDA	Serial Data Input/Output
SCL	Serial Clock Input
$\overline{EVENT}$	Open-drain Event Output
V_{CC}	Power Supply
V_{SS}	Ground

DESCRIPTION

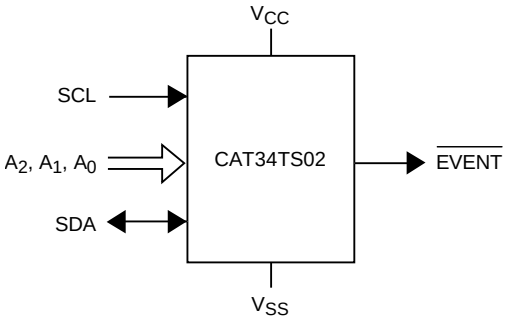
The CAT34TS02 combines a 12-bit (plus Sign bit) Digital Output Temperature Sensor (TS) with 2-Kb of Serial Presence Detect (SPD) EEPROM.

The TS measures temperature aproximately 10 times every second. Temperature readings can be retrieved by the host via the I^2C/SMBus interface, and are compared to several trigger limits stored into internal registers. Over and under limit conditions are signaled on the open-drain $\overline{EVENT}$ pin.

The integrated 2-Kb SPD EEPROM is internally organized as 16 pages of 16 bytes each, for a total of 256 bytes. It features a 16-byte page write buffer and supports both the Standard (100kHz) as well as Fast (400kHz) I^2C™ protocol.

Write operations to the lower half memory can be inhibited via software commands. The CAT34TS02 features Permanent, as well as Reversible Software Write Protection, as defined for DDR3 DIMMs.

FUNCTIONAL SYMBOL



ABSOLUTE MAXIMUM RATINGS[1]

Operating Temperature	-45°C to +130°C
Storage Temperature	-65°C to +150°C
Voltage on any pin with respect to Ground[2]	-0.5V to +6.5V

RELIABILITY CHARACTERISTICS[3]

Symbol	Parameter	Min	Units
N_{END}[4]	Endurance (EEPROM)	1,000,000	Write Cycles
T_{DR}	Data Retention (EEPROM)	100	Years

TEMPERATURE CHARACTERISTICS

T_A = −20°C to +125°C, V_{CC} = 3.0 V to 3.6 V, unless otherwise specified

Parameter	Test Conditions/Comments	Max	Unit
Temperature Reading Error Class B, JC42.4 compliant	75°C ≤ T_A ≤ 95°C, active range	+/- 1.0	°C
	40°C ≤ T_A ≤ 125°C, monitor range	+/- 2.0	°C
	-20°C ≤ T_A ≤ 125°C, sensing range	+/- 3.0	°C
ADC Resolution		12	Bits
Temperature Resolution		0.0625	°C
Temperature Conversion Time		100	ms
Thermal Resistance[3] θ_{JA}	Junction-to-Ambient (Still Air)	92	ºC/W

D.C. OPERATING CHARACTERISTICS

T_A = −20°C to +125°C, V_{CC} = 3.0V to 3.6V

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
I_{CC1}	Supply Current	TS Converting; EEPROM idle		200	µA
I_{SHDN}	Supply Current	TS shut-down; EEPROM idle		5	µA
I_{CC2}	Supply Current	EEPROM Read; TS shut-down		0.5	mA
I_{CC3}	Supply Current	EEPROM Write; TS shut-down		1	mA
I_L	I/O Pin Leakage Current	Pin at GND or V_{CC}		5	µA
V_{IL}	Input Low Voltage		-0.5	0.2 x V_{CC}	V
V_{IH}	Input High Voltage		0.8 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} > 2.5V		0.4	V
ΔV_{HV}	A_0 Overdrive (V_{HV} - V_{CC})	1.7 V < V_{CC} < 3.6 V	4.8		V
I_{HVD}	A_0 High Voltage Detector Current			0.1	mA
V_{HV}	A_0 Very High Voltage		7	10	V

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The DC input voltage on any pin should not be lower than -0.5V or higher than V_{CC} + 0.5V. During transitions, the voltage on any pin may undershoot to no less than -1.5V or overshoot to no more than V_{CC} + 1.5V, for periods of less than 20 ns.

(3) Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where T_J is the junction temperature and T_A is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2-layer PCB.

(4) Page Mode, V_{CC} = 5.0V, 25°C

A.C. CHARACTERISTICS[1]

T_A = −20°C to +125°C, V_{CC} = 3.0V to 3.6V

Symbol	Parameter	Min	Max	Units
F_{SCL}	Clock Frequency	10[2]	400	kHz
$t_{HD:STA}$	START Condition Hold Time	0.6		µs
t_{LOW}	Low Period of SCL Clock	1.3		µs
t_{HIGH}	High Period of SCL Clock	0.6		µs
$t_{SU:STA}$	START Condition Setup Time	0.6		µs
$t_{HD:DAT}$	Data Hold Time	0		ns
$t_{SU:DAT}$	Data Setup Time	100		ns
t_R	SDA and SCL Rise Time		300	ns
t_F[1]	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	0.6		µs
t_{BUF}	Bus Free Time Between STOP and START	1.3		µs
t_{AA}	SCL Low to SDA Data Out		0.9	µs
t_{DH}	Data Out Hold Time	100		ns
T_i[1]	Noise Pulse Filtered at SCL and SDA Inputs		50	ns
t_{WR}	Write Cycle Time		5	ms
t_{PU}[4]	Power-up to Ready Mode		100	ms
$t_{D:SMB}$[2]	SMBus Time-Out (Maximum SCL LOW Time)		10	ms

A.C. TEST CONDITIONS

Input Drive Levels	$0.2V_{CC}$ to $0.8V_{CC}$
Input Rise and Fall Time	< 50ns
Input Reference Levels	$0.25V_{CC}$, $0.75V_{CC}$
Output Reference Level	$0.5V_{CC}$
Output Test Load	I_{OL} = 3mA (V_{CC} > 2.5V); I_{OL} = 1mA (V_{CC}<2.5V); C_L = 100pF

PIN IMPEDANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.0V to 3.6V, f = 100kHz, unless otherwise specified

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
C_{IN}[3	SDA, $\overline{EVENT}$ Pin Capacitance	V_{IN} = 0		8	pF
C_{IN}[3]	Input Capacitance (other pins)	V_{IN} = 0		6	pF

Notes:

(1) Test Conditions according to A.C. TEST CONDITIONS Table.

(2) The TS interface will release the bus after the SMBus time-out of 10ms. The SPD interface has no time-out.

(3) These parameters are tested initially and after a design or process change that affects the parameter.

(4) A valid temperature reading can not be expected sooner than approx. 100ms after V_{cc} reaches the nominal value of 3.0V.

PIN DESCRIPTION

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

SDA: The Serial Data I/O pin receives input data and transmits data stored in the internal registers. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address pins set the device address. These pins have on-chip pull-down resistors and will default to an address of 000 if left unconnected.

$\overline{\text{EVENT}}$: The open-drain $\overline{\text{EVENT}}$ pin can be programmed to signal over/under temperature limit conditions.

POWER-ON RESET (POR)

The CAT34TS02 incorporates Power-On Reset (POR) circuitry which monitors the supply voltage, and then resets (initializes) the internal state machines below (above) a POR trigger level of approximately 1.2 V, i.e. well below the minimum recommended V_{CC} value.

The TS component will power-up into conversion mode, while the SPD EEPROM component will power-up into Standby mode.

The internal state machines will operate properly above the POR trigger level, but valid temperature readings can be expected only after the first conversion cycle under nominal bias conditions.

DEVICE INTERFACE

The CAT34TS02 supports the Inter-Integrated Circuit (I^2C) and the System Management Bus (SMBus) data transmission protocols. These protocols describe serial communication between transmitters and receivers sharing a 2-wire data bus. Data flow is controlled by a Master device, which generates the serial clock and the START and STOP conditions. The CAT34TS02 acts as a Slave device. Master and Slave alternate as transmitter and receiver. Up to 8 CAT34TS02 devices may be present on the bus simultaneously, and can be individually addressed by matching the logic state of the address inputs A0, A1, and A2.

I^2C/SMBUS PROTOCOL

The I^2C/SMBus uses two 'wires', one for clock (SCL) and one for data (SDA). The two wires are connected to the V_{CC} supply via pull-up resistors. Master and Slave devices connect to the bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 1).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all Slaves. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP tells the Slave that no more data will be written to or read from the Slave.

DEVICE ADDRESSING

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address (the preamble) select either the Temperature Sensor (TS) registers (0011) or the EEPROM memory contents (1010), as shown in Figure 2. The next 3 bits, A2, A1 and A0, select one of 8 possible Slave devices. The last bit, R/$\overline{\text{W}}$, specifies whether a Read (1) or Write (0) operation is being performed

ACKNOWLEDGE

A matching Slave address is acknowledged (ACK) by the Slave by pulling down the SDA line during the 9^{th} clock cycle (Figure 3). After that, the Slave will acknowledge all data bytes sent to the bus by the Master. When the Slave is the transmitter, the Master will in turn acknowledge data bytes in the 9^{th} clock cycle. The Slave will stop transmitting after the Master does not respond with acknowledge (NoACK) and then issues a STOP. Bus timing is illustrated in Figure 4.

Figure 1. Start/Stop Timing

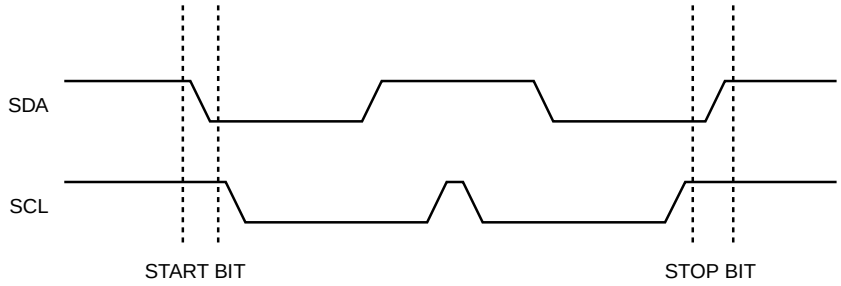


Figure 2. Slave Address Bits

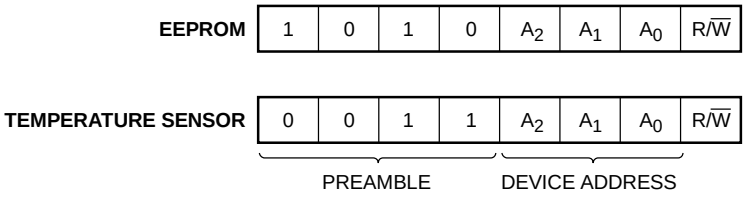


Figure 3. Acknowledge Timing

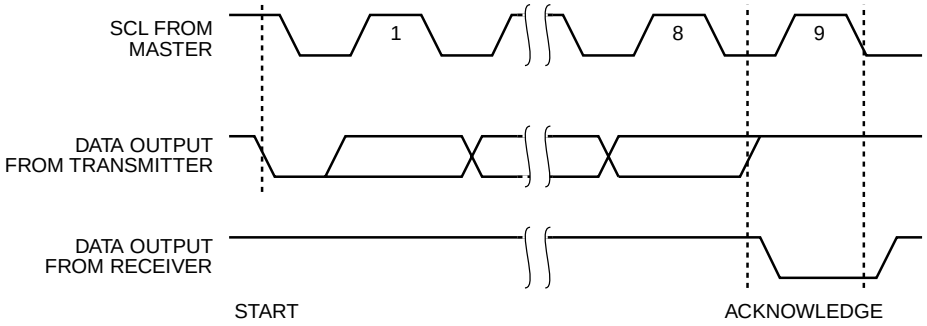
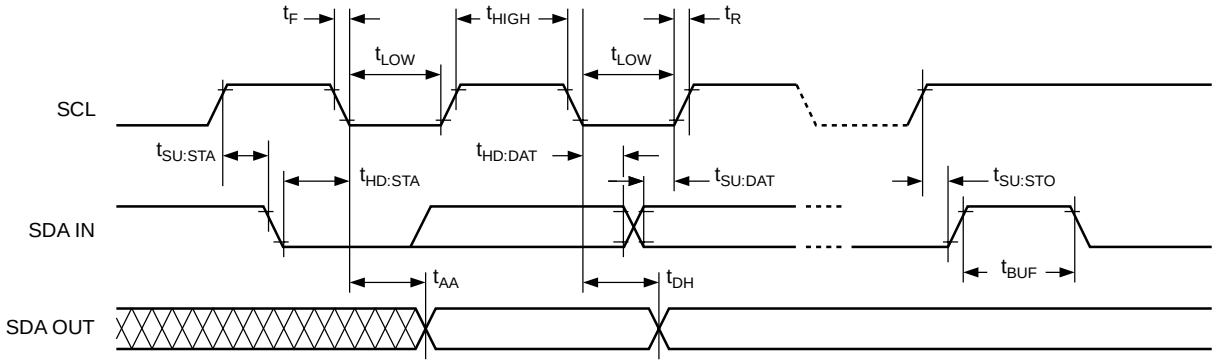


Figure 4. Bus Timing



WRITE OPERATIONS

EEPROM Byte and TS Register Write

To write data to a TS register, or to the on-board EEPROM, the Master creates a START condition on the bus, and then sends out the appropriate Slave address (with the R/$\overline{W}$ bit set to '0'), followed by an address byte and data byte(s). The matching Slave will acknowledge the Slave address, EEPROM byte or TS register address and the data byte(s), one for EEPROM data (Figure 5) and two for TS register data (Figure 6). The Master then ends the session by creating a STOP condition on the bus. The STOP completes the (volatile) TS register update or starts the internal Write cycle for the (non-volatle) EEPROM data (Figure 7).

EEPROM Page Write

The on-board EEPROM contains 256 bytes of data, arranged in 16 pages of 16 bytes each. A page is selected by the 4 most significant bits of the address byte immediatelly following the Slave address, while the 4 least significant bits point to the byte within the page. Up to 16 bytes can be written in one Write cycle (Figure 8).

The internal EEPROM byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 16 data bytes, then earlier data will be overwritten by later data in a 'wrap-around' fashion within the selected page. The internal Write cycle, using the most recently loaded data, then starts immediatelly following the STOP.

Acknowledge Polling

Acknowledge polling can be used to determine if the CAT34TS02 is busy writing to EEPROM, or is ready to accept commands. Polling is executed by interrogating the device with a 'Selective Read' command (see READ OPERATIONS). The CAT34TS02 will not acknowlwdge the Slave address as long as internal EEPROM Write is in progress.

DELIVERY STATE

The CAT34TS02 is shipped 'unprotected', i.e. neither SWP flag is set. The entire 2-Kb memory is erased, i.e. all bytes are FFh.

Figure 5. EEPROM Byte Write

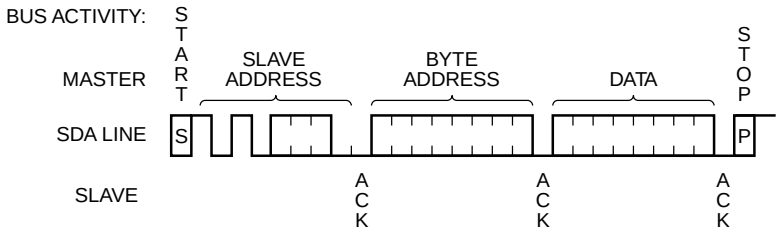


Figure 6. Temperature Sensor Register Write

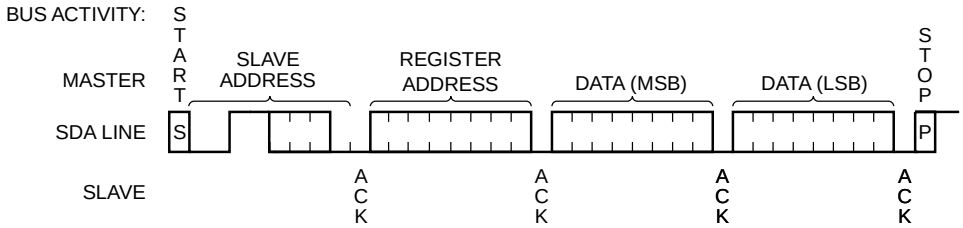


Figure 7. EEPROM Write Cycle Timing

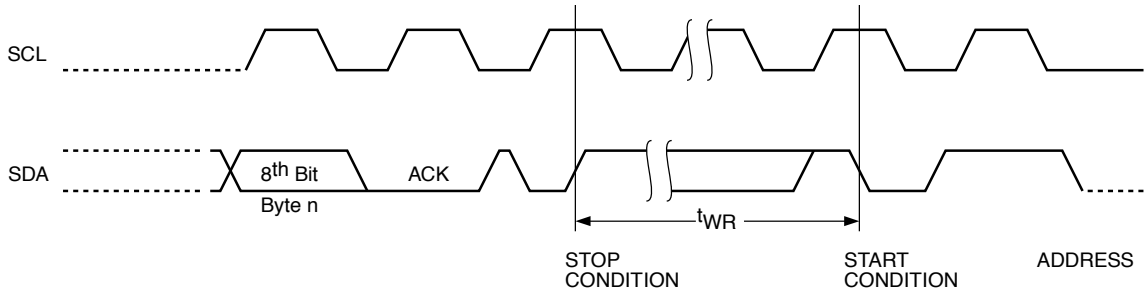
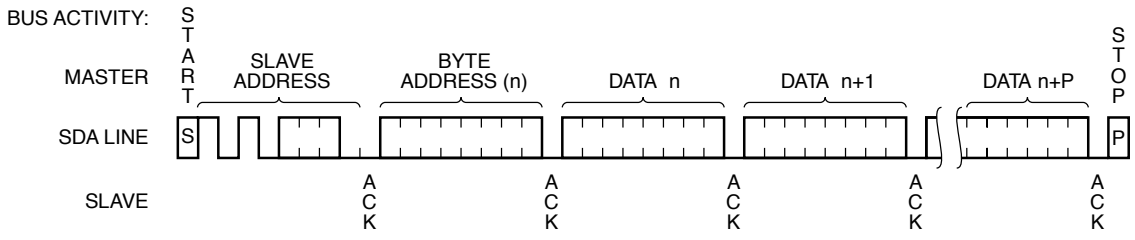


Figure 8. EEPROM Page Write



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

READ OPERATIONS

Immediate Read

Upon power-up, the address counters for both the Temperature Sensor (TS) and on-board EEPROM are initialized to 00h. The TS address counter will thus point to the Capability Register and the EEPROM address counter will point to the first location in memory. The two address counters may be updated by subsequent operations.

A CAT34TS02 presented with a Slave address containing a '1' in the R/$\overline{W}$ position will acknowledge the Slave address and will then start transmitting data being pointed at by the current EEPROM data or respectively TS register address counter. The Master stops this transmission by responding with NoACK, followed by a STOP (Figure 9),.

Selective Read

The Read operation can be started at an address different from the one stored in the respective address counters, by preceeding the Immediate Read sequence with a 'data less' Write operation. The Master sends out a START, Slave address and address byte, but rather than following up with data (as in a Write operation), the Master then issues another START and continuous with an Immediate Read sequence (Figure 10).

Sequential EEPROM Read

EEPROM data can be read out indefinitely, as long as the Master responds with ACK (Figure 11). The internal address count is automatically incremented after every data byte sent to the bus. If the end of memory is reached during continuous Read, then the address counter 'wraps-around' to beginning of memory, etc. Sequential Read works with either Immediate Read or Selective Read, the only difference being that in the latter case the starting address is intentionally updated.

Figure 9. Immediate Read

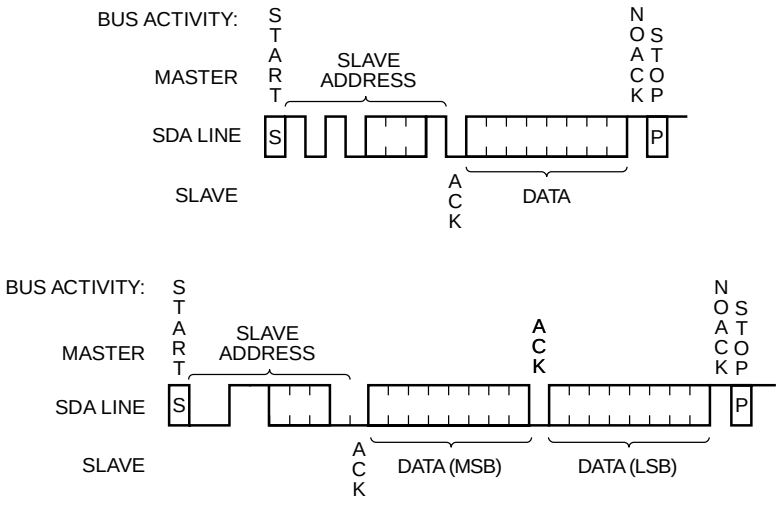


Figure 10. Selective Read

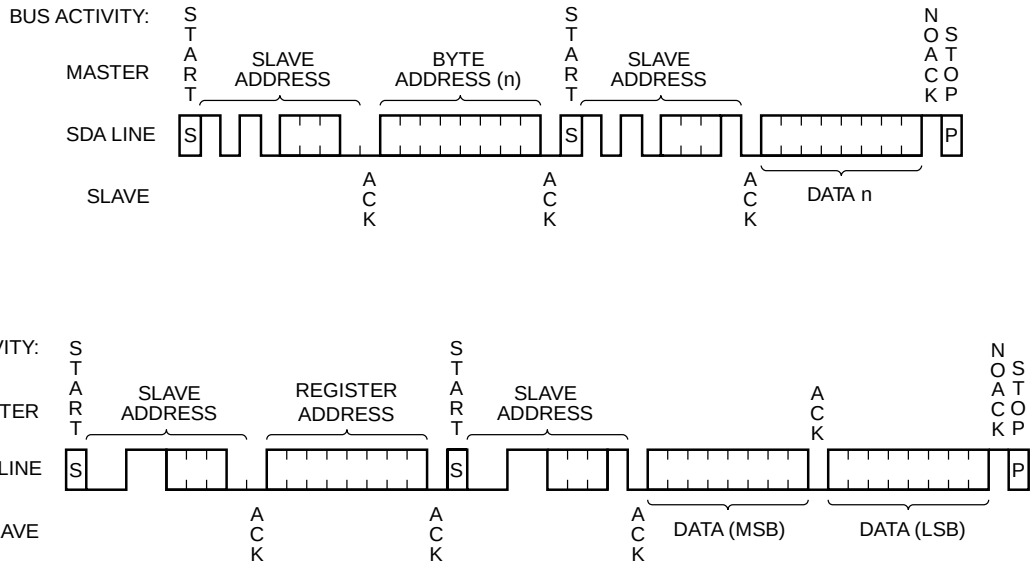
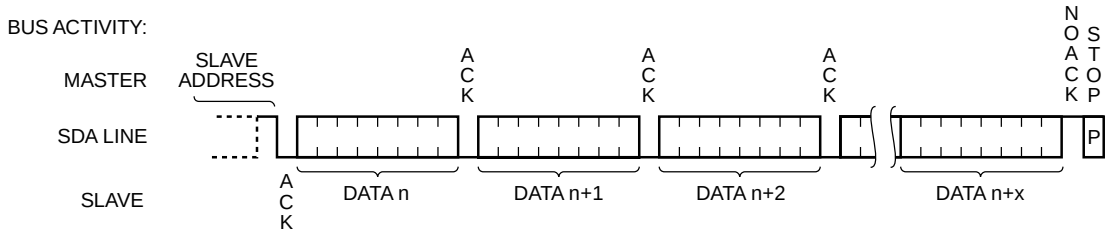


Figure 11. EEPROM Sequential Read



SOFTWARE WRITE PROTECTION

The lower half of memory (first 128 bytes) can be protected against Write requests by setting one of two Software Write Protection (SWP) flags.

The Permanent Software Write Protection (PSWP) flag can be set or read while all address pins are at regular CMOS levels (GND or V_{CC}), whereas a very high voltage V_{HV} must be present on address pin A0 to set, clear or read the Reversible Software Write Protection (**RSWP**) flag. The D.C. OPERATING CONDITIONS for RSWP operations are shown in Table 1.

The SWP commands are listed in Table 2. All commands are preceded by a START and terminated with a STOP, following the ACK or NoACK from the CAT34TS02. All SWP related Slave addresses use the pre-amble: 0110 (6h), instead of the regular 1010 (Ah) used for memory access. For **PSWP** commands, the three address pins can be at any logic level, whereas for **RSWP** commands the address pins must be at pre-assigned logic levels.

V_{HV} is interpreted as logic '1'. The V_{HV} condition must be established on pin A0 before the START and maintained just beyond the STOP. Otherwise an RSWP request could be interpreted by the CAT34TS02 as a PSWP request.

The SWP Slave addresses follow the standard I^2C convention, i.e. to read the state of the SWP flag, the LSB of the Slave address must be '1', and to set or clear a flag, it must be '0'. For Write commands a dummy byte address and dummy data byte must be provided (Figure 12). In contrast to a regular memory Read, a SWP Read does not return Data. Instead the CAT34TS02 will respond with NoACK if the flag is set and with ACK if the flag is not set. Therefore, the Master can immediately follow up with a STOP, as there is no meaningful data following the ACK interval (Figure 13).

Table 1: RSWP D.C. Operation Condition

Symbol	Parameter	Test Conditions	Min	Max	Units
ΔV_{HV}	A_0 Overdrive (V_{HV} - V_{CC})	1.7 V < V_{CC} < 3.6 V	4.8		V
I_{HVD}	A_0 High Voltage Detector Current			0.1	mA
V_{HV}	A_0 Very High Voltage		7	10	V

Table 2. SWP Commands

Command	Address Pin Levels[1]			Prior Flag State[2]		Slave Address[3]					ACK	Address Byte	ACK	Data Byte	ACK	Internal Write Cycle
	A_2	A_1	A_0	PSWP	RSWP	b7 to b4	b3	b2	b1	b0						
Set/ Check PSWP	A_2	A_1	A_0	0	X	0110	A_2	A_1	A_0	0	YES	X	YES	X	YES	YES
	A_2	A_1	A_0	0	X		A_2	A_1	A_0	1	YES					
Set/ Check RSWP	V_{IL}	V_{IL}	V_{HV}	0	0		0	0	1	0	YES	X	YES	X	YES	YES
	V_{IL}	V_{IL}	V_{HV}	0	0		0	0	1	1	YES					
	V_{IL}	V_{IL}	V_{HV}	0	1		0	0	1	X	NO					
Clear/ Check RSWP[4]	V_{IL}	V_{IH}	V_{HV}	0	X		0	1	1	0	YES	X	YES	X	YES	YES
	V_{IL}	V_{IH}	V_{HV}	0	X		0	1	1	1	YES					
Any[5]	X	X	X	1	X		X	X	X	X	NO					

Figure 12. Software Write Protect (Write)

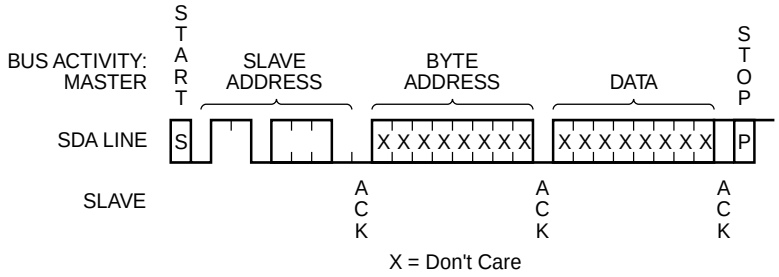
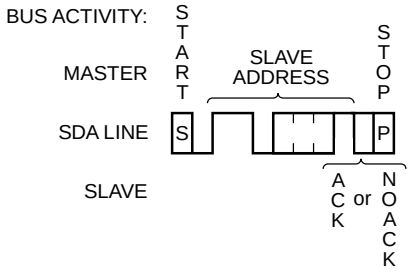


Figure 13. Software Write Protect (Read)



Notes:
(1) Entries shown as A_2, A_1 and A_0 are either at V_{IH} or at V_{IL}.
(2) This is the state of the SWP flags prior to applying the SWP command.
(3) Here A_2, A_1 and A_0 reflect the logic state corresponding to the respective physical pin inputs.
(4) The Read command (b0 = 1), simply confirms that the RSWP flag can be cleared.
(5) Once the PSWP flag is set, the device will respond to any SWP command with NoACK.

TEMPERATURE SENSOR OPERATION

The TS component in the CAT34TS02 combines a Proportional to Absolute Temperature (PTAT) sensor with a ∑-Δ modulator, yielding a 12 bit (13 bit including sign) digital temperature representation.

The TS is free running on an internal clock, and starts a conversion cycle at least every 100ms. The result of the conversion is stored in the **Temperature Value** (**TV**) **Register**. While a conversion is in progress, attempts at reading the **TV** register will yield temperature values corresponding to the previous conversion. **TV** register contents are saved during Shut-down periods.

At the end of the conversion cycle, the value stored in the **TV** register is compared against limit values stored in the **Alarm Temperature Upper Boundary Trip,** the **Alarm Temperature Lower Boundary Trip** and **Critical Temperature Trip** registers. If the measured value is outside the boundary limits or above the critical limit, then the $\overline{\text{EVENT}}$ pin may be activated. The $\overline{\text{EVENT}}$ output function is programmable, via the **Configuration Register** for interrupt mode, comparator mode and polarity.

The temperature limit registers can be Read or Written by the host, via the serial interface. At power-on, these registers are initialized to default values, and should be updated by the host to the desired values.

REGISTERS

The CAT34TS02 contains eight 16-bit wide registers allocated to TS functions, as shown in Table 3. Upon power-up, the internal address counter points to the capability register.

Capability Register (User Read Only)

This register lists the capabilities of the TS, as detailed in the corresponding bit map.

Configuration Register (Read/Write)

This register controls the various operating modes of the TS, as detailed in the corresponding bit map.

Temperature Trip Point Registers (Read/Write)

The CAT34TS02 features 3 temperature limit registers. They are the Alarm Temperature Upper Boundary Trip register, the Alarm Temperature Lower Boundary Trip register, and the Critical Temperature Trip register. The **TV** register contents are compared to the various limit values, and the resulting event may be used to activate the $\overline{\text{EVENT}}$ pin. To avoid superfluous $\overline{\text{EVENT}}$ pin activity, this pin can be disabled while updating the limit registers. The pin may be re-enabled, as soon as a valid comparison can be expected. The format of the limit registers is detailed in the corresponding bit maps. Data format is two's complement with the LSB representing 0.25°C.

Testing Temperature Trip Point Operation

A common technique for verifying temperature trip points and operation of the upper, lower and critical temperature threshold limits is to maintain a fixed temperature and 'sweep' the trigger limits.

This completely digital technique is faster when compared to raising and/or lowering the device temperature itself (as would happen during normal operation). In the present implementation of the CAT34TS02, this method may yield false results, since the various flag bits representing the relation between actual temperature and limit values, are updated only at the end of a conversion cycle, rather than all the time. Therefore, the flag bits may take on the correct value as late as perhaps 100 ms after the limit registers have been reset and an attempt at reading the TV register is made. Automated programs used in testing temperature sensors would need to take this delay into account in order to produce meaningful results.

Temperature Value Register (User Read Only)

This register stores the trip status and the temperature measured by the TS, as detailed in the corresponding bit map. The temperature is stored in a 13-bit, two's complement format, with the MSB (D12) representing the sign. The next bit (D11) represents 128°C, and the LSB (D0) represents 0.0625°C. D15, D14 and D13 are the trip status bits, representing the internal temperature trip detection and are not affected by the status of the event or configuration bits. When both the above' (D14) and the 'below' (D13) bits are '0', the current temperature reading is within alarm window boundaries, as defined in the configuration register.

Device ID and Revision Register (Read Only)

The manufacturer assigns the device ID and device revision. The device revision starts at 0 and is incremented by 1 whenever the manufacturer issues an update to the device. The format of this register is detailed in the corresponding bit map.

Table 3: The TS Registers

Register Address	Register Name	Power-On Default	Read/Write
0x00	Capability Register	0x001F	Read
0x01	Configuration Register	0x0000	Read/Write
0x02	Alarm Temperature Upper Boundary Trip Register	0x0400	Read/Write
0x03	Alarm Temperature Lower Boundary Trip Register	0x00A0	Read/Write
0x04	Critical Temperature Trip Register	0x0500	Read/Write
0x05	Temperature Value Register	Undefined	Read
0x06	Manufacturer ID Register	0x1B09	Read
0x07	Device ID/Revision Register	0x080X	Read
0x07	Device ID/Revision Register	0x080X	Read
0x08 – 0xFF(1)	Reserved	–	–

CAPABILITY REGISTER

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	Resolution		Range	Accuracy	Trip Mode

Bit	Description
D0	1: Alarm and Critical Temperature
D1	1: ±1°C over the active range and ±2°C over the monitor range (Class B)
D2	1: Positive and Negative Temperature
D4:D3	11: LSB = 0.0625°C
D15:D5	Reserved for future use; must be 0

Notes:

(1) Attempts to read from register addresses 0x08 - 0xFF will return NoACK and the content of the last accessed register is output as data. If no register was accessed (read or written) after power-up, the content of the Capability Register (address 0x00, value 0x001F) is output.

CONFIGURATION REGISTER

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Hysteresis		Shut-down mode	Critical lock bit	Alarm lock bit	Clear event	Event output status	Event output control	Critical event only	Event polarity	Event mode

Bit	Description
D0 (1)	0: Comparator mode (default) 1: Interrupt mode
D1 (1)	0: Active low (default) 1: Active high.
D2 (1)	0: EVENT output triggered by alarm or critical temperature event (default) 1: EVENT output triggered by critical temperature event only
D3 (1)	0: EVENT output disabled (default) 1: EVENT output enabled
D4 (2)	0: EVENT output pin is not being asserted (default) 1: EVENT output pin is being asserted as a result of an alarm or a critical temperature event
D5 (3)	0: No effect (default) 1: Clears an active event in interrupt mode only
D6 (4)	0: Alarm trip registers can be altered (default) 1: Alarm trip registers cannot be altered
D7 (4)	0: Critical trip register can be altered (default) 1: Critical trip register cannot be altered
D8 (4), (5)	0: Thermal Sensor (TS) enabled (default) 1: Thermal Sensor (TS) shut down
D10:D9	00: Disable hysteresis (default) 01: Set hysteresis at 1.5°C 10: Set hysteresis at 3°C 11: Set hysteresis at 6°C

Notes:
(1) Can not be written as long as either one of the two lock bits (D6 or D7) is set.
(2) The actual cause of an event can be determined by reading the temperature value registers. Interrupt events can be cleared by writing to the clear event bit (D5). This is a read-only bit.
(3) Writing to this bit has no effect in comparator mode. When read, this bit always returns 0. Once the DUT temperature is greater than the critical temperature, an event cannot be cleared (see Figure 5).
(4) Cleared at power-on reset (POR). Once set, this bit can only be cleared by a POR condition.
(5) When the device is shut down, both the band-gap and the ADC are disabled to save power, and no events are generated. Attempts to set this bit are ignored, as long as either one of the two lock bits (D6 or D7) is set. However, the bit can be cleared at any time.

ALARM TEMPERATURE UPPER BOUNDARY TRIP REGISTER

			Sign MSB										LSB		
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	Alarm window upper boundary temperature											0	0

ALARM TEMPERATURE LOWER BOUNDARY TRIP REGISTER

			Sign MSB										LSB		
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	Alarm window lower boundary temperature											0	0

CRITICAL TEMPERATURE TRIP REGISTER

			Sign MSB										LSB		
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	Critical temperature											0	0

TEMPERATURE VALUE REGISTER

			Sign MSB												LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Above critical trip	Above alarm window	Below alarm window	Temperature												

Bit	Description
D13	0: Temperature is equal to or above the alarm window lower boundary temperature 1: Temperature is below the alarm window lower boundary temperature
D14	0: Temperature is equal to or below the alarm window upper boundary temperature. 1: Temperature is above the alarm window upper boundary temperature
D15	0: Temperature is below the critical temperature setting 1: Temperature is equal to or above the critical temperature setting

REGISTER DATA FORMAT

The values used in the temperature value register and the 3 temperature trip point registers are expressed in two's complement format. The measured temperature value is expressed with 12-bit resolution, while the 3 trip temperature limits are set with 10-bit resolution. The total temperature range is arbitrarily defined as 256°C, thus yielding an LSB of 0.0625°C for the measured temperature and 0.25°C for the 3 limit settings. Bit D12 in all temperature registers represents the sign, with a '0' indicating a positive, and a '1' a negative value. In two's complement format, negative values are obtained by complementing their positive counterpart and adding a '1', so that the sum of opposite signed numbers, but of equal absolute value, adds up to zero.

Note that trailing '0' bits, are '0' irrespective of polarity. Therefore the don't care bits (D1 and D0) in the 10-bit resolution temperature limit registers, are always '0'. Also note that temperatures below −20°C will produce erroneous readings.

12-Bit Temperature Data Format

Binary (D12 to D0)	Hex	Temperature
1 1110 1100 0000	1EC0	−20°C
1 1111 1111 1111	1FFF	−0.0625°C
0 0000 0000 0000	000	0°C
0 0000 0000 0001	001	+0.0625°C
0 0001 1001 0000	190	+25°C
0 0011 0010 0000	320	+50°C
0 0111 1101 0000	7D0	+125°C

EVENT PIN FUNCTIONALITY

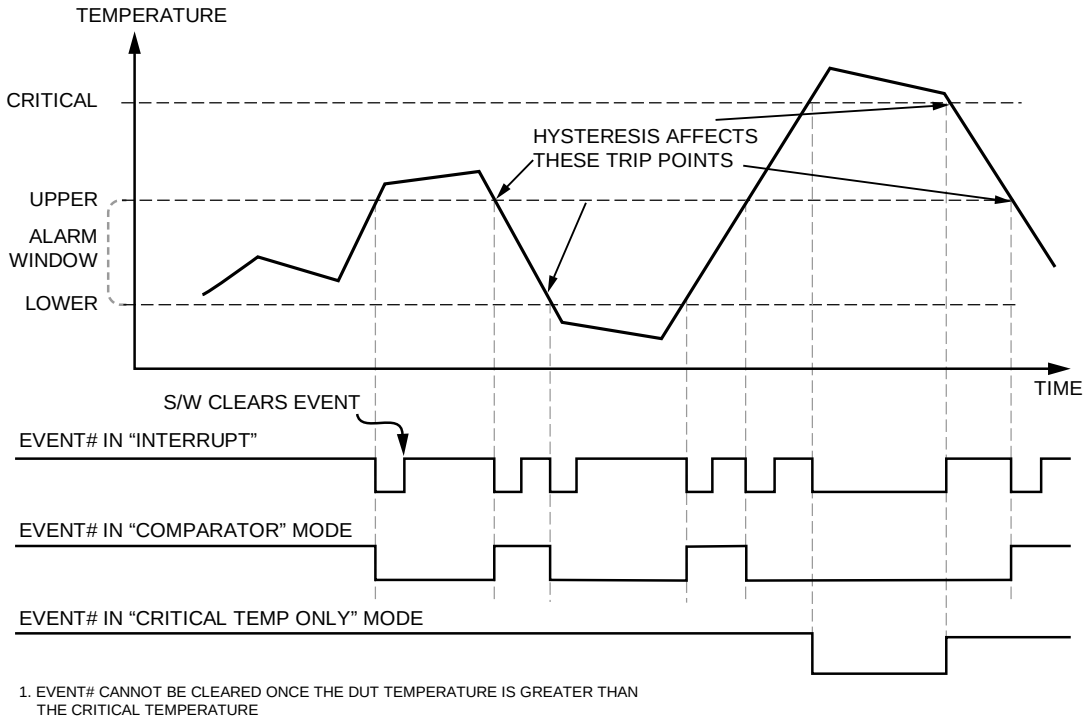
The $\overline{\text{EVENT}}$ output reacts to temperature changes as illustrated in Figure 14, and according to the operating mode defined by the Configuration register.

In **Interrupt Mode** the $\overline{\text{EVENT}}$ output can be asserted every time the temperature crosses one of the alarm window limits, and can be de-asserted by writing a '1' to the clear event bit in the configuration register. When the temperature exceeds the critical limit, the device switches to comparator mode and $\overline{\text{EVENT}}$ remains asserted as long as the temperature stays above the critical limit (setting the clear event bit will have no effect in this case). When the temperature drops below the critical limit, the device switches back to either interrupt or comparator mode, as programmed in the configuration register.

In **Comparator Mode**, the $\overline{\text{EVENT}}$ output is asserted outside the alarm window limits, while in **Critical Temperature Mode**, $\overline{\text{EVENT}}$ is asserted only above the critical limit. The exact trip limits are determined by the 3 temperature limit settings and the hystersis offsets, as dictated by the corresponding Configuration register bits (see also Figure 15).

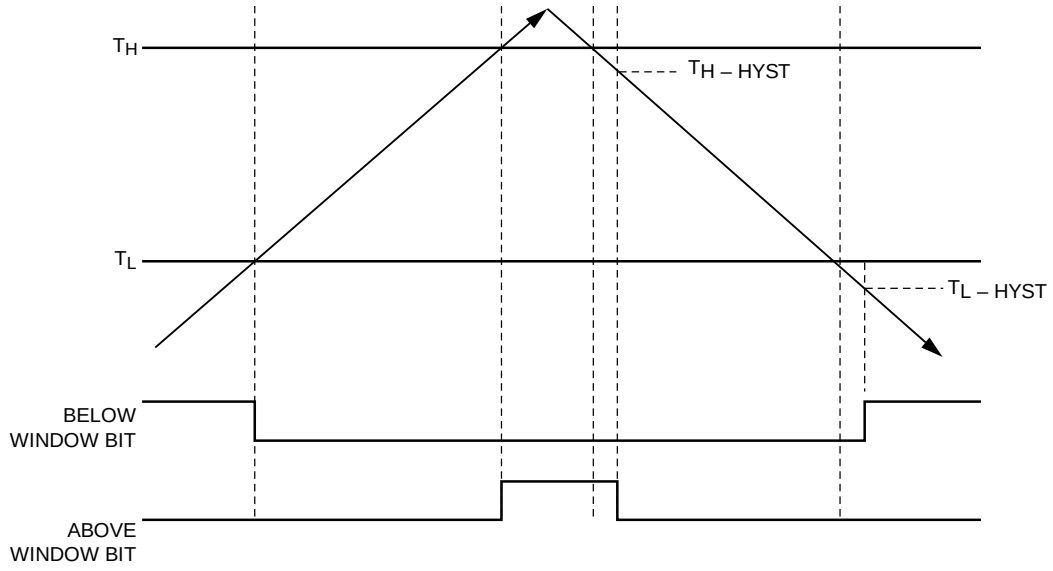
The $\overline{\text{EVENT}}$ output will retain the state preceding a shut-down command.

Figure 14. Event Detail



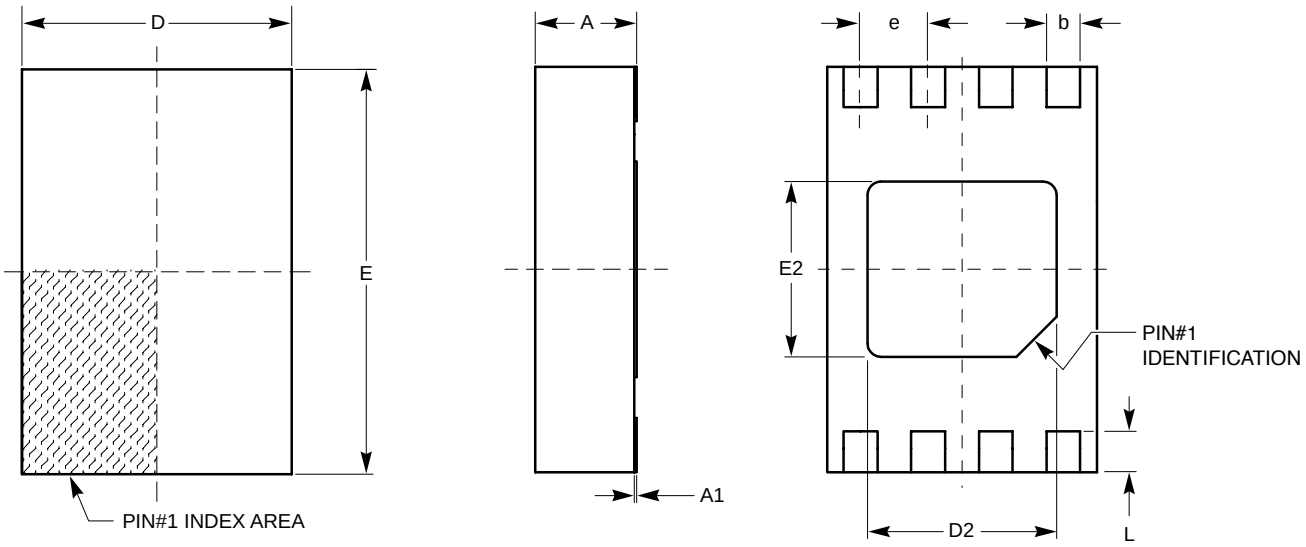
1. EVENT# CANNOT BE CLEARED ONCE THE DUT TEMPERATURE IS GREATER THAN THE CRITICAL TEMPERATURE

Figure 15. Hysteresis Detail

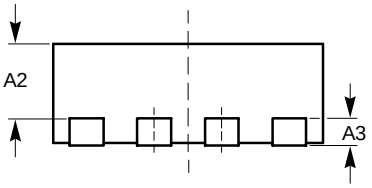


PACKAGE OUTLINE DRAWING

TDFN 8-PAD 2 X 3MM (VP2)[1][2]



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**



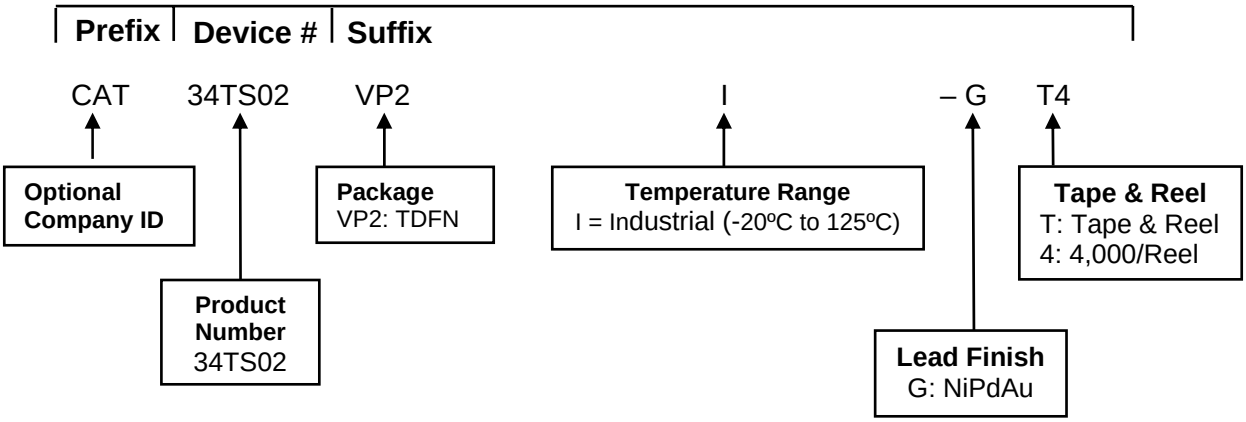
FRONT VIEW

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e		050 TYP	
L	0.20	0.30	0.40

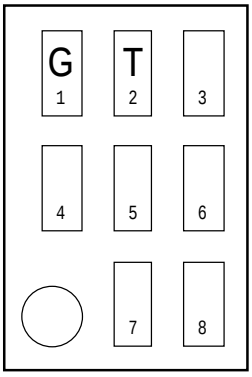
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC specification MO-229.

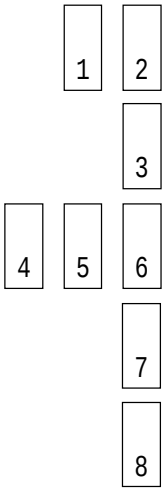
EXAMPLE OF ORDERING INFORMATION



TOP MARK CODES



Top Mark Legend (Position)



Mark “GT”.

Assembly location code (1 digit; “S” is for STARS Microelectronics-Thailand)

Last three digits of assembly lot number.

Production year (last digit).

Production month (1 - 9, A, B, C).

Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu.

(3) This device used in the above example is a CAT34TS02VP2I-GT4 (i.e. TDFN, Industrial Temperature, NiPdAu, Tape & Reel, 4,000/Reel).

(4) For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

REVISION HISTORY

Date	Revision	Description
06-Aug-08	A	Initial Issue
15-Aug-08	B	Update Power-On Reset, Temperature Sensor Operation and Register
04-Nov-08	C	Change logo and fine print to ON Semiconductor

PUBLICATION ORDERING INFORMATION
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