

# TOSHIBA MOS MEMORY PRODUCTS

TC5565APL-10, TC5565APL-12, TC5565APL-15  
 TC5565AFL-10, TC5565AFL-12, TC5565AFL-15

## DESCRIPTION

The TC5565APL/AFL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE2 is a logical low or \CE1 is a logical high, the device is placed in low power standby mode in which standby current is 2uA typically. The TC5565APL/AFL has three control inputs. Two chip enable (\CE1, CE2) allow for device selection and data retention control, and an output enable input (\OE) provides fast memory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5565APL also features pin compatibility with the 64K bit EPROM (TMM2764D).

RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems. The TC5565APL is offered in a dual-in-line 28 pin standard plastic package. The TC5565AFL is offered in 28 pin mini Flat Package.

## FEATURES

- Low Power Dissipation  
27.5mW/MHz(Max.) operating
- Standby Current: 100uA(Max.) Ta=70°C
- Access Time  
TC5565APL/AFL-10 : 100ns(Max.)  
TC5565APL/AFL-12 : 120ns(Max.)  
TC5565APL/AFL-15 : 150ns(Max.)
- 5V Single Power Supply
- Power Down Features: CE2, \CE1
- Fully Static Operation

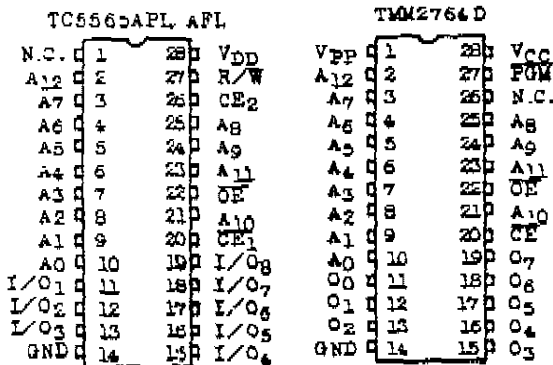
Data Retention Supply Voltage: 2.0-5.5V

- Directly TTL Compatible  
: All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	TC5565APL
300 mil DIP (Slim Package)	*TC5563APL
Flat Package (SOP)	TC5565AFL

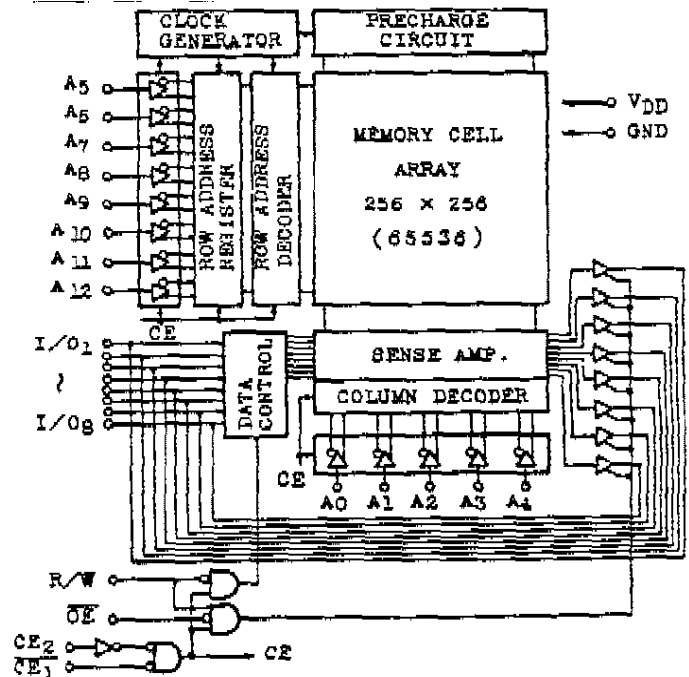
\* See TC5563APL Technical Data.

## PIN CONNECTION (TOP VIEW)



AO-A12	Address Inputs
R/W	Read/Write Control Input
\OE	Output Enable Input
\CE1, CE2	Chip Enable Inputs
I/O1 - I/O8	Data Input/Output
V <sub>DD</sub>	Power (+5V)
GND	Ground
N.C.	No Connection

## BLOCK DIAGRAM



**TC5565APL-10, TC5565APL-12, TC5565APL-15  
TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

OPERATION MODE	\CE1	CE2	\OE	R/W	1/01-T/08	POWER
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	H	*	L	D <sub>IN</sub>	I <sub>DDO</sub>
Output Deselect	L	H	H	H	High-Z	I <sub>DDO</sub>
Standby	H	*	*	*	High-Z	I <sub>DDS</sub>
		L	*	*	High-Z	I <sub>DDS</sub>

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~7.0	v
V <sub>IN</sub>	Input Voltage	*-0.3~7.0	v
V <sub>I/O</sub>	Input and Output Voltage	-0-5-VDD+0.5	v
P <sub>D</sub>	Power Dissipation	1.0/0.6**	W
T <sub>solder</sub>	Soldering Temperature	260-10	°C sec
T <sub>stg</sub>	Storage Temperature	-55~150	°C
T <sub>opr</sub>	Operating Temperature	0-70	°C

\*-3.0V at pulse width 50ns MAX. \*\*Flat package

D.C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	Typ.	MAX.	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	v
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>DD</sub> +0.3	v
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V
V <sub>DH</sub>	Data-Retention Supply Voltage	2.0	-	5.5	V

**TC5565APL-10, TC5565APL-12, TC5565APL-15**  
**TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

D.C and OPERATING CHARACTERISTICS (Ta=0~70°C, V<sub>DD</sub> = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> =0~V <sub>DD</sub>	-	-	±1.0	μA		
I <sub>OH</sub>	Output High Current	VOH-2-4V	-1.0	-		mA		
I <sub>OL</sub>	Output Low Current	VOL-0.4V	4.0	-		mA		
I <sub>LO</sub>	Output Leakage Current	V <sub>IH</sub> or CE2-VOL or \CE1 = V <sub>IH</sub> or CE2=V <sub>OL</sub> Or R/W = V <sub>IL</sub> or \OE=V <sub>IH</sub> V <sub>OUT</sub> =0~V <sub>DD</sub>	-	-	±1.0	μA		
I <sub>DDO1</sub>	Operating Current	V <sub>DD</sub> = 5.5V \CE1=V <sub>IL</sub> CE2=V <sub>IH</sub> Other input= V <sub>IH</sub> /V <sub>IL</sub>	t <sub>cycle</sub> =1.0us			10	mA	
			TC5565APL-10 TC5565AFL-10	t <sub>cycle</sub> =100ns	-	-	45	mA
			TC5565APL-12 TC5565AFL-12	t <sub>cycle</sub> =120ns	-	-	40	mA
			TC5565A?L-15 TC5565AFL-15	t <sub>cycle</sub> =150ns	-	-	35	mA
I <sub>DDO2</sub>	Operating Current	V <sub>DD</sub> =5.5V \CE1=0.2V CE2=V <sub>DD</sub> - 0.2V Other Input= V <sub>DD</sub> - 0.2V/0.2V	t <sub>cycle</sub> =1.0us	-	-	5	mA	
			TC5565APL-10 TC5565AFL-10	t <sub>cycle</sub> =100ns	-	-	40	mA
			TC5565AFL-12 TC5565AFL-12	t <sub>cycle</sub> =120ns	-	-	35	mA
			TC5565APL-15 TC5565AFL-15	t <sub>cycle</sub> =150ns	-	-	30	mA
I <sub>DDS1</sub>	Standby Current	\CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub>			3	mA		
*I <sub>DDS2</sub>		\CE1 = V <sub>DD</sub> - 0.2V or CE2 = 0.2V	V <sub>DD</sub> = 5.5V	-	2	100	μA	
			V <sub>DD</sub> = 3.0V	-	1	50	μA	

Note \* In standby mode with \CE1 >= V<sub>DD</sub> - 0.2V, these specification limits are guaranteed under the condition of CE2 >= V<sub>DD</sub> - 0.2V or CE2 <= 0.2V.

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	-	-	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	-	-	10	pF

\* This parameter periodically sampled is not 100% tested.

**TC5565APL-10, TC5565APL-12, TC5565APL-15  
TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

**A.C. CHARACTERISTICS** (Ta=0~70°C, V<sub>DD</sub> = 5V±10%)

**Read Cycle**

SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
t <sub>RC</sub>	Read Cycle Time	100	-	120	-	150	-
t <sub>ACC</sub>	Address Access Time	-	100	-	120	-	150
t <sub>COL</sub>	\CE1 Access Time	-	100	-	120	-	150
t <sub>CO2</sub>	CE2 Access Time	-	100	-	120	-	150
t <sub>OE</sub>	Output Enable to Output Valid	-	50	-	60	-	70
t <sub>COE</sub>	Chip Enable (\CE1, CE2) to Output in Low-Z	10	-	10	-	15	-
t <sub>OEE</sub>	Output Enable to Output in Low-Z	5	-	5	-	5	-
t <sub>OD</sub>	Chip Enable (CE1, CE2) to Output in High-Z	-	35	-	40	-	50
t <sub>ODO</sub>	Output Enable to Output in High-Z	-	35	-	40	-	50
t <sub>OH</sub>	Output Data Hold Time	20	-	20	-	20	-

**Write Cycle**

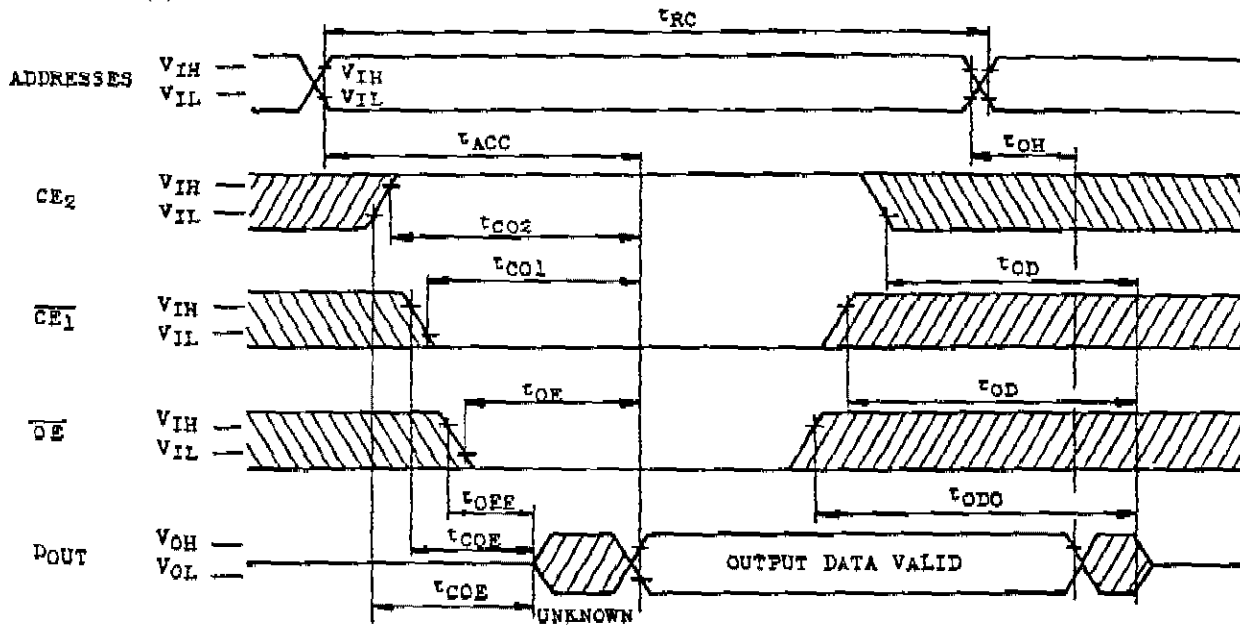
SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL- 5 TC5565AFL- 5	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX..
t <sub>WC</sub>	Write Cycle Time	100	-	120	-	150	-
t <sub>WP</sub>	Write Pulse Width	60	-	70	-	90	-
t <sub>CW</sub>	Chip Selection to End of Write	80	-	85	-	100	-
t <sub>AS</sub>	Address Set up Time	0	-	0	-	0	-
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-
t <sub>ODW</sub>	R/W to Output High-Z	-	35	0	40	-	50
t <sub>OEW</sub>	R/W to Output Low-Z	5	-	5	-	10	-
t <sub>DS</sub>	Data Set up Time	40	-	50	-	60	-
t <sub>DH</sub>	Data Hold Time	0	-	0	-	0	-

**A.C. TEST CONDITION**

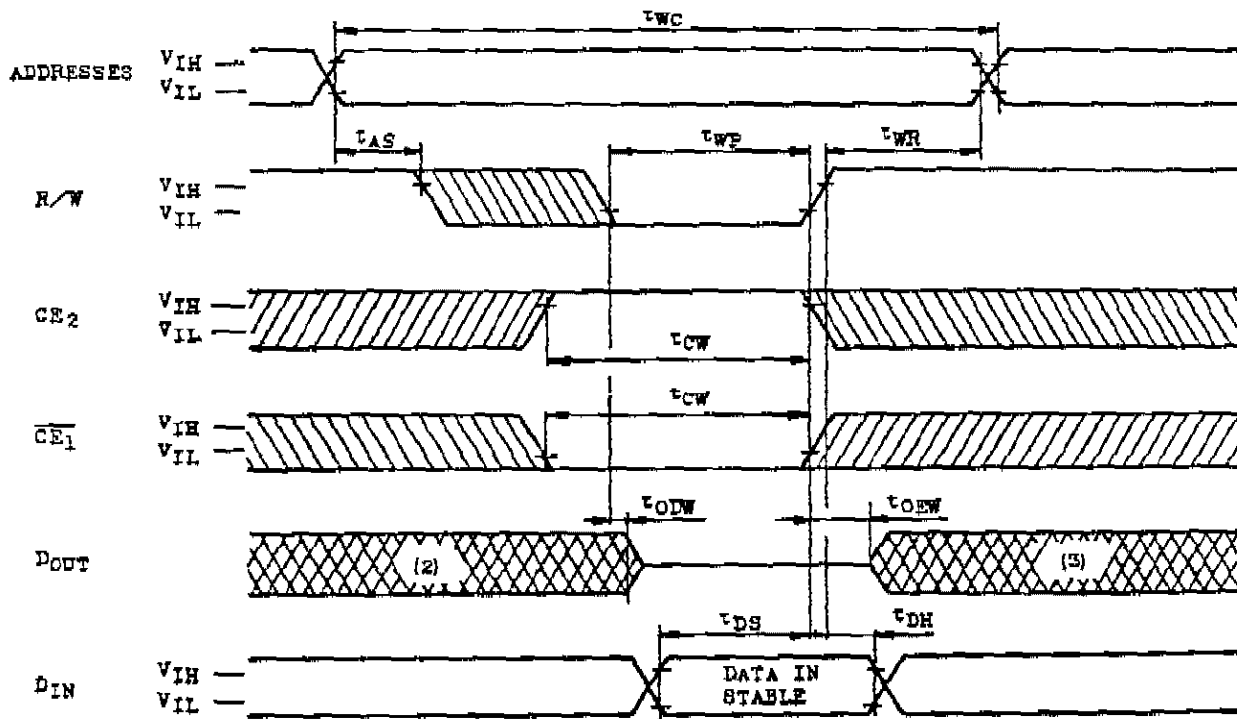
Output Load		: 100pF + 1 TTL Gate
Input Pulse Level		: 0.6V, 2.4V
Timing Measurement	V <sub>IN</sub>	: 0.8V, 2.2V
Reference Level	V <sub>OUT</sub>	: 0.8V, 2.2V
t <sub>r</sub> , t <sub>f</sub>		: 5ns

TC5565APL-10, TC5565APL-12, TC5565APL-15  
 TC5565AFL-10, TC5565AFL-12, TC5565AFL-15

TIMING WAVEFORMS  
 READ CYCLE (1)

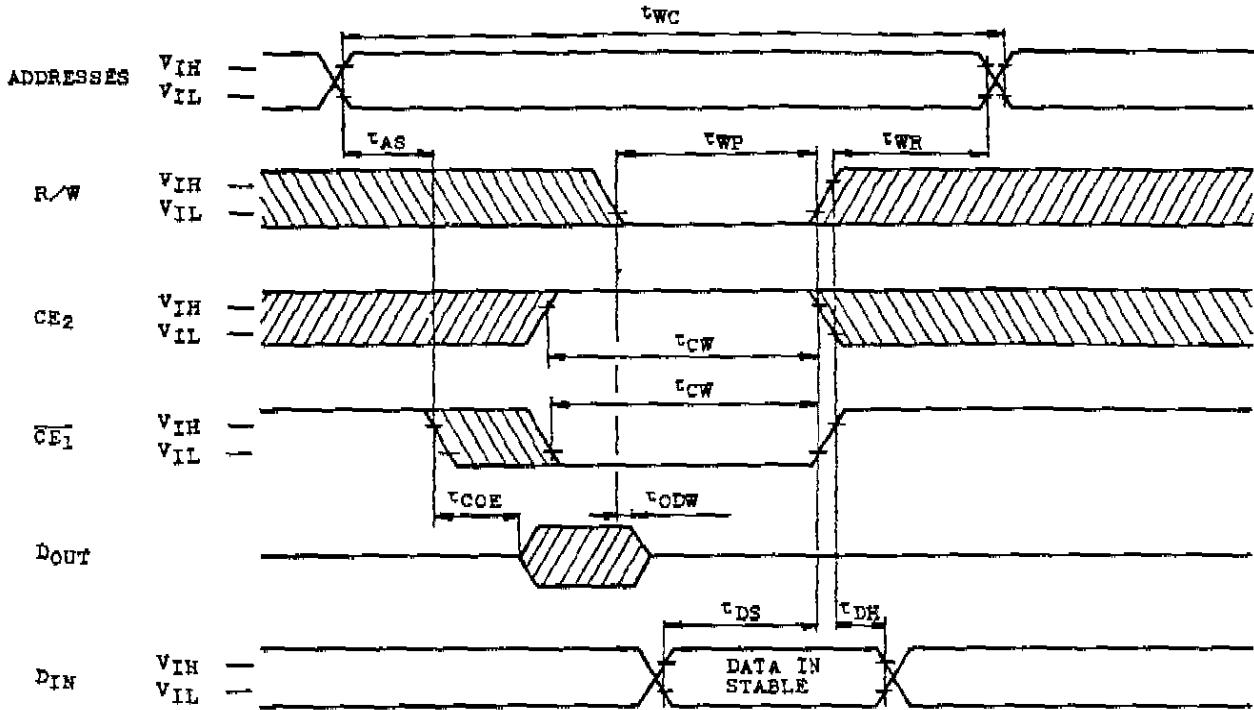


WRITE CYCLE 1 (4) (R/W Controlled Write)

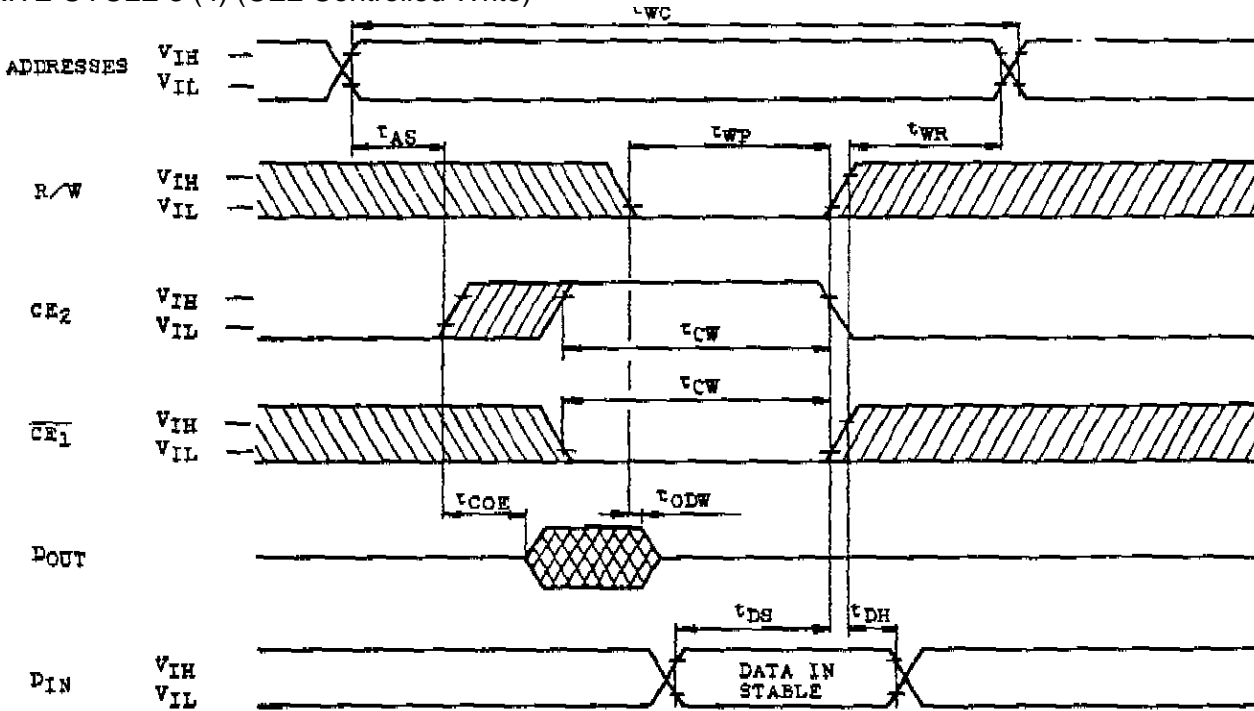


TC5565APL-10, TC5565APL-12, TC5565APL-15  
 TC5565AFL-10, TC5565AFL-12, TC5565AFL-15

WRITE CYCLE 2 (4) (\overline{CE1} Controlled Write)



WRITE CYCLE 3 (4) ( $\overline{CE2}$  Controlled Write)



**TC5565APL-10, TC5565APL-12, TC5565APL-15**  
**TC5565AFL-10, TC5565AFL-12, TC5565AFL-15**

Note 1. R/W is High for Read Cycle.

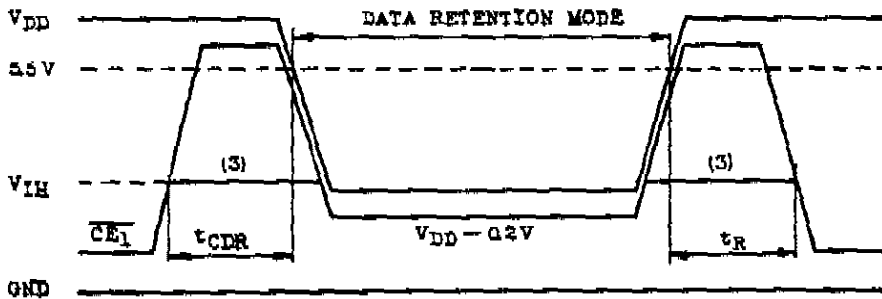
2. Assuming that \CE1 Low transition of CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that \CE1 High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that \OE is High for Write Cycle, Outputs are in high impedance state during this period.

**DATA RETENTION CHARACTERISTICS (Ta=0~70°C)**

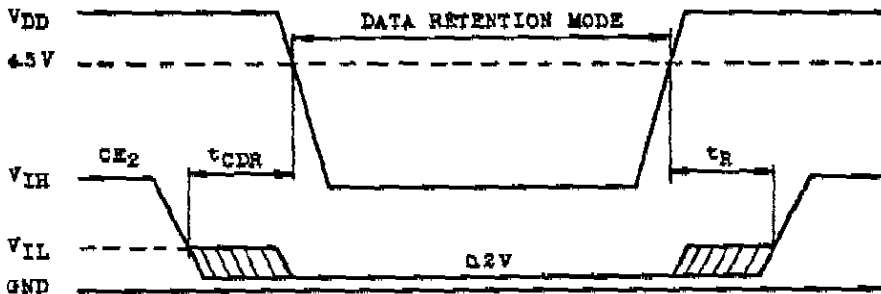
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	V
I <sub>DDs2</sub>	Stand by Supply Current	VDD=3.0V	-	50	uA
		VDD=5.5V	-	100	
t <sub>CDR</sub>	Chip Deselection to Data Retention Mode	0	-	-	us
t <sub>R</sub>	Recovery Mode	t <sub>RC</sub> (1)	-	-	us

Note (1) : Read cycle Time.

**\CE1 Controlled Data Retention Mode (2)**



**CE2 Controlled Data Retention Mode (4)**



## TC5565APL-10, TC5565APL-12, TC5565APL-15 TC5565AFL-10, TC5565AFL-12, TC5565AFL-15

- Note 2 : In  $\overline{\text{CE1}}$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $\text{CE2} \leq 0.2\text{V}$  Or  $\text{CE2} \geq V_{\text{DD}} - 0.2\text{V}$ .
- 3 : If the  $V_{\text{IH}}$  of  $\overline{\text{CE1}}$  is 2.2V in operation,  $I_{\text{DDSI}}$  current flows during the period that the  $V_{\text{DD}}$  voltage is going down from 4.5V to 2.4V,
- 4 ; In  $\text{CE2}$  controlled data retention mode, minimum standby current mode is achieved under the condition of  $\text{CE2} \leq 0.2\text{V}$ .

### DEVICE INFORMATION

The TC5565APL/AFL is an synchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on  $V_{\text{DD}}$  /GND lines. Thus the use of about 0.1 $\mu\text{F}$  decoupling capacitor for every device is recommended to eliminate such noise.

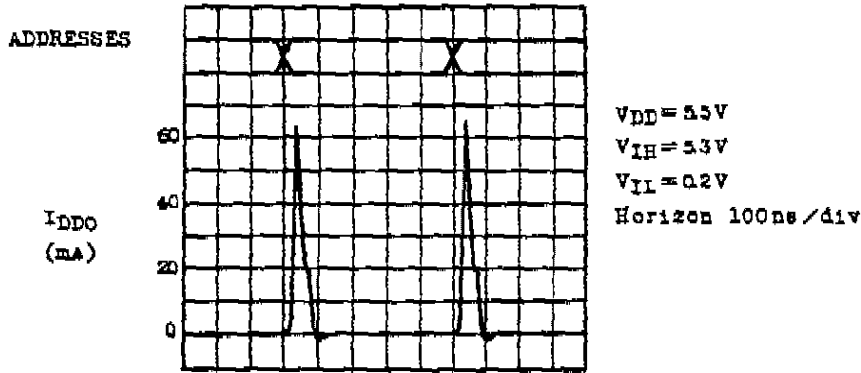


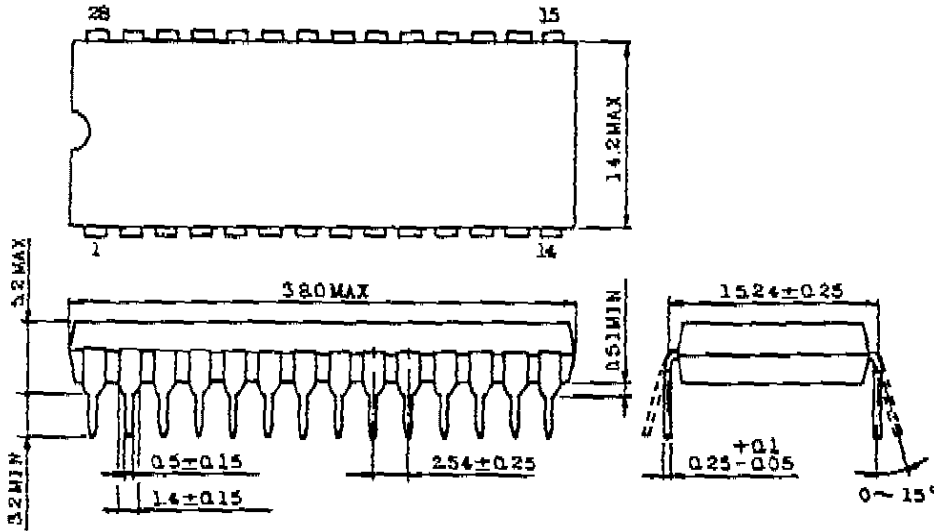
Fig. TYPICAL CURRENT WAVEFORMS



TC5565APL-10, TC5565APL-12, TC5565APL-15  
 TC5565AFL-10, TC5565AFL-12, TC5565AFL-15

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

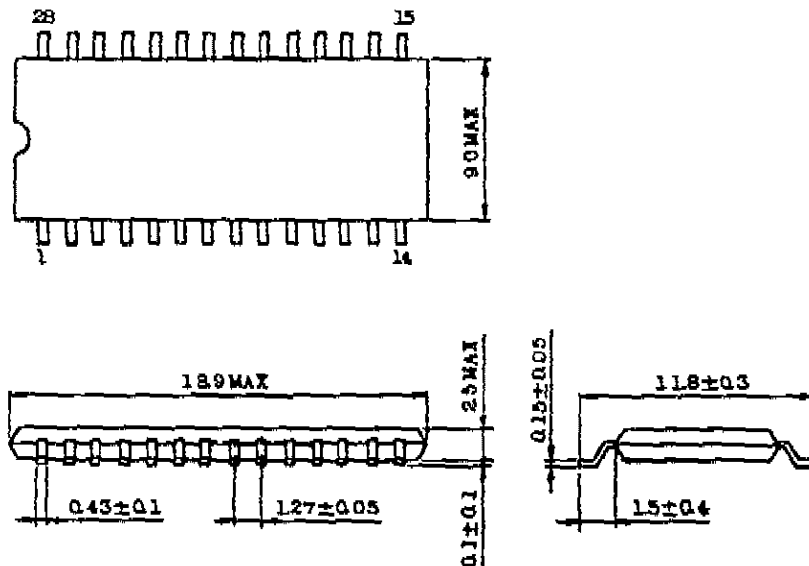
Unit in mm



Note) Lead pitch is 2.54 and tolerance is  $\pm 0.25$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

MFP 28 PIN OUTLINE DRAWING (F28GC-P)

Unit in mm



Note) Lead pitch is 1.27 and tolerance is  $\pm 0.12$  against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.