

LH28F128BFHTPBTL75A Flash Memory 16Mbit (8Mbitx16)

(Model Number: LHF12F17)

Spec. Issue Date: June 7, 2004



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PRELIMINARY SPECIFICATIONS Product Type 128 M b i t Flash Memory L H 2 8 F 1 2 8 B F H T — P B T L 7 5 A Model No. (LHF12F17) This device specification is subject to change without notice. * This specifications contains 32 pages including the cover and appendix. **CUSTOMERS ACCEPTANCE** DATE: BY: **PRESENTED** Dept. General Manager **REVIEWED BY:** PREPARED BY:

Product Development Dept. II System-Flash Division Integrated Circuits Group **SHARP CORPORATION**



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- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.
 - (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
 - Office electronics
 - Instrumentation and measuring equipment
 - Machine tools
 - Audiovisual equipment
 - Home appliance
 - Communication equipment other than for trunk lines
 - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
 - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
 - Mainframe computers
 - Traffic control systems
 - Gas leak detectors and automatic cutoff devices
 - Rescue and security equipment
 - Other safety devices and safety equipment, etc.
- (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
 - Aerospace equipment
 - Communications equipment for trunk lines
 - Control equipment for the nuclear power industry
 - Medical equipment related to life support, etc.
- (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.
- Please direct all queries regarding the products covered herein to a sales representative of the company.



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LH28F128BFHT-PBTL75A 128Mbit (8Mbit×16) Page Mode Dual Work Flash MEMORY

- 128-M density with 16-bit I/O Interface
- High Performance Reads

HARP

- 75/25ns 8-Word Page Mode
- 6-Plane Dual Work Operation
 - Read operations are available during Block Erase or (Page Buffer) Program between two different Planes
 - Plane Architecture: 16M, 24M, 24M, 24M, 24M, 16M
- Low Power Operation
 - 2.7V Read and Write Operations
 - V_{CCO} for Input/Output Power Supply Isolation
 - Automatic Power Savings Mode reduces I_{CCR} in Static Mode
- Enhanced Code + Data Storage
 - 5µs Typical Erase/Program Suspends
- OTP (One Time Program) Block
 - 4-Word Factory-Programmed Area
 - 4-Word User-Programmable Area
- High Performance Program with Page Buffer
 - 16-Word Page Buffer
 - 5µs/Word (Typ.) at WP#/ACC=9.5V
- Operating Temperature -40°C to +85°C
- CMOS Process (P-type silicon substrate)

- Flexible Blocking Architecture
 - Eight 4-Kword Parameter Blocks
 - Two-hundred and fifty-five 32-Kword Main Blocks
 - Bottom Parameter Location
- Enhanced Data Protection Features
 - Individual Block Lock and Block Lock-Down with Zero-Latency
 - All blocks are locked at power-up or device reset.
 - Block Erase, Full Chip Erase, (Page Buffer) Word Program Lockout during Power Transitions
- Automated Erase/Program Algorithms
 - 3.0V Low-Power 11µs/Word (Typ.) Programming
 - 9.5V No Glue Logic 9µs/Word (Typ.) Production Programming and 0.8s Erase (Typ.)
- Cross-Compatible Command Support
 - Basic Command Set
 - Common Flash Interface (CFI)
- Extended Cycling Capability
 - Minimum 100,000 Block Erase Cycles
- 56-Lead TSOP (Normal Bend)
- ETOX^{TM*} Flash Technology
- Not designed or rated as radiation hardened

The product, which is 6-Plane Page Mode Dual Work (Simultaneous Read while Erase/Program) Flash memory, is a low power, high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at V_{CC}=2.7V-3.3V. Its low voltage operation capability greatly extends battery life for portable applications.

The product provides high performance asynchronous page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states.

The memory array block architecture utilizes Enhanced Data Protection features, and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program.

Special OTP (One Time Program) block provides an area to store permanent code such as an unique number.

* ETOX is a trademark of Intel Corporation.

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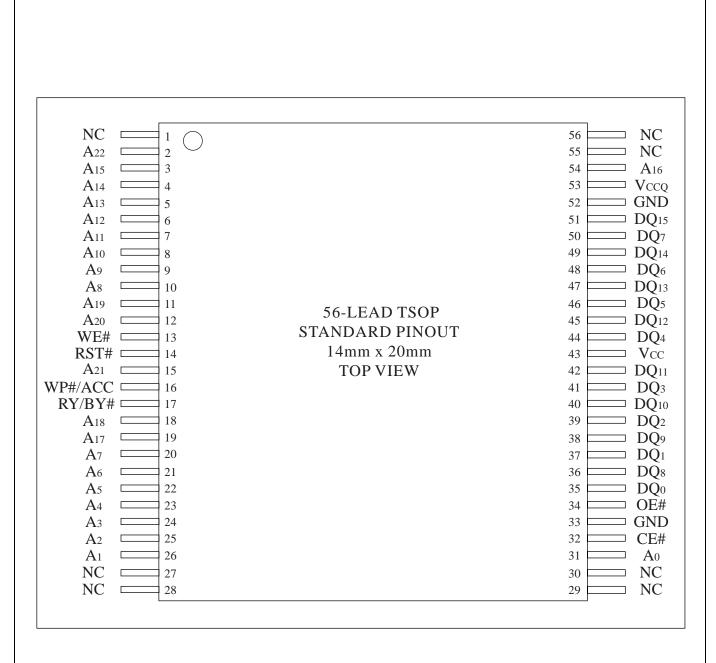


Figure 1. 56-Lead TSOP (Normal Bend) Pinout





Symbol	Type	Name and Function
A ₂₂ -A ₀	INPUT	ADDRESS INPUTS: Inputs for addresses.
DQ ₁₅ -DQ ₀	INPUT/ OUTPUT	DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code and identifier code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high (V_{IH}) deselects the device and reduces power consumption to standby levels.
RST#	INPUT	RESET: When low (V_{IL}) , RST# resets internal automation and inhibits write operations which provides data protection. RST#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RST# must be low during power-up/down.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of CE# or WE# (whichever goes high first).
WP#/ACC	INPUT/ SUPPLY	WRITE PROTECT: When WP#/ACC is V_{IL} , locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and not locked-down. When WP#/ACC is V_{IH} , lock-down is disabled. Applying 9.5V±0.5V to WP#/ACC provides fast erasing or fast programming mode. In this mode, WP#/ACC is power supply pin. Applying 9.5V±0.5V to WP#/ACC during erase/program can only be done for a maximum of 1,000 cycles on each block. WP#/ACC may be connected to 9.5V±0.5V for a total of 80 hours maximum. Use of this pin at 9.5V+0.5V beyond these limits may reduce block cycling capability or cause permanent damage.
RY/BY#	OPEN DRAIN OUTPUT	READY/BUSY#: Indicates the status of the internal WSM (Write State Machine). When low, WSM is performing an internal operation (block erase, full chip erase, (page buffer) program or OTP program). RY/BY#-High Z indicates that the WSM is ready for new commands, block erase is suspended and (page buffer) program is inactive, (page buffer) program is suspended, or the device is in reset mode.
V _{CC}	SUPPLY	DEVICE POWER SUPPLY (2.7V-3.3V): With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
V _{CCQ}	SUPPLY	INPUT/OUTPUT POWER SUPPLY (2.7V-3.3V): Power supply for all input/output pins.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internally connected; it may be driven or floated.

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Table 2. Simultaneous Operation Modes Allowed with 6 Planes $^{(1,\,2)}$

	THEN THE MODES ALLOWED IN THE OTHER PLANE IS:										
IF ONE PLANE IS:	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X		X		X	X
Read ID/OTP	X	X	X	X	X	X		X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X		X		X	X
Word Program	X	X	X	X							X
Page Buffer Program	X	X	X	X							X
OTP Program			X								
Block Erase	X	X	X	X							
Full Chip Erase			X								
Program Suspend	X	X	X	X							X
Block Erase Suspend	X	X	X	X	X	X				X	

NOTES:

- 1. "X" denotes the operation available.
- 2. Dual Work Restrictions:

Status register reflects WSM (Write State Machine) state.
Only one plane can be erased or programmed at a time - no command queuing.

Commands must be written to an address within the block targeted by that command.

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		$[A_{22}-A_0]$			
		_			
ŀ	32-Kword Block 86 32-Kword Block 85	278000H - 27FFFFH 270000H - 277FFFH			
H	32-Kword Block 84	268000H - 26FFFFH			
Ī	32-Kword Block 83	260000H - 267FFFH			
	32-Kword Block 82	258000H - 25FFFFH			
ŀ	32-Kword Block 81	250000H - 257FFFH 248000H - 24FFFFH			
H	32-Kword Block 80 32-Kword Block 79	240000H - 247FFFH			$[A_{22}-A_0]$
t	32-Kword Block 78	238000H - 23FFFFH			$[A22^{-}A0]$
I	32-Kword Block 77	230000H - 237FFFH		32-Kword Block 38	0F8000H - 0FFFFFH
ļ	32-Kword Block 76	228000H - 22FFFFH		32-Kword Block 37	0F0000H - 0F7FFFH
+	32-Kword Block 75 32-Kword Block 74	220000H - 227FFFH 218000H - 21FFFFH		32-Kword Block 36	0E8000H - 0EFFFFH 0E0000H - 0E7FFFH
İ	32-Kword Block 73	210000H - 217FFFH		32-Kword Block 35 32-Kword Block 34	0D8000H - 0DFFFFH
Į	32-Kword Block 72	208000H - 20FFFFH		32-Kword Block 33	0D0000H - 0D7FFFH
-	32-Kword Block 71	200000H - 207FFFH		32-Kword Block 32	0C8000H - 0CFFFFH
-	32-Kword Block 70 32-Kword Block 69	1F8000H - 1FFFFFH 1F0000H - 1F7FFFH		32-Kword Block 31	OC0000H - 0C7FFFH
-	32-Kword Block 68	1E8000H - 1EFFFFH		32-Kword Block 30 32-Kword Block 29	0B8000H - 0BFFFFH 0B0000H - 0B7FFFH
Ī	32-Kword Block 67	1E0000H - 1E7FFFH		32-Kword Block 29	0A8000H - 0AFFFFH
	32-Kword Block 66	1D8000H - 1DFFFFH		32-Kword Block 27	0A0000H - 0A7FFFH
-	32-Kword Block 65	1D0000H - 1D7FFFH		32-Kword Block 26	098000H - 09FFFFH
ŀ	32-Kword Block 64 32-Kword Block 63	1C8000H - 1CFFFFH 1C0000H - 1C7FFFH		32-Kword Block 25	090000H - 097FFFH 088000H - 08FFFFH
t	32-Kword Block 62	1B8000H - 1BFFFFH		32-Kword Block 24 32-Kword Block 23	080000H - 087FFFH
	32-Kword Block 61	1B0000H - 1B7FFFH		32-Kword Block 22	078000H - 07FFFFH
<u>.</u>	32-Kword Block 60	1A8000H - 1AFFFFH	[유	32-Kword Block 21	070000H - 077FFFH
3 -	32-Kword Block 59 32-Kword Block 58	1A0000H - 1A7FFFH 198000H - 19FFFFH	PLANEO	32-Kword Block 20	068000H - 06FFFFH
FLAINE	32-Kword Block 57	190000H - 197FFFH	IΞ	32-Kword Block 19 32-Kword Block 18	060000H - 067FFFH 058000H - 05FFFFH
7	32-Kword Block 56	188000H - 18FFFFH	🗖	32-Kword Block 17	050000H - 057FFFH
-	32-Kword Block 55	180000H - 187FFFH		32-Kword Block 16	048000H - 04FFFFH
-	32-Kword Block 54	178000H - 17FFFFH		32-Kword Block 15	040000H - 047FFFH
ŀ	32-Kword Block 53 32-Kword Block 52	170000H - 177FFFH 168000H - 16FFFFH		32-Kword Block 14 32-Kword Block 13	038000H - 03FFFFH 030000H - 037FFFH
	32-Kword Block 51	160000H - 167FFFH		32-Kword Block 12	028000H - 02FFFFH
-	32-Kword Block 50	158000H - 15FFFFH		32-Kword Block 11	020000H - 027FFFH
-	32-Kword Block 49	150000H - 157FFFH		32-Kword Block 10	018000H - 01FFFFH
ŀ	32-Kword Block 48 32-Kword Block 47	148000H - 14FFFFH 140000H - 147FFFH		32-Kword Block 9 32-Kword Block 8	010000H - 017FFFH 008000H - 00FFFFH
	32-Kword Block 46	138000H - 13FFFFH		4-Kword Block 7	007000H - 007FFFH
	32-Kword Block 45	130000H - 137FFFH		4-Kword Block 6	006000H - 006FFFH
+	32-Kword Block 44	128000H - 12FFFFH		4-Kword Block 5	005000H - 005FFFH
ł	32-Kword Block 43 32-Kword Block 42	120000H - 127FFFH 118000H - 11FFFFH		4-Kword Block 4 4-Kword Block 3	004000H - 004FFFH 003000H - 003FFFH
į	32-Kword Block 41	110000H - 117FFFH		4-Kword Block 3	002000H - 002FFFH
	32-Kword Block 40	108000H - 10FFFFH		4-Kword Block 1	001000H - 001FFFH
	32-Kword Block 39	100000H - 107FFFH		4-Kword Block 0	000000H - 000FFFH
		[bit		PLANE0: 16 M	

Figure 2.1. Memory Map (Bottom Parameter, Plane 0 and Plane 1)



32-Kword Block 181 5700000H - 577FFFH 32-Kword Block 179 550000H - 567FFFH 32-Kword Block 179 550000H - 567FFFH 32-Kword Block 178 550000H - 557FFFH 32-Kword Block 178 55000H - 557FFFH 32-Kword Block 175 540000H - 547FFFH 32-Kword Block 175 32-Kword Block 175 540000H - 547FFFH 32-Kword Block 176 32-Kword Block 173 530000H - 537FFFH 32-Kword Block 171 520000H - 527FFFH 32-Kword Block 171 520000H - 527FFFH 32-Kword Block 171 520000H - 527FFFH 32-Kword Block 170 518000H - 517FFFH 32-Kword Block 165 50000H - 517FFFH 32-Kword Block 166 478000H - 477FFFH 32-Kword Block 166 478000H - 477FFFH 32-Kword Block 167 480000H - 477FFFH 32-Kword Block 167 480000H - 477FFFH 32-Kword Block 168 480000H - 477FFFH 32-Kword Block 157 480000H - 477FFFH 32-Kword Block 158 480000H - 477FFFH 32-Kword Block 159 420000H - 477FFFH 32-Kword Block 159 420000H - 477FFFH 32-Kword Block 151 480000H - 477FFFH 32-Kword Block 157 480000H - 477FFFH 32-Kword Block 157 480000H - 477FFFH 32-Kword Block 157 48000H - 477FFFH 32-Kword Block 151 49000H - 477FFFH 32-Kword Block 157 49000H - 477FFFH 32-Kword Block 157 49000H - 477FFFH 32-Kword Block 157 49000H - 477FFFH 32-Kword Block 158 49000H - 477FFFH 32-Kword Block 157 49000H - 477FFFH 32-Kword Block						
32-Kword Block 182						
32-Kword Block 180 32-Kword Block 180 32-Kword Block 180 32-Kword Block 195 32-Kword Block 195 32-Kword Block 175 32-Kword Block 177 32-Kword Block 177 32-Kword Block 175 32-Kword Block 176 32-Kword Block 176 32-Kword Block 177 32-Kword Block 177 32-Kword Block 177 32-Kword Block 178 32-Kword Block 188 32-Kword Block 189 32-Kword Bloc						
32-Kword Block 180 32-Kword Block 180 32-Kword Block 180 32-Kword Block 195 32-Kword Block 195 32-Kword Block 175 32-Kword Block 177 32-Kword Block 177 32-Kword Block 175 32-Kword Block 176 32-Kword Block 176 32-Kword Block 177 32-Kword Block 177 32-Kword Block 177 32-Kword Block 178 32-Kword Block 188 32-Kword Block 189 32-Kword Bloc			[[]]			[0.4.4.4]
32-Kword Block 180			[A22-A0]			[A22-A0]
32-Kword Block 179 32-Kword Block 179 558000H - 567FFFH 32-Kword Block 177 558000H - 567FFFH 32-Kword Block 177 52-Kword Block 176 548000H - 547FFFH 32-Kword Block 175 54000H - 547FFFH 32-Kword Block 175 53800H - 53FFFFH 32-Kword Block 174 53800H - 53FFFFH 32-Kword Block 175 32-Kword Block 175 32-Kword Block 174 53800H - 53FFFFH 32-Kword Block 175 32-Kword Block 175 32-Kword Block 175 32-Kword Block 175 32-Kword Block 176 32-Kword Block 177 32-Kword Block 176 32-Kword Block 177 32-Kword Block 176 32-Kword Block 169 510000H - 527FFFH 32-Kword Block 169 510000H - 527FFFH 32-Kword Block 169 32-Kword Block 164 48000H - 447FFFH 32-Kword Block 155 32-Kword Block 156 32-Kword Block 157 32-Kword Block 169 32-Kword Block 160 32-Kword Block 160 32-Kword Block 160 32-Kword Block 160 32-Kword Block 173 32-Kword Block 160 32-Kword Block 180 32-Kword Block 180 32-Kword Block 180 32-Kword Block 180 32-Kword Block 181 32-Kword Block 184 48000H - 47FFFH 32-Kword Block 181 32-Kword Block 184 48000H - 47FFFH 32-Kword Block 181 32-Kword Block 184 48000H - 47FFFH 32-Kword Block 181 32-Kword Block 184 48000H - 47FFFH 32-Kword Block 181 32-Kword Block 183 32-Kword Block 183 40000H - 47FFFH 32-Kword Block 184 48000H - 47FFFH 32-Kword Block 184 48000H - 47FFFH 32-Kword Block 185 32-Kword Block 185 32-Kword Block 184 48000H - 47FFFH 32-Kword Block 180 32-Kword Block 181 32-Kword Block 181 32-Kword Block 181 32-Kword Block 181 32-Kword Block 183 32-Kword Block 183 32-Kword Block 183 32-Kword Block		32-Kword Block 182			32-Kword Block 134	3F8000H - 3FFFFFH
32-Kword Block 179 550000H - 567FFFH 32-Kword Block 131 32-Kword Block 131 32-Kword Block 137 32-Kword Block 177 32-Kword Block 177 32-Kword Block 175 340000H - 547FFFH 32-Kword Block 175 32-Kword Block 171 32-Kword Block 175 32-Kword Block 175 32-Kword Block 167 32-Kword Block 169 310000H - 517FFFH 32-Kword Block 169 310000H - 517FFFH 32-Kword Block 169 32-Kword Block 169 32-Kword Block 167 32-Kword Block 168 4F8000H - 4FFFFFH 32-Kword Block 169 4F8000H - 4FFFFFH 32-Kword Block 160 4F8000H - 4FFFFFH 32-Kword Block 161 4F8000H - 4FFFFH 32-Kword Block 161 4F800						3F0000H - 3F7FFFH
32-Kword Block 178 32-Kword Block 177 32-Kword Block 177 32-Kword Block 177 32-Kword Block 174 32-Kword Block 174 32-Kword Block 173 32-Kword Block 174 32-Kword Block 173 32-Kword Block 174 32-Kword Block 175 32-Kword Block 175 32-Kword Block 175 32-Kword Block 170 32-Kword Block 180 32-Kword Block 181 32-Kword Block 180 32-Kword Block 181 32-Kword Block 180 32-Kword Block 181 32-Kword Block 183 32-Kword Block 183 32-Kword Block 183 32-Kword Block 184 480000+ 487FFFH 32-Kword Block 183 32-Kword Block 183 32-Kword Block 183 32-Kword Block 184 480000+ 487FFFH 32-Kword Block 183						
32-Kword Block 177						
32-Kword Block 176 32-Kword Block 175 32-Kword Block 174 33-Kword Block 174 33-Kword Block 174 33-Kword Block 175 33-Kword Block 172 33-Kword Block 171 33-Kword Block 170 33-Kword Block 160 33-Kword Block 160 33-Kword Block 167 33-Kword Block 168 33-Kword Block 167 33-Kword Block 167 33-Kword Block 167 33-Kword Block 167 33-Kword Block 168 33-Kword Block 161 33-Kword Block 164 33-Kword Block 165 33-Kword Block 164 33-Kword Block 165 33-Kword Block 164 33-Kword Block 164 33-Kword Block 165 33-Kword Block 164 33-Kword Block 165 33-Kword Block 164 33-Kword Block 165 33-Kword Block 164 33-Kword Block 164 33-Kword Block 165 33-Kword Block 164 33-Kword Block 164 33-Kword Block 165 33-Kword Block 165 33-Kword Block 164 33-Kword Block 165 33-Kword Block 164 33-Kword Block 165 33-Kword Block 165 33-Kword Block 165 33-Kword Block 164 33-Kword Block 165 33-Kword Block 165 33-Kword Block 166 33-Kword Block 167 33-Kword Block 167 33-Kword Block 168 33-Kword Block 168 33-Kword Block 169 33-Kword Block 169 33-Kword Block 169 33-Kword Block 170 33-Kword Bloc						
32-Kword Block 175 540000H - 547FFFH 32-Kword Block 173 53000H - 537FFFH 32-Kword Block 173 53000H - 537FFFH 32-Kword Block 173 53000H - 537FFFH 32-Kword Block 121 38000H - 347FFF 32-Kword Block 171 52000H - 527FFFH 32-Kword Block 169 510000H - 517FFFH 32-Kword Block 169 510000H - 517FFFH 32-Kword Block 168 50800H - 507FFFH 32-Kword Block 168 50800H - 507FFFH 32-Kword Block 166 47800H - 47FFFFH 32-Kword Block 165 47800H - 47FFFFH 32-Kword Block 166 47800H - 47FFFFH 32-Kword Block 161 47800H - 47FFFH 32-Kword Block 163 48000H - 47FFFH 32-Kword Block 159 40000H - 47FFFH 32-Kword Block 159 40000H - 47FFFH 32-Kword Block 151 48000H - 47FFFH 32-Kword Block 152 48000H - 47FFFH 32-Kword Block 154 48000H - 47FFFH 32-Kword Block 155 48000H - 47FFFH 32-Kword Block 151 48000H - 47FFFH 32-Kword Block 151 48000H - 47FFFH 32-Kword Block 152 48000H - 47FFFH 32-Kword Block 154 48000H - 47FFFH 32-Kword Block 164 48000H - 47FFFH 32-Kword Block 164 48000H - 47FFFH 32-Kword Block 140 43000H - 47FFFH 32-Kword Block 141 43000H - 47FFFH 32-Kword Block 141 43000H - 47FFFH 32-Kword Block 141 43000H - 47FFFH 32-Kword Block 142 43000H - 47FFFH 32-Kword Block 142 43000H - 47FFFH 32-Kword Block 143 40000H - 47FFFH 32-Kword Block 140 42800H - 47FFFH 32-Kword Block 140 42800H - 47FFFH 32-Kword Block 141 43000H - 47FFFH 32-Kword Block 141 43000H - 47FFFH 32-Kword Block 140 42800H - 47FFFH 32-Kword Block 140 42800H - 47FFFH 32-Kword Block 140 42800H - 47FFFH 3						3C8000H - 3CFFFFH
32-Kword Block 174 32-Kword Block 173 32-Kword Block 171 32-Kword Block 171 32-Kword Block 171 32-Kword Block 171 32-Kword Block 170 32-Kword Block 170 32-Kword Block 170 32-Kword Block 167 32-Kword Block 168 32-Kword Block 168 32-Kword Block 168 32-Kword Block 167 32-Kword Block 164 488000H - 4FFFFH 32-Kword Block 163 32-Kword Block 164 488000H - 4FFFFH 32-Kword Block 163 32-Kword Block 164 32-Kword Block 163 32-Kword Block 164 32-Kword Block 165 32-Kword Block 164 32-Kword Block 165 32-Kword Block 164 32-Kword Block 165 32-Kword Block 167 32-Kword Block 167 32-Kword Block 168 32-Kword Block 169 32-Kword Block 169 32-Kword Block 160 32-Kword Block 170 32-Kword Block 17						3C0000H - 3C7FFFH
32-Kword Block 172 32-Kword Block 175 32-Kword Block 177 32-Kword Block 177 32-Kword Block 169 32-Kword Block 165 33-Kword Block 168 33-Kword Block 167 32-Kword Block 165 32-Kword Block 165 32-Kword Block 164 488000H - 4FFFFH 32-Kword Block 163 488000H - 4FFFFH 32-Kword Block 164 428000H - 4FFFFH 32-Kword Block 165 32-Kword Block 164 428000H - 4FFFFH 32-Kword Block 159 32-Kword Block 151 32-Kword Block 152 32-Kword Block 153 32-Kword Block 144 48000H - 47FFFH 32-Kword Block 101 32-Kword Block 102 32-Kword Block 104 32-Kword Block 103 32-Kword Block 144 48000H - 47FFFH 32-Kword Block 92 22-Kword Block 92 22-Kword Block 92 22-Kword Block 92 22-Kword Block 93 22-Kword Block		32-Kword Block 174	538000H - 53FFFFH		32-Kword Block 126	3B8000H - 3BFFFFH
32-Kword Block 170 32-Kword Block 169 32-Kword Block 169 32-Kword Block 169 32-Kword Block 166 32-Kword Block 161 32-Kword Block 164 32-Kword Block 165 32-Kword Block 164 32-Kword Block 164 32-Kword Block 165 32-Kword Block 164 32-Kword Block 165 32-Kword Block 164 32-Kword Block 165 32-Kword Block 161 32-Kword Block 150 32-Kword Block 159 32-Kword Block 159 32-Kword Block 157 32-Kword Block 157 32-Kword Block 157 32-Kword Block 157 32-Kword Block 151 32-Kword Block 154 32-Kword Block 155 32-Kword Block 154 32-Kword Block 154 32-Kword Block 155 32-Kword Block 155 32-Kword Block 154 32-Kword Block 155 32-Kword Block 155 32-Kword Block 154 32-Kword Block 155 32-Kword Block 144 348000H - 447FFFH 32-Kword Block 100 32-Kword Block 145 32-Kword Block 146 32-Kword Block 147 32-Kword Block 147 32-Kword Block 148 32-Kword Block 149 32-Kword Block 149 32-Kword Block 149 32-Kword Block 140 32-Kword Block		32-Kword Block 173			32-Kword Block 125	3B0000H - 3B7FFFH
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32-Kword Block 147 460000H - 467FFFH 32-Kword Block 99 2E0000H - 2E7FFF 32-Kword Block 145 450000H - 457FFFH 32-Kword Block 97 2D0000H - 2D7FF 32-Kword Block 143 440000H - 447FFFH 32-Kword Block 95 2C8000H - 2C7FFI 32-Kword Block 142 438000H - 437FFFH 32-Kword Block 94 2B8000H - 2C7FFI 32-Kword Block 141 43000H - 437FFFH 32-Kword Block 94 2B8000H - 2B7FFI 32-Kword Block 140 428000H - 427FFFH 32-Kword Block 95 2B0000H - 2B7FFI 32-Kword Block 140 428000H - 427FFFH 32-Kword Block 92 2A8000H - 2B7FFI 32-Kword Block 139 420000H - 427FFFH 32-Kword Block 92 2A8000H - 2A7FF 32-Kword Block 138 418000H - 417FFFH 32-Kword Block 90 298000H - 297FFFI 32-Kword Block 136 408000H - 407FFFH 32-Kword Block 89 290000H - 297FFF 32-Kword Block 136 408000H - 407FFFH 32-Kword Block 89 288000H - 287FFF 32-Kword Block 136 408000H - 407FFFH 32-Kword Block 87 280000H - 287FFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFF 32-Kword Block 87 280000H -						2F0000H - 2F7FFFH
32-Kword Block 146 458000H - 45FFFFH 32-Kword Block 98 2D8000H - 2DFFF 32-Kword Block 145 48000H - 44FFFFH 32-Kword Block 96 2C8000H - 2CFFF 32-Kword Block 142 438000H - 44FFFFH 32-Kword Block 95 2C0000H - 2CFFF 32-Kword Block 142 438000H - 43FFFFH 32-Kword Block 95 2E8000H - 2FFFF 32-Kword Block 141 430000H - 43FFFFH 32-Kword Block 93 2B0000H - 2BFFFF 32-Kword Block 140 428000H - 42FFFFH 32-Kword Block 92 2A8000H - 2AFFF 32-Kword Block 139 420000H - 42FFFFH 32-Kword Block 91 2A0000H - 2AFFF 32-Kword Block 137 410000H - 417FFFH 32-Kword Block 89 290000H - 297FFF 32-Kword Block 136 408000H - 40FFFFH 32-Kword Block 89 290000H - 297FFF 32-Kword Block 136 408000H - 40FFFFH 32-Kword Block 89 288000H - 28FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 89 288000H - 28FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 89 288000H - 28FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 89 288000H - 28FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 89 288000H - 28FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 89 280000H - 28FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 89 280000H - 28FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 89 280000H - 28FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 89 280000H - 28FFFF 32-Kword Block 89 280000						2E8000H - 2EFFFFH
32-Kword Block 145 450000H - 457FFFH 32-Kword Block 97 2D0000H - 2D7FFF 32-Kword Block 144 448000H - 447FFFH 32-Kword Block 95 2C0000H - 2C7FFF 32-Kword Block 141 438000H - 437FFFH 32-Kword Block 95 2E8000H - 2EFFFF 32-Kword Block 141 430000H - 437FFFH 32-Kword Block 95 2E8000H - 2EFFFF 32-Kword Block 140 428000H - 427FFFH 32-Kword Block 92 2A8000H - 2EFFFF 32-Kword Block 139 420000H - 427FFFH 32-Kword Block 92 2A8000H - 2EFFFF 32-Kword Block 137 410000H - 417FFFH 32-Kword Block 90 298000H - 297FFFF 32-Kword Block 136 408000H - 407FFFH 32-Kword Block 89 290000H - 297FFFF 32-Kword Block 136 408000H - 407FFFH 32-Kword Block 88 288000H - 287FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFFF 32-Kword Block 87 280000H - 287						
32-Kword Block 144						
32-Kword Block 143						
32-Kword Block 142 438000H - 43FFFFH 32-Kword Block 94 2B8000H - 2BFFFF 32-Kword Block 140 428000H - 42FFFFH 32-Kword Block 139 420000H - 42FFFFH 32-Kword Block 139 420000H - 42FFFFH 32-Kword Block 137 32-Kword Block 137 418000H - 41FFFFH 32-Kword Block 91 240000H - 2AFFFF 32-Kword Block 137 410000H - 41FFFFH 32-Kword Block 90 298000H - 29FFFF 32-Kword Block 136 408000H - 40FFFFH 32-Kword Block 88 288000H - 28FFFFF 32-Kword Block 135 400000H - 40FFFFH 32-Kword Block 87 280000H - 28FFFFF 32-Kword Block 135 400000H - 40FFFFH 32-Kword Block 87 280000H - 28FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF						
32-Kword Block 141 430000H - 437FFFH 32-Kword Block 93 2B0000H - 2B7FFI 32-Kword Block 140 428000H - 42FFFFH 32-Kword Block 92 2A8000H - 2AFFF 32-Kword Block 139 420000H - 427FFFH 32-Kword Block 91 2A0000H - 2A7FF 32-Kword Block 138 418000H - 41FFFFH 32-Kword Block 90 298000H - 29FFFF 32-Kword Block 137 410000H - 417FFFH 32-Kword Block 89 290000H - 297FFF 32-Kword Block 136 408000H - 40FFFFH 32-Kword Block 88 288000H - 28FFFF 32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFF						
32-Kword Block 140 428000H - 42FFFFH 32-Kword Block 92 2A8000H - 2AFFF 32-Kword Block 139 420000H - 42FFFH 32-Kword Block 91 2A0000H - 2AFFF 32-Kword Block 138 418000H - 41FFFFH 32-Kword Block 90 298000H - 29FFFF 32-Kword Block 137 410000H - 41FFFFH 32-Kword Block 89 290000H - 29FFFF 32-Kword Block 136 408000H - 40FFFFH 32-Kword Block 88 288000H - 28FFFF 32-Kword Block 135 400000H - 40FFFFH 32-Kword Block 87 280000H - 287FFF						
32-Kword Block 139						2A8000H - 2AFFFFH
32-Kword Block 138		32-Kword Block 139	420000H - 427FFFH		32-Kword Block 91	2A0000H - 2A7FFFH
32-Kword Block 136						298000H - 29FFFFH
32-Kword Block 135 400000H - 407FFFH 32-Kword Block 87 280000H - 287FFF						290000H - 297FFFH
						288000H - 28FFFFH
		32-Kword Block 135	400000H - 407FFFH		32-Kword Block 87	280000H - 287FFFH
		DI ANICO OZIO	n ·		DI ANIES SAR	m ·
PLANE3: 24 Mbit PLANE2: 24 Mbit		PLANE3: 24 M	DIT		PLANE2 : 24 M	ID1t

Figure 2.2. Memory Map (Bottom Parameter, Plane 2 and Plane 3)

						$[A_{22}-A_0]$
			Ī		32-Kword Block 230	6F8000H - 6FFFFFH
					32-Kword Block 229	6F0000H - 6F7FFFH
					32-Kword Block 228	6E8000H - 6EFFFFH
					32-Kword Block 227	6E0000H - 6E7FFFH
					32-Kword Block 226	6D8000H - 6DFFFFH 6D0000H - 6D7FFFH
					32-Kword Block 225 32-Kword Block 224	6C8000H - 6CFFFFH
					32-Kword Block 223	6C0000H - 6C7FFFH
					32-Kword Block 222	6B8000H - 6BFFFFH
					32-Kword Block 221	6B0000H - 6B7FFFH
					32-Kword Block 220	6A8000H - 6AFFFFH
]	32-Kword Block 219	6A0000H - 6A7FFFH
					32-Kword Block 218	698000H - 69FFFFH
		FA 4 7		-	32-Kword Block 217	690000H - 697FFFH 688000H - 68FFFFH
		$[A_{22}-A_0]$		-	32-Kword Block 216 32-Kword Block 215	680000H - 687FFFH
22.1/	Z 1. D11- 2/2	7F8000H - 7FFFFFH			32-Kword Block 214	678000H - 67FFFFH
	Kword Block 262 Kword Block 261	7F0000H - 7F7FFFH			32-Kword Block 214	670000H - 677FFFH
	Sword Block 260	7E8000H - 7EFFFFH			32-Kword Block 212	668000H - 66FFFFH
	Kword Block 259	7E0000H - 7E7FFFH			32-Kword Block 211	660000H - 667FFFH
32-K	Kword Block 258	7D8000H - 7DFFFFH			32-Kword Block 210	658000H - 65FFFFH
	Kword Block 257	7D0000H - 7D7FFFH			32-Kword Block 209	650000H - 657FFFH
	Kword Block 256	7C8000H - 7CFFFFH			32-Kword Block 208 32-Kword Block 207	648000H - 64FFFFH 640000H - 647FFFH
	Kword Block 255	7C0000H - 7C7FFFH 7B8000H - 7BFFFFH			32-Kword Block 207	638000H - 63FFFFH
	Kword Block 254 Kword Block 253	7B0000H - 7B7FFFH			32-Kword Block 205	630000H - 637FFFH
	Kword Block 252	7A8000H - 7AFFFFH			32-Kword Block 204	628000H - 62FFFFH
	Kword Block 251	7A0000H - 7A7FFFH			32-Kword Block 203	620000H - 627FFFH
	Kword Block 250	798000H - 79FFFFH			32-Kword Block 202	618000H - 61FFFFH
32-K	Kword Block 249	790000H - 797FFFH		4	32-Kword Block 201	610000H - 617FFFH
	Kword Block 248	788000H - 78FFFFH		PLANE4	32-Kword Block 200	608000H - 60FFFFH
$\sqrt{32-K}$	Kword Block 247	780000H - 787FFFH		\overline{A}	32-Kword Block 199 32-Kword Block 198	600000H - 607FFFH 5F8000H - 5FFFFFH
32-K	Kword Block 246 Kword Block 245	778000H - 77FFFFH 770000H - 777FFFH		F	32-Kword Block 197	5F0000H - 5F7FFFH
	Kword Block 244	768000H - 76FFFFH			32-Kword Block 196	5E8000H - 5EFFFFH
	Kword Block 243	760000H - 767FFFH			32-Kword Block 195	5E0000H - 5E7FFFH
	Kword Block 242	758000H - 75FFFFH			32-Kword Block 194	5D8000H - 5DFFFFH
32-K	Kword Block 241	750000H - 757FFFH			32-Kword Block 193	5D0000H - 5D7FFFH
	Kword Block 240	748000H - 74FFFFH			32-Kword Block 192	5C8000H - 5CFFFFH
	Kword Block 239	740000H - 747FFFH			32-Kword Block 191	5C0000H - 5C7FFFH 5B8000H - 5BFFFFH
	Kword Block 238	738000H - 73FFFFH 730000H - 737FFFH			32-Kword Block 190 32-Kword Block 189	5B0000H - 5B7FFFH
	Kword Block 237 Kword Block 236	728000H - 72FFFFH			32-Kword Block 188	5A8000H - 5AFFFFH
	Kword Block 235	720000H - 727FFFH			32-Kword Block 187	5A0000H - 5A7FFFH
	Kword Block 234	718000H - 71FFFFH			32-Kword Block 186	598000H - 59FFFFH
32-K	Kword Block 233	710000H - 717FFFH		ļ	32-Kword Block 185	590000H - 597FFFH
	Kword Block 232	708000H - 70FFFFH			32-Kword Block 184	588000H - 58FFFFH
32-K	Kword Block 231	700000H - 707FFFH	l		32-Kword Block 183	_ 580000H - 587FFFH
DT A	NID5 . 1 C NA	h:4			DI ANIDA . OANA	h.i.t
PLA	NE5 : 16 M	DIL			PLANE4 : 24 M	บน

Figure 2.3. Memory Map (Bottom Parameter, Plane 4 and Plane 5)



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Table 3. Identifier Codes and OTP Address for Read Operation

	Code	Address [A ₁₅ -A ₀]	Data [DQ ₁₅ -DQ ₀]	Notes
Manufacturer Code	Manufacturer Code	0000Н	00B0H	1
Device Code	Device Code	0001H	0011H	1
Block Lock Configuration	Block is Unlocked		$DQ_0 = 0$	2, 3
Code	Block is Locked	Block	$DQ_0 = 1$	2, 3
	Block is not Locked-Down	Address + 2	$DQ_1 = 0$	2, 3
	Block is Locked-Down		$DQ_1 = 1$	2, 3
OTP	OTP Lock	0080H	OTP-LK	1, 4
	OTP	0081-0088H	OTP	1, 5

- $1.\ A_{22}\text{-}A_{16}\ \text{must be the address within the plane to which the Read Identifier Codes/OTP command (90H) has been written.}$
- 2. Block Address = The beginning location of a block address within the plane to which the Read Identifier Codes/OTP command (90H) has been written.
- 3. DQ₁₅-DQ₂ are reserved for future implementation.
- 4. OTP-LK=OTP Block Lock configuration.
- 5. OTP=OTP Block data.

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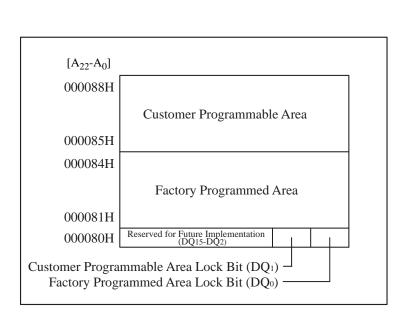


Figure 3. OTP Block Address Map for OTP Program (The area outside 80H~88H cannot be used.)



Table 4. Bus Operation^(1, 2)

Mode	Notes	RST#	CE#	OE#	WE#	Address	DQ ₁₅₋₀	RY/BY# (8)
Read Array	6	V _{IH}	V _{IL}	V _{IL}	V _{IH}	X	D _{OUT}	High Z
Output Disable		V _{IH}	V _{IL}	V _{IH}	V _{IH}	X	High Z	X
Standby		V _{IH}	V _{IH}	X	X	X	High Z	X
Reset	3	V_{IL}	X	X	X	X	High Z	High Z
Read Identifier Codes/OTP	6	V _{IH}	V _{IL}	V _{IL}	V _{IH}	See Table 3	See Table 3	High Z
Read Query	6,7	V_{IH}	V _{IL}	V_{IL}	V _{IH}	X	D _{OUT}	High Z
Read Status Register	6	V_{IH}	$V_{\rm IL}$	$V_{\rm IL}$	V _{IH}	X	D _{OUT}	X
Write	4,5,6	V_{IH}	V _{IL}	V _{IH}	V _{IL}	X	D _{IN}	X

- 1. Refer to DC Characteristics for \boldsymbol{V}_{IL} or \boldsymbol{V}_{IH} voltages.
- 2. X can be V_{IL} or V_{IH} for control pins and addresses.
 3. RST# at GND±0.2V ensures the lowest power consumption.
- 4. Command writes involving block erase, full chip erase, (page buffer) program or OTP program are reliably executed when $V_{CC}=2.7V-3.3V$.
- 5. Refer to Table 5 for valid D_{IN} during a write operation.
- 6. Never hold OE# low and WE# low at the same timing.
- 7. Query code = Common Flash Interface (CFI) code.
- 8. RY/BY# is V_{OL} when the WSM (Write State Machine) is executing internal block erase, full chip erase, (page buffer) program or OTP program algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with program and page buffer program inactive), (page buffer) program suspend mode, or reset mode.



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Bus First Bus Cycle Second Bus Cycle Command Cycles Notes Oper⁽¹⁾ Oper⁽¹⁾ Addr⁽²⁾ Data⁽³⁾ Addr⁽²⁾ Data Req'd Read Array Write PA **FFH** Read Identifier Codes/OTP ≥ 2 4 Write PA 90H Read IA or OA ID or OD Read Ouery ≥ 2 Write PA 98H Read **OA** OD 2 Write PA Read Status Register PA 70H Read **SRD** Write PA 50H Clear Status Register 1 **Block Erase** 2 5 Write BA 20H Write BA D₀H 2 5.9 30H Write X D₀H Full Chip Erase Write X 40H or **Program** 2 5.6 Write WA Write WA WD 10H Write WA E8H Write WA N-1 Page Buffer Program > 4 5.7 Block Erase and (Page Buffer) 1 8.9 Write B0H PA Program Suspend Block Erase and (Page Buffer) 1 8.9 Write PA D0H Program Resume Set Block Lock Bit 2 Write BA 60H Write BA 01H Clear Block Lock Bit 2 10 Write BA 60H Write BA D₀H 2 Write Set Block Lock-down Bit Write BA60H BA 2FH 2 Write OA C₀H Write OA OD **OTP Program**

Table 5. Command Definitions⁽¹¹⁾

NOTES:

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- 1. Bus operations are defined in Table 4.
- 2. All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.
 - X=Any valid address within the device.
 - PA=Address within the selected plane.
 - IA=Identifier codes address (See Table 3).
 - QA=Query codes address.
 - BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
 - WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
 - OA=Address of OTP block to be read or programmed (See Figure 3).
- 3. ID=Data read from identifier codes. (See Table 3).
 - QD=Data read from query database.
 - SRD=Data read from status register. See Table 9.1, Table 9.2 for a description of the status register bits.
 - WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.
 - OD=Data within OTP block. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.
 - N-1=N is the number of the words to be loaded into a page buffer.
- 4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code and the data within OTP block (See Table 3).
 - The Read Query command is available for reading CFI (Common Flash Interface) information.
- 5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is V_{IH} .
- 6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.



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- 7. Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H).
- 8. If the program operation in one plane is suspended and the erase operation in other plane is also suspended, the suspended program operation will be resumed first.
- 9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
- 10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP#/ACC is V_{IL} . When WP#/ACC is V_{IH} , lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
- 11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used



		(2)			
State	WP#/ACC	DQ ₁ ⁽¹⁾	$DQ_0^{(1)}$	State Name	Erase/Program Allowed (2)
[000]	0	0	0	Unlocked	Yes
[001] ⁽³⁾	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101] ⁽³⁾	1	0	1	Locked	No
[110] ⁽⁴⁾	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

Table 6. Functions of Block Lock⁽⁵⁾ and Block Lock-Down

NOTES:

- 1. $DQ_0=1$: a block is locked; $DQ_0=0$: a block is unlocked. $DQ_1=1$: a block is locked-down; $DQ_1=0$: a block is not locked-down.
- 2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
- 3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (WP#/ACC=0) or [101] (WP#/ACC=1), regardless of the states before power-off or reset operation.
- 4. When WP#/ACC is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
- 5. OTP (One Time Program) block has the lock function which is different from those described above.

	Current S	State		Result after Lock Command Written (Next State)			
State	WP#/ACC	DQ ₁	DQ_0	Set Lock ⁽¹⁾	Clear Lock ⁽¹⁾	Set Lock-down ⁽¹⁾	
[000]	0	0	0	[001]	No Change	[011] ⁽²⁾	
[001]	0	0	1	No Change ⁽³⁾	[000]	[011]	
[011]	0	1	1	No Change	No Change	No Change	
[100]	1	0	0	[101]	No Change	[111] ⁽²⁾	
[101]	1	0	1	No Change	[100]	[111]	
[110]	1	1	0	[111]	No Change	[111] ⁽²⁾	
[111]	1	1	1	No Change	[110]	No Change	

Table 7. Block Locking State Transitions upon Command Write⁽⁴⁾

- 1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
- 2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ₀=0), the corresponding block is locked-down and automatically locked at the same time.
- 3. "No Change" means that the state remains unchanged after the command written.
- 4. In this state transitions table, assumes that WP#/ACC is not changed and fixed V_{IL} or V_{IH} .



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Table 8. Block Locking State Transitions upon WP#/ACC Transition⁽⁴⁾

Danie Grate		Current Sta	ite		Result after WP#/ACC	Transition (Next State)
Previous State	State	WP#/ACC	DQ_1	DQ_0	WP#/ACC=0→1 ⁽¹⁾	WP#/ACC= $1 \rightarrow 0^{(1)}$
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
$[110]^{(2)}$					[110]	-
Other than [110] ⁽²⁾	[011]	0	1	1	[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	$[011]^{(3)}$
-	[111]	1	1	1	-	[011]

- 1. "WP#/ACC=0 \to 1" means that WP#/ACC is driven to V $_{IH}$ and "WP#/ACC=1 \to 0" means that WP#/ACC is driven to V $_{IL}$.
- 2. State transition from the current state [011] to the next state depends on the previous state.
- 3. When WP#/ACC is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
- 4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.



		Tal	ble 9.1. Status l	Register Definit	ion
GWSMS	GRESS	GREECES	GPRPOPS	GWPACCS	

GWSMS	GBESS	GBEFCES	GPBPOPS	GWPACCS	GPBPSS	GDPS	R
15	14	13	12	11	10	9	8
PWSMS	GBESS	GBEFCES	GPBPOPS	GWPACCS	GPBPSS	GDPS	R
7	6	5	4	3	2	1	0

NOTES:

SR.7 = PLANE WRITE STATE MACHINE STATUS (PWSMS)

- 1 = Ready
- 0 = Busy

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SR.6 = GLOBAL BLOCK ERASE SUSPEND STATUS (GBESS)

- 1 = Block Erase Suspended
- 0 = Block Erase in Progress/Completed

SR.5 = GLOBAL BLOCK ERASE AND FULL CHIP ERASE STATUS (GBEFCES)

- 1 = Error in Block Erase or Full Chip Erase
- 0 = Successful Block Erase or Full Chip Erase

SR.4 = GLOBAL (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (GPBPOPS)

- 1 = Error in (Page Buffer) Program or OTP Program
- 0 = Successful (Page Buffer) Program or OTP Program

SR.3 = GLOBAL WP#/ACC STATUS (GWPACCS)

- $1 = V_{CCO} + 0.4V < WP\#/ACC < 9.0V Detect,$ Operation Abort
- 0 = WP#/ACC OK

SR.2 = GLOBAL (PAGE BUFFER) PROGRAM SUSPEND STATUS (GPBPSS)

- 1 = (Page Buffer) Program Suspended
- 0 = (Page Buffer) Program in Progress/Completed

SR.1 = GLOBAL DEVICE PROTECT STATUS (GDPS)

- 1 = Erase or Program Attempted on a Locked Block, Operation Abort
- 0 = Unlocked

Status Register indicates the status of the WSM (Write State Machine). However, SR.7 indicates the status of WSM in each plane. Even if the SR.7 is "1", the WSM may be occupied by the other plane.

In the plane to which the command is issued, Check SR.7 or RY/BY# to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of WP#/ACC level. The WSM interrogates and indicates the WP#/ACC level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when WP#/ $ACC \neq V_{ACCH}$.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.

 $SR.0 = RESERVED \ FOR \ FUTURE \ ENHANCEMENTS \ (R) \ \Big|_{SR.0} \ is \ reserved \ for \ future \ use \ and \ should \ be \ masked \ out$ when polling the status register.



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Table 9.2. Status Register Definition (Continued)

SR.15 = GLOBAL WRITE STATE MACHINE STATUS (GWSMS)

1 = Ready

0 = Busy

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SR.14 = GLOBAL BLOCK ERASE SUSPEND STATUS (GBESS)

1 = Block Erase Suspended

0 = Block Erase in Progress/Completed

SR.13 = GLOBAL BLOCK ERASE AND FULL CHIP ERASE STATUS (GBEFCES)

1 = Error in Block Erase or Full Chip Erase

0 = Successful Block Erase or Full Chip Erase

SR.12 = GLOBAL (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (GPBPOPS)

1 = Error in (Page Buffer) Program or OTP Program

0 = Successful (Page Buffer) Program or OTP Program

SR.11 = GLOBAL WP#/ACC STATUS (GWPACCS)

 $1 = V_{CCO} + 0.4V < WPP\#/ACC < 9.0V$ Detect, **Operation Abort**

0 = WP#/ACCOK

SR.10 = GLOBAL (PAGE BUFFER) PROGRAM SUSPEND STATUS (GPBPSS)

1 = (Page Buffer) Program Suspended

0 = (Page Buffer) Program in Progress/Completed

SR.9 = GLOBAL DEVICE PROTECT STATUS (GDPS)

1 = Erase or Program Attempted on a Locked Block, Operation Abort

0 = Unlocked

NOTES:

Status Register SR.15-SR.9 indicates the status of the WSM.

Check SR.15 or RY/BY# to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.14 - SR.9 are invalid while SR.15="0".

If both SR.13 and SR.12 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit attempt, an improper command sequence was entered.

SR.11 does not provide a continuous indication of WP#/ACC level. The WSM interrogates and indicates the WP#/ACC level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.11 is not guaranteed to report accurate feedback when WP#/ $ACC \neq V_{ACCH}$.

SR.9 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.

 $SR.8 = RESERVED \ FOR \ FUTURE \ ENHANCEMENTS \ (R) \ \Big|_{SR.8} \ is \ reserved \ for \ future \ use \ and \ should \ be \ masked \ out$ when polling the status register.



Table 10.	Extended Stat	us Register	Definition
-----------	---------------	-------------	------------

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	1	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE
ENHANCEMENTS (R)

HARP

XSR.7 = STATE MACHINE STATUS (SMS)

1 = Page Buffer Program available

0 = Page Buffer Program not available

XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.

XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.





1 Electrical Specifications

1.1 Absolute Maximum Ratings*

Operating Temperature

During Read, Erase and Program ...-40°C to +85°C (1)

Storage Temperature

During under Bias.....-40°C to +85°C During non Bias....-65°C to +125°C

Voltage On Any Pin (except V_{CC}, V_{CCO} and WP#/ACC)

.....-0.5V to V_{CCO}+0.5V ⁽²⁾

 V_{CC} and V_{CCO} Supply Voltage -0.2V to +3.7V $^{(2)}$

WP#/ACC Supply Voltage -0.2V to +10.3V (2, 3, 4)

Output Short Circuit Current 100mA (5)

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

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NOTES:

- 1. Operating temperature is for extended temperature product defined by this specification.
- 2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} , V_{CCQ} and WP#/ACC pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC} +0.5V which, during transitions, may overshoot to V_{CC} +2.0V for periods <20ns.
- 3. Maximum DC voltage on WP#/ACC may overshoot to +11.0V for periods <20ns.
- 4. WP#/ACC erase/program voltage is normally 2.7V-3.3V. Applying 9.0V-10.0V to WP#/ACC during erase/program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. WP#/ACC may be connected to 9.0V-10.0V for a total of 80 hours maximum.
- 5. Output shorted for no more than one second. No more than one output shorted at a time.

1.2 Operating Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Operating Temperature	T_A	-40	+25	+85	°C	
V _{CC} Supply Voltage	V _{CC}	2.7	3.0	3.3	V	1
I/O Supply Voltage	V _{CCQ}	2.7	3.0	3.3	V	1
WD##AGGWI	V_{IL}	-0.2		0.4	V	
WP#/ACC Voltage when Used as a Logic Control	V _{IH}	2.4		V _{CCQ} + 0.4	V	1
WP#/ACC Supply Voltage	V _{ACCH}	9.0	9.5	10.0	V	1, 2
Main Block Erase Cycling: WP#/ACC=V _{IL} or V _{IH}		100,000			Cycles	
Parameter Block Erase Cycling: WP#/ACC=V _{IL} or V _{IH}		100,000			Cycles	
Main Block Erase Cycling: WP#/ACC=V _{ACCH} , 80 hrs.				1,000	Cycles	
Parameter Block Erase Cycling: WP#/ACC=V _{ACCH} , 80 hrs.				1,000	Cycles	
Maximum WP#/ACC hours at VACCH				80	Hours	

- 1. See DC Characteristics tables for voltage range-specific specification.
- 2. Applying WP#/ACC=9.0V-10.0V during a erase or program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. A permanent connection to WP#/ACC=9.0V-10.0V is not allowed and can cause damage to the device.



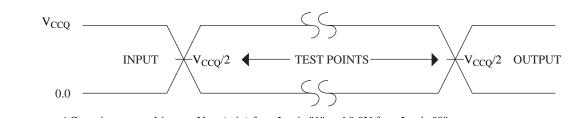
1.2.1 Capacitance $^{(1)}$ (T_A=+25°C, f=1MHz)

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input Capacitance	C_{IN}	V _{IN} =0.0V		4	7	pF
WP#/ACC Input Capacitance	C _{IN}	V _{IN} =0.0V		18	22	pF
Output Capacitance	C_{OUT}	V _{OUT} =0.0V		6	10	pF

NOTE:

1. Sampled, not 100% tested.

1.2.2 AC Input/Output Test Conditions



AC test inputs are driven at $V_{CCQ}(min)$ for a Logic "1" and 0.0V for a Logic "0". Input timing begins, and output timing ends at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5ns. Worst case speed conditions are when $V_{CC}=V_{CC}(min)$.

Figure 4. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.3V

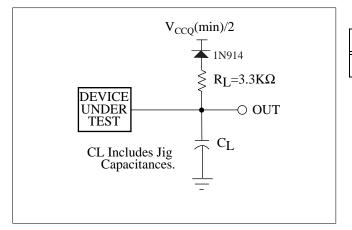


Figure 5. Transient Equivalent Testing Load Circuit

Table 11. Test Configuration Capacitance Loading Value

Test Configuration	$C_L(pF)$
V _{CC} =2.7V-3.3V	50



1.2.3 DC Characteristics

$V_{CC} = 2.7V - 3.3V$

Symbol	Param	eter	Notes	Min.	Тур.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	-1.0		+1.0	μΑ	V _{CC} =V _{CC} Max.,
I_{LO}	Output Leakage Current		1	-1.0		+1.0	μΑ	$V_{CCQ} = V_{CCQ}Max.,$ $V_{IN}/V_{OUT} = V_{CCQ} \text{ or }$ GND
I_{CCS}	V _{CC} Standby Current		1,7,8		9	40	μА	$V_{CC} = V_{CC} Max.,$ $CE \# = RST \# =$ $V_{CCQ} \pm 0.2 V,$ $WP \# / ACC = V_{CCQ} \text{ or }$ GND
I _{CCAS}	V _{CC} Automatic Power Savings Current		1,3,7		9	40	μA	V _{CC} =V _{CC} Max., CE#=GND±0.2V, WP#/ACC=V _{CCQ} or GND
I_{CCD}	V _{CC} Reset Current		1,7		9	40	μΑ	RST#=GND±0.2V
T	Average V _{CC} Read Current Normal Mode		1,6,7		20	30	mA	V _{CC} =V _{CC} Max., CE#=V _{IL} ,
I_{CCR}	Average V _{CC} Read Current Page Mode	8 Word Read	1,6,7		5	10	mA	OE#=V _{IH} , f=5MHz
T	V _{CC} (Page Buffer) P	rogram Current	1,4,6,7		20	60	mA	WP#/ACC=V _{IL} or V _{IH}
I_{CCW}	VCC (Fage Bullet) F	rogram Current	1,4,6,7		10	20	mA	WP#/ACC=V _{ACCH}
I	V _{CC} Block Erase,		1,4,6,7		10	30	mA	WP#/ACC=V _{IL} or V _{IH}
I_{CCE}	Full Chip Erase Curr	rent	1,4,6,7		4	10	mA	WP#/ACC=V _{ACCH}
I _{CCWS} I _{CCES}	V _{CC} (Page Buffer) P Block Erase Suspend	-	1,2,6,7		10	200	μА	CE#=V _{IH}
I _{ACCS} I _{ACCR}	WP#/ACC Standby	or Read Current	1,5,6,7		2	5	μΑ	WP#/ACC≤V _{CC}
I_{ACCW}	WP#/ACC (Page	Buffer) Program	1,4,5,6,7		2	5	μΑ	WP#/ACC=V _{IL} or V _{IH}
ACCW	Current		1,4,5,6,7		10	30	mA	WP#/ACC=V _{ACCH}
Lagge	WP#/ACC Block Era		1,4,5,6,7		2	5	μΑ	WP#/ACC=V _{IL} or V _{IH}
I _{ACCE}	Full Chip Erase Current		1,4,5,6,7		5	15	mA	WP#/ACC=V _{ACCH}
I _{ACCWS}	WP#/ACC (Page Bu	ffer) Program	1,5,6,7		2	5	μΑ	WP#/ACC=V _{IL} or V _{IH}
-ACCWS	Suspend Current		1,5,6,7		10	200	μΑ	WP#/ACC=V _{ACCH}
I _{ACCES}		Erase Suspend	1,5,6,7		2	5	μΑ	WP#/ACC=V _{IL} or V _{IH}
-ACCES	Current		1,5,6,7		10	200	μΑ	WP#/ACC=V _{ACCH}

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DC Characteristics (Continued)

$V_{CC} = 2.7V - 3.3V$

Symbol	Parameter	Notes	Min.	Тур.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	5	-0.4		0.4	V	
V _{IH}	Input High Voltage	4	2.4		V _{CCQ} + 0.4	V	
V _{OL}	Output Low Voltage	4,8			0.2	V	$V_{CC}=V_{CC}Min.,$ $V_{CCQ}=V_{CCQ}Min.,$ $I_{OL}=100\mu A$
V _{OH}	Output High Voltage	4	V _{CCQ} -0.2			V	$V_{CC}=V_{CC}Min.,$ $V_{CCQ}=V_{CCQ}Min.,$ $I_{OH}=-100\mu A$
V _{ACCH}	WP#/ACC during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations		9.0	9.5	10.0	V	
V_{LKO}	V _{CC} Lockout Voltage		1.5			V	

NOTES:

- 1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC} =3.0V, V_{CCQ} =3.0V and T_A =+25°C unless V_{CC} is specified.
- 2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW} . If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR} .
- 3. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVOV}) provide new data when addresses are changed.
- 4. Sampled, not 100% tested.
- 5. Applying 9.5V±0.5V to WP#/ACC provides fast erasing or fast programming mode. In this mode, WP#/ACC is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the V_{CC} power bus.

Applying 9.5V±0.5V to WP#/ACC during erase/program can only be done for a maximum of 1,000 cycles on each block. WP#/ACC may be connected to 9.5V±0.5V for a total of 80 hours maximum.

- 6. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.
- 7. For all pins other than those shown in test conditions, input level is V_{CCO} or GND.
- 8. Includes RY/BY#.





1.2.4 AC Characteristics - Read-Only Operations⁽¹⁾

V_{CC} =2.7V-3.3V, T_A =-40°C to +85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Read Cycle Time		75		ns
t _{AVQV}	Address to Output Delay			75	ns
t _{ELQV}	CE# to Output Delay	3		75	ns
t _{APA}	Page Address Access Time			25	ns
t _{GLQV}	OE# to Output Delay	3		20	ns
t _{PHQV}	RST# High to Output Delay			150	ns
$t_{\rm EHQZ},t_{\rm GHQZ}$	CE# or OE# to Output in High Z, Whichever Occurs First	2		20	ns
$t_{\rm ELQX}$	CE# to Output in Low Z	2	0		ns
t_{GLQX}	OE# to Output in Low Z	2	0		ns
t _{OH}	Output Hold from First Occurring Address, CE# or OE# change	2	0		ns
t _{AVEL} , t _{AVGL}	Address Setup to CE#, OE# Going Low for Reading Status Register	4, 6	10		ns
t _{ELAX} , t _{GLAX}	Address Hold from CE#, OE# Going Low for Reading Status Register	5, 6	10		ns
t _{EHEL} , t _{GHGL}	CE#, OE# Pulse Width High for Reading Status Register	6	20		ns

- 1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
- 2. Sampled, not 100% tested.

- OE# may be delayed up to t_{ELQV} t_{GLQV} after the falling edge of CE# without impact to t_{ELQV}.
 Address setup time (t_{AVEL}, t_{AVGL}) is defined from the falling edge of CE# or OE# (whichever goes low last).
 Address hold time (t_{ELAX}, t_{GLAX}) is defined from the falling edge of CE# or OE# (whichever goes low last).
 Specifications t_{AVEL}, t_{AVGL}, t_{ELAX}, t_{GLAX} and t_{EHEL}, t_{GHGL} for read operations apply to only status register read operations.



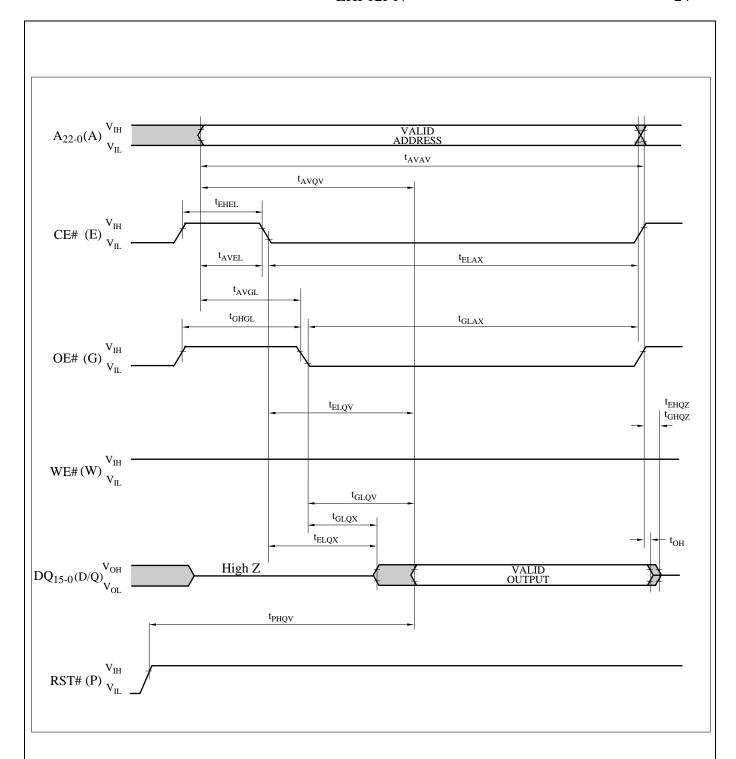


Figure 6. AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes, OTP Block or Query Code



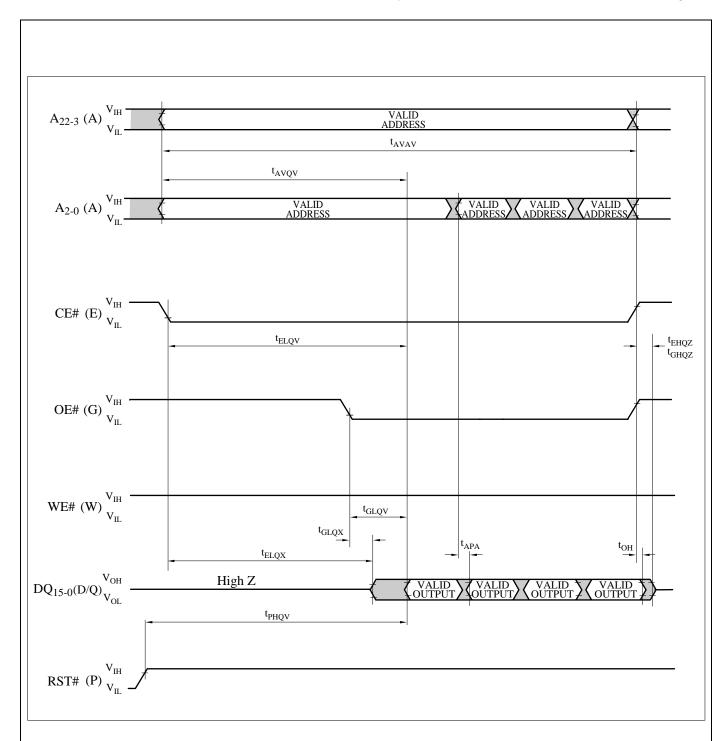


Figure 7. AC Waveform for Asynchronous 4-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



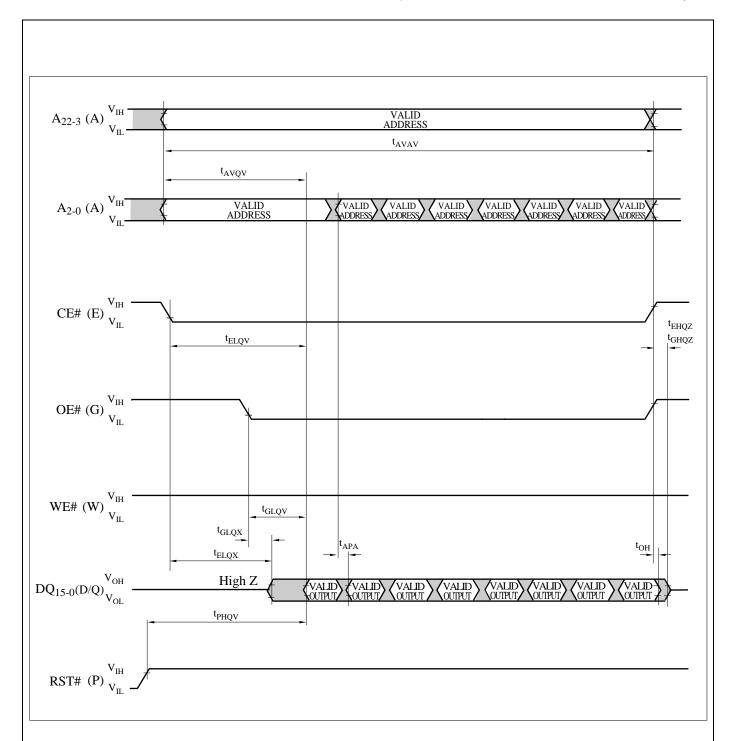


Figure 8. AC Waveform for Asynchronous 8-Word Page Mode Read Operations from Main Blocks or Parameter Blocks





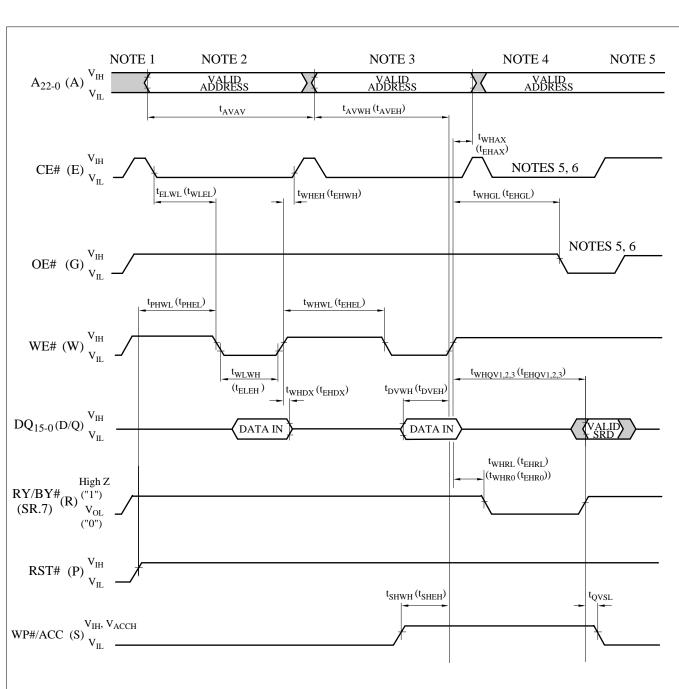
1.2.5 AC Characteristics - Write Operations^{(1), (2)}

V_{CC} =2.7V-3.3V, T_{A} =-40°C to +85°C

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{AVAV}	Write Cycle Time		75		ns
t _{PHWL} (t _{PHEL})	RST# High Recovery to WE# (CE#) Going Low	3	150		ns
t _{ELWL} (t _{WLEL})	CE# (WE#) Setup to WE# (CE#) Going Low		0		ns
t _{WLWH} (t _{ELEH})	WE# (CE#) Pulse Width	4	50		ns
t _{DVWH} (t _{DVEH})	Data Setup to WE# (CE#) Going High	7	40		ns
t _{AVWH} (t _{AVEH})	Address Setup to WE# (CE#) Going High	7	40		ns
t _{WHEH} (t _{EHWH})	CE# (WE#) Hold from WE# (CE#) High		0		ns
$t_{WHDX} (t_{EHDX})$	Data Hold from WE# (CE#) High		0		ns
$t_{WHAX} (t_{EHAX})$	Address Hold from WE# (CE#) High		0		ns
$t_{WHWL} (t_{EHEL})$	WE# (CE#) Pulse Width High	5	25		ns
t _{SHWH} (t _{SHEH})	WP#/ACC High Setup to WE# (CE#) WP#/ACC=VIH	3	0		ns
'SHWH ('SHEH)	Going High WP#/ACC=V _{ACCH}		200		118
$t_{WHGL} (t_{EHGL})$	Write Recovery before Read		30		ns
t _{QVSL}	WP#/ACC High Hold from Valid SRD, RY/BY# High Z	3	0		ns
t _{WHR0} (t _{EHR0})	WE# (CE#) High to SR.7 Going "0"	3, 6		t _{AVQV} +50	ns
$t_{WHRL} (t_{EHRL})$	WE# (CE#) High to RY/BY# Going Low	3		100	ns

- 1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
- 2. A write operation can be initiated and terminated with either CE# or WE#.
- 3. Sampled, not 100% tested.
- 4. Write pulse width (t_{WP}) is defined from the falling edge of CE# or WE# (whichever goes low last) to the rising edge of CE# or WE# (whichever goes high first). Hence, t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH} .
- 5. Write pulse width high (t_{WPH}) is defined from the rising edge of CE# or WE# (whichever goes high first) to the falling edge of CE# or WE# (whichever goes low last). Hence, t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL} .
- 6. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes/OTP command=t_{AVOV}+100ns.
- 7. Refer to Table 5 for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.





- 1. V_{CC} power-up and standby.
- 2. Write each first cycle command.
- 3. Write each second cycle command or valid address and data.
- 4. Automated erase or program delay.
- 5. Read status register data.
- 6. For read operation, OE# and CE# must be driven active, and WE# de-asserted.

Figure 9. AC Waveform for Write Operations





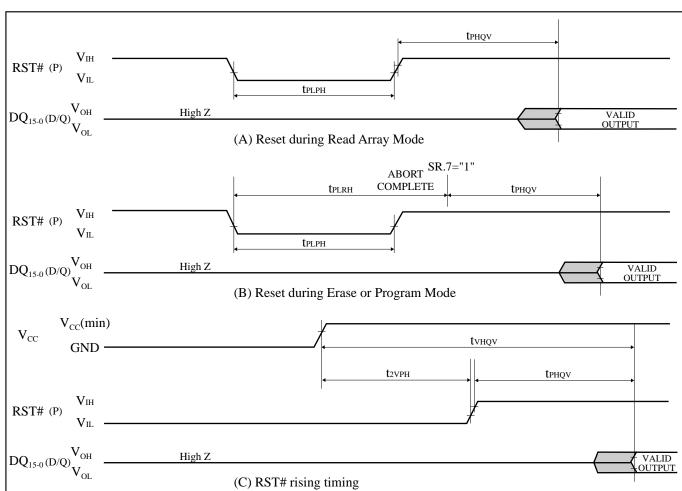


Figure 10. AC Waveform for Reset Operations

Reset AC Specifications (V $_{CC}$ =2.7V-3.3V, T $_{A}$ =-40°C to +85°C)

Symbol	Parameter	Notes	Min.	Max.	Unit
t _{PLPH}	RST# Low to Reset during Read (RST# should be low during power-up.)		100		ns
t _{PLRH}	RST# Low to Reset during Erase or Program	1, 3, 4		22	μs
t _{2VPH}	V _{CC} 2.7V to RST# High	1, 3, 5	100		ns
t_{VHQV}	V _{CC} 2.7V to Output Delay	3		1	ms

- 1. A reset time, t_{PHQV}, is required from the later of SR.7 (RY/BY#) going "1" (High Z) or RST# going high until outputs are valid. Refer to AC Characteristics Read-Only Operations for t_{PHQV}.
- 2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
- 3. Sampled, not 100% tested.
- 4. If RST# asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
- 5. When the device power-up, holding RST# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.





1.2.7 Block Erase, Full Chip Erase, (Page Buffer) Program and OTP Program Performance⁽³⁾

 V_{CC} =2.7V-3.3V, T_{A} =-40°C to +85°C

Symbol	Parameter	Notes	Page Buffer Command is	111			WP#/ACC=V _{ACCH} (In Manufacturing)			Unit
			Used or not Used	Min.	Typ.(1)	Max. ⁽²⁾	Min.	Typ.(1)	Max. ⁽²⁾	
t_{WPB}	4-Kword Parameter Block	2	Not Used		0.05	0.3		0.04	0.12	S
WPB	Program Time	2	Used		0.03	0.12		0.02	0.06	S
$t_{ m WMB}$	32-Kword Main Block	2	Not Used		0.38	2.4		0.31	1.0	s
WMB	Program Time	2	Used		0.24	1.0		0.17	0.5	S
t _{WHQV1} /	Word Program Time	2	Not Used		11	200		9	185	μs
t_{EHQV1}	I word Program Time		Used		7	100		5	90	μs
$t_{\mathrm{WHOV1}}/$ t_{EHOV1}	OTP Program Time	2	Not Used		36	400		27	185	μs
t _{WHQV2} / t _{EHQV2}	4-Kword Parameter Block Erase Time	2	-		0.5	4		0.4	4	s
t _{WHQV3} / t _{EHQV3}	32-Kword Main Block Erase Time	2	-		0.9	5		0.8	5	s
	Full Chip Erase Time	2			240	1400		200	1400	S
$t_{\mathrm{WHRH1}}/$ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10		5	10	μs
t _{WHRH2} / t _{EHRH2}	Block Erase Suspend Latency Time to Read	4	-		5	20		5	20	μs
t _{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			500			μs

- 1. Typical values measured at V_{CC} =3.0V, WP#/ACC=3.0V or 9.5V, and T_A =+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
- 2. Excludes external system-level overhead.
- 3. Sampled, but not 100% tested.
- 4. A latency time is required from writing suspend command (WE# or CE# going high) until SR.7 going "1" or RY/BY# going High Z.
- 5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.



A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

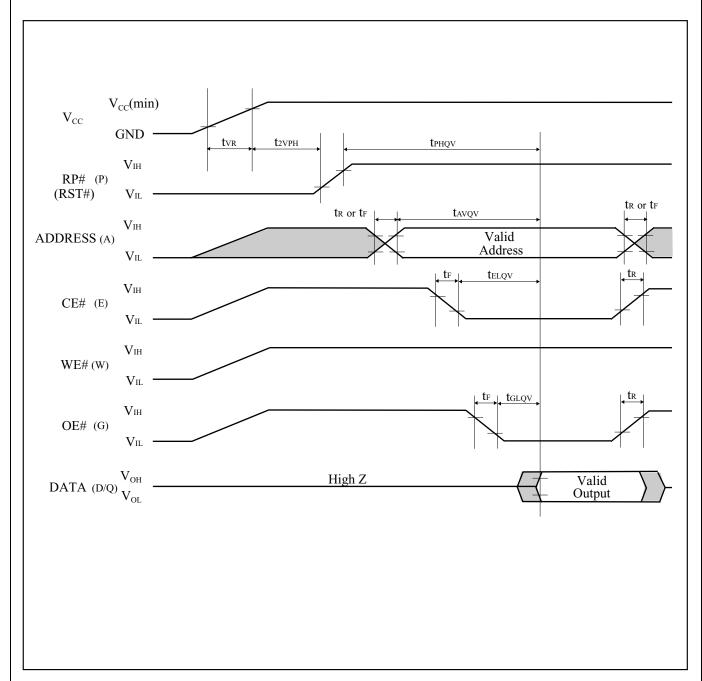


Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR} , t_R , t_F in the figure, refer to the next page. See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.



A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	V _{CC} Rise Time	1	0.5	30000	μs/V
t _R	Input Signal Rise Time			1	μs/V
t _F	Input Signal Fall Time	1, 2		1	μs/V

NOTES:

- Sampled, not 100% tested.
 This specification is applied for not only the device power-up but also the normal operations.

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A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

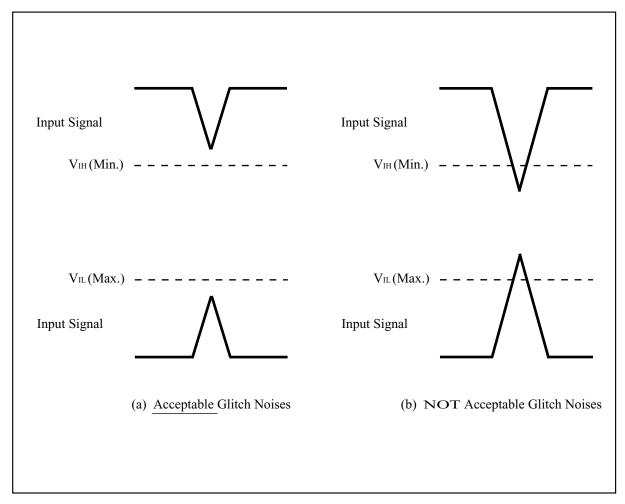


Figure A-2. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for $V_{IH}\,(\mbox{Min.})$ and $V_{IL}\,(\mbox{Max.}).$



A-2 RELATED DOCUMENT INFORMATION $^{(1)}$

Document No.	Document Name		
AP-001-SD-E	Flash Memory Family Software Drivers		
AP-006-PT-E	Data Protection Method of SHARP Flash Memory		
AP-007-SW-E	RP#, V _{PP} Electric Potential Switching Circuit		

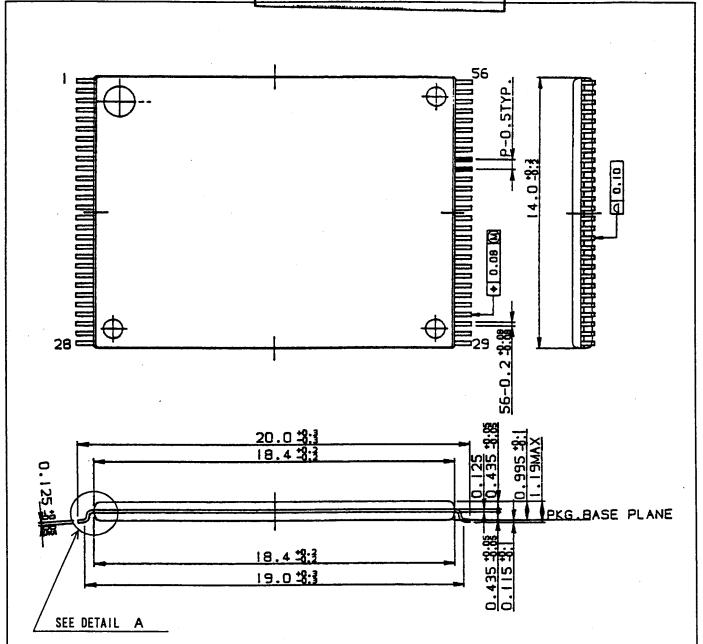
NOTE:

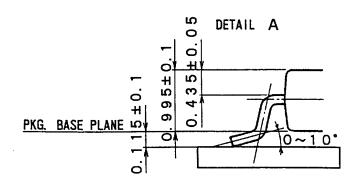
1. International customers should contact their local SHARP or distribution sales office.

Rev. 1.10

SHARP

PRELIMINARY





名称	リード仕上	TIN-LEAD 備考	プラスチックパッケージ外形寸法は、バリを含まないものとする。
NAME TSOP56-P-1420	LEAD FINISH	PLATING NOTE	Plastic body dimensions do not

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