NANDxxxxMx

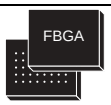
256/512-Mbit or 1-Gbit (x8/x16, 1.8/2.6 V, 528-byte page) NAND flash and 256/512-Mbit (x16/x32, 1.8 V) LPSDRAM, MCP or PoP

Features

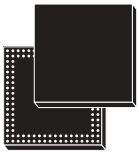
- Packages
  - MCP (multichip package)
  - PoP (package on package)
- Device composition
  - 1 die of 256 or 512 Mbits or 1 Gbit (x8/x16) SLC small page NAND flash memory
  - 1 die of 256 or 512 Mbits (x16 or x32) SDR/DDR LPSDRAM
- Supply voltages
  - V_{DDF} = 1.7 V to 1.95 V or 2.5 V to 3.6 V
  - V_{DDD} = V_{DDQD} = 1.7 V to 1.95 V
- Electronic signature
- ECOPACK® packages
- Temperature range: –30 to 85 °C

Flash memory

- NAND interface
  - x8/x16 bus width
  - Multiplexed address/data
- Page size
  - x8 device: (512 + 16 spare) bytes
  - x16 device: (256 + 8 spare) words
- Block size
  - x8 device: (16K + 512 spare) bytes
  - x16 device: (8K + 256 spare) words
- Page read/program
  - Random access: 12 µs (3 V), 15 µs (1.8 V)
  - Sequential access: 30 ns (3 V), 50 ns (1.8 V)
  - Page program time: 200 µs (typ)
- Copy back program mode
  - Fast page copy without external buffering
- Fast block erase
  - Block erase time: 2 ms (typ)
  - Status register



TFBGA107 10.5 × 13 × 1.2 mm (ZBB)
TFBGA149 10 × 13.5 × 1.2 mm (ZBA)
TFBGA137 10.5 × 13 × 1.2 mm (ZBC)



TFBGA152 14 x 14 x 1.1 mm

- Data integrity
  - 100 000 program/erase cycles
  - 10 years data retention

Single or double data rate LPSDRAM

- Interface: ×16 or ×32 bus width
- Deep power-down mode
- 1.8 V LVCMOS interface
- Quad internal banks controlled by BA0, BA1
- Automatic and controlled precharge
- Auto refresh and self refresh
  - 8 192 refresh cycles/64 ms
  - Programmable partial array self refresh
  - Auto temperature compensated self refresh
- Wrap sequence: sequential/interleave
- Burst termination by Burst Stop command and Precharge command

Table 1. Device summary

NANDxxxxMx	NAND88R3M0	NAND99W3M0
	NAND98R3M0	NAND99W3M1
	NAND98W3M0	NANDA9W3M1
	NAND99R3M0	NAND99R4M2
	NAND99R3M2	NAND98W3M1
	NAND98R3M1	NAND98R3M2

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1 Description

The NANDxxxxMx devices (see *Table 1: Device summary* for the list of devices) combine two memory devices in a multichip package:

- 256-Mbit, 512-Mbit, or 1-Gbit SLC small page NAND flash memory, and either:
- 256-Mbit or 512-Mbit SDR (single data rate) LPSDRAM or
- 256-Mbit or 512-Mbit DDR (double data rate) LPSDRAM

The NAND flash memory and LPSDRAM components have separate power supplies and grounds. They also have separate control, address and input/output signals; this allows simultaneous access to both devices at any moment. The NAND flash memory and LPSDRAM components are distinguished by a Chip Enable input, $\overline{E}_F$, for the NAND flash memory and a Chip Select, $\overline{E}_D$, for the LPSDRAM. See *Figure 1* and *Figure 2* in conjunction with *Table 4* and *Table 5* for an overview of the signals associated with each component.

The NANDxxxxMx devices are available with a 1.8 V or 2.6 V voltage supply and are offered in the following packages as shown in *Table 2: Product list*:

- TFBGA107 (10.5 × 13 × 1.2 mm)
- TFBGA149 (10 × 13.5 × 1.2 mm)
- TFBGA137 (10.5 × 13 × 1.2 mm)
- TFBGA152 (14 × 14 × 1.1 mm)

The memories are supplied with all the NAND flash memory bits erased (set to '1').

This datasheet should be read in conjunction with the SLC small page NAND flash memory and LPSDRAM datasheets.

Table 2. Product list

Root part number	NAND product	LPSDRAM product	Package
NAND88R3M0	256 Mbits (×8) - 1.8 V	SDR 256 Mbits (×16) 1.8 V, 133 MHz	TFBGA107
NAND99R3M0	512 Mbits (×8) - 1.8 V	SDR 512 Mbits (×16) 1.8 V, 133 MHz	TFBGA149
NAND98R3M0	512 Mbits (×8) - 1.8 V	SDR 256 Mbits (×16) 1.8 V, 133 MHz	TFBGA107
			TFBGA149
			TFBGA152
NAND99W3M1	512 Mbits (×8) - 2.6 V	SDR 512 Mbits (×32) 1.8 V, 133 MHz	TFBGA137
NAND99W3M0	512 Mbits (×8) - 2.6 V	SDR 512 Mbits (×16) 1.8 V, 133 MHz	TFBGA107
NAND98W3M0	512 Mbits (×8) - 2.6 V	SDR 256 Mbits (×16) 1.8 V, 133 MHz	TFBGA107
NANDA9W3M1	1 Gbit (x8) - 2.6 V	SDR 512 Mbits (x32) 1.8 V, 133 MHz	TFBGA 137
NAND99R4M2	512 Mbits (x16) - 1.8 V	DDR 512 Mbits (x16) 1.8 V, 133 MHz	TFBGA 149
NAND99R3M2	512 Mbits (×8) - 1.8 V	DDR 512 Mbits (x16) 1.8 V, 133 MHz	TFBGA107
NAND98W3M1	512 Mbits (×8) - 2.6 V	SDR 256 Mbits (x32) 1.8 V, 133 MHz	TFBGA 137
NAND98R3M1	512 Mbits (×8) - 1.8 V	SDR 256 Mbits (x32) 1.8 V, 133 MHz	TFBGA 137
NAND98R3M2	512 Mbits (x8) - 1.8 V	DDR 256 Mbits (x16) 1.8 V, 133 MHz	TFBGA 107

1.1 NAND flash memory component

The NANDxxxxMx devices have a 1.8 V or 2.6 V power supply and contain 1 die of NAND flash memory with the following features:

- 256 Mbits, 512 Mbits, or 1 Gbit
- x8/x16 bus width
- Chip Enable ‘don’t care’ option

Table 2 specifies the type of NAND flash memory component contained in each product.

For detailed information on how to use the SLC small page NAND flash memory devices, refer to the respective datasheets, which are available on the internet site *http://www.numonyx.com,* or from your local Numonyx distributor.

1.2 LPSDRAM component

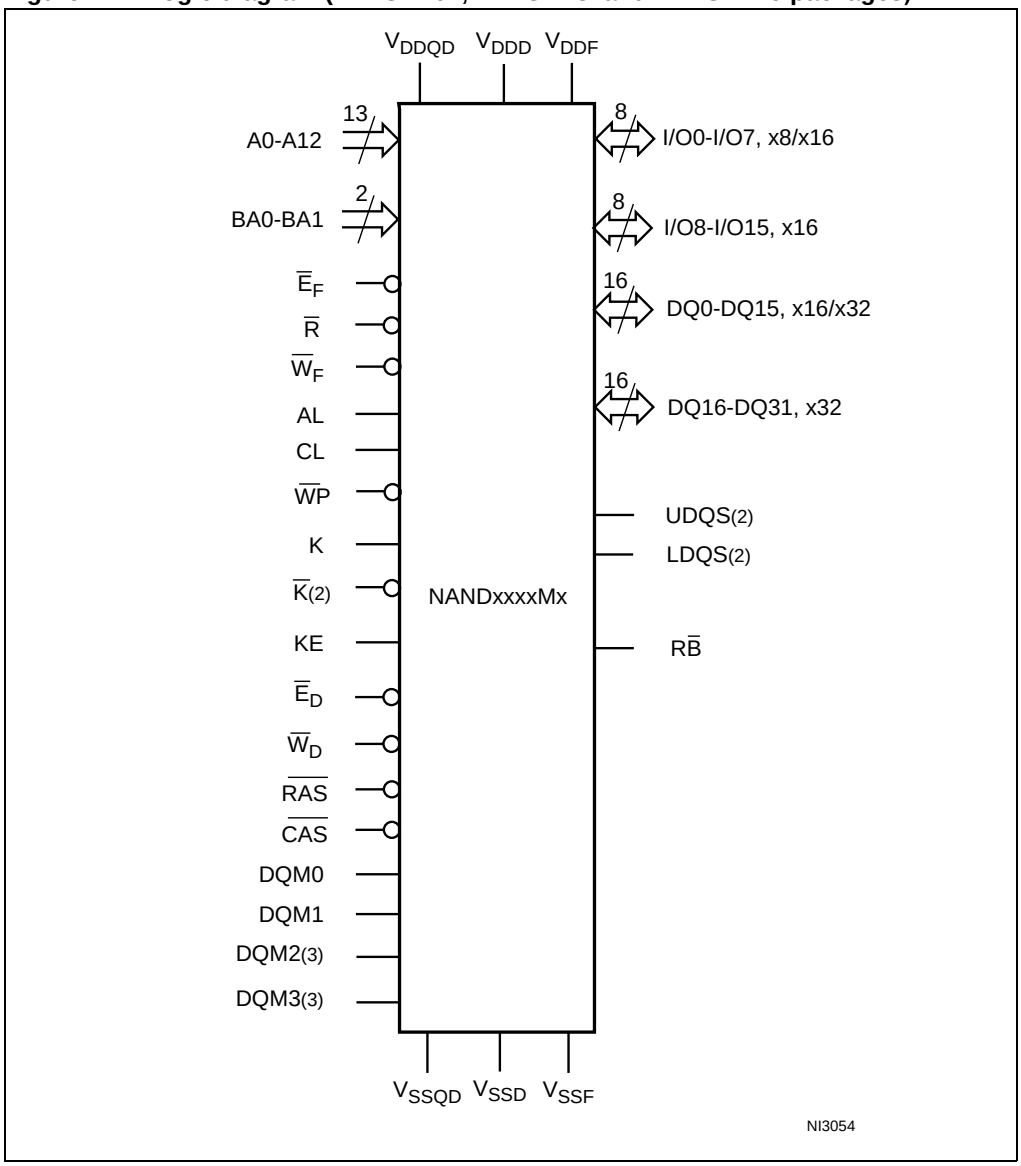
Table 3 provides details on the SDR or DDR LPSDRAM component contained in each device.

Table 3. LPSDRAM details

Root part number	LPSDRAM type	LPSDRAM name
NAND88R3M0 NAND98W3M0	256 Mbits (x16) single data rate	M65KA256AF
NAND98R3M0 (TFBGA152)	256 Mbits (x16) single data rate	M65KA256AF
NAND99R3M0 NAND99W3M0	512 Mbits (x16) single data rate	M65KA512AB
NAND99W3M1 NANDA9W3M1	512 Mbits (x32) single data rate	M65KC512AB or M65KC512AC
NAND99R4M2	512 Mbits (x16) double data rate	M65KG512AH
NAND99R3M2	512 Mbits (x16) double data rate	M65KG512AH
NAND98W3M1	256 Mbits (x32) single data rate	M65KA256AJ
NAND98R3M1	256 Mbits (x32) single data rate	M65KA256AJ
NAND98R3M0 (TFBGA107 and TFBGA149)	256 Mbits (x16) single data rate	M65KA256AF or M65KA256AJ
NAND98R3M2	256 Mbits (x16) double data rate	M65KG256AJ

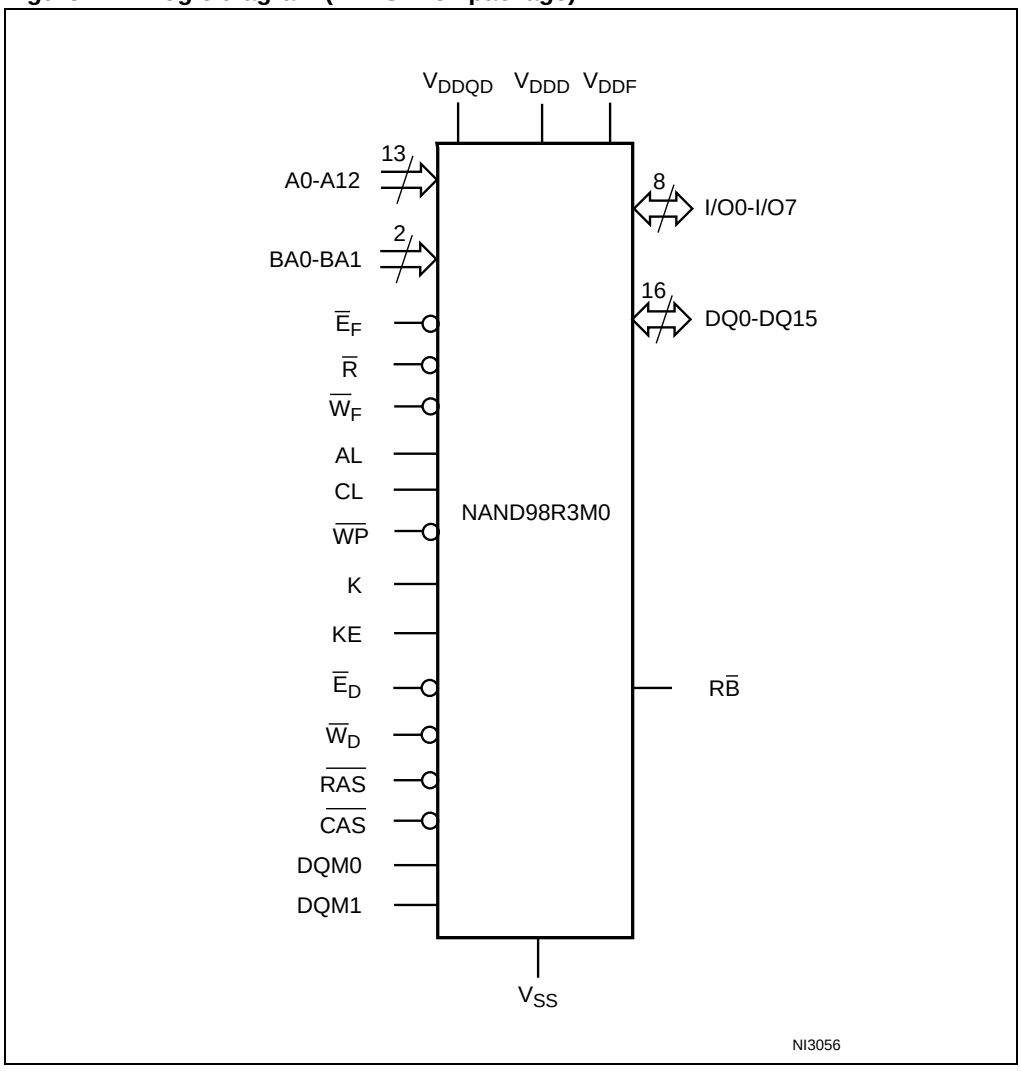
For detailed information on how to use the SDR/DDR LPSDRAM devices, refer to the M65KA256AF, M65KA512AB, M65KC512AB, M65KC512AC, M65KG512AH, M65KAxxxAJ, and M65KGxxxAJ datasheets available from your local Numonyx distributor.

Figure 1. Logic diagram (TFBGA107, TFBGA137and TFBGA149 packages)



1. See *Table 4* for the description of the signals related to these packages.
2. $\overline{K}$ is only available in MCP with DDR, LDQS, and UDQS are only available in MCP with DDR x16.
3. DQM2 and DQM3 are only available in MCP with SDR/DDR x32.

Figure 2. Logic diagram (TFBGA152 package)



1. See *Table 5* for the description of the signals related to these packages.

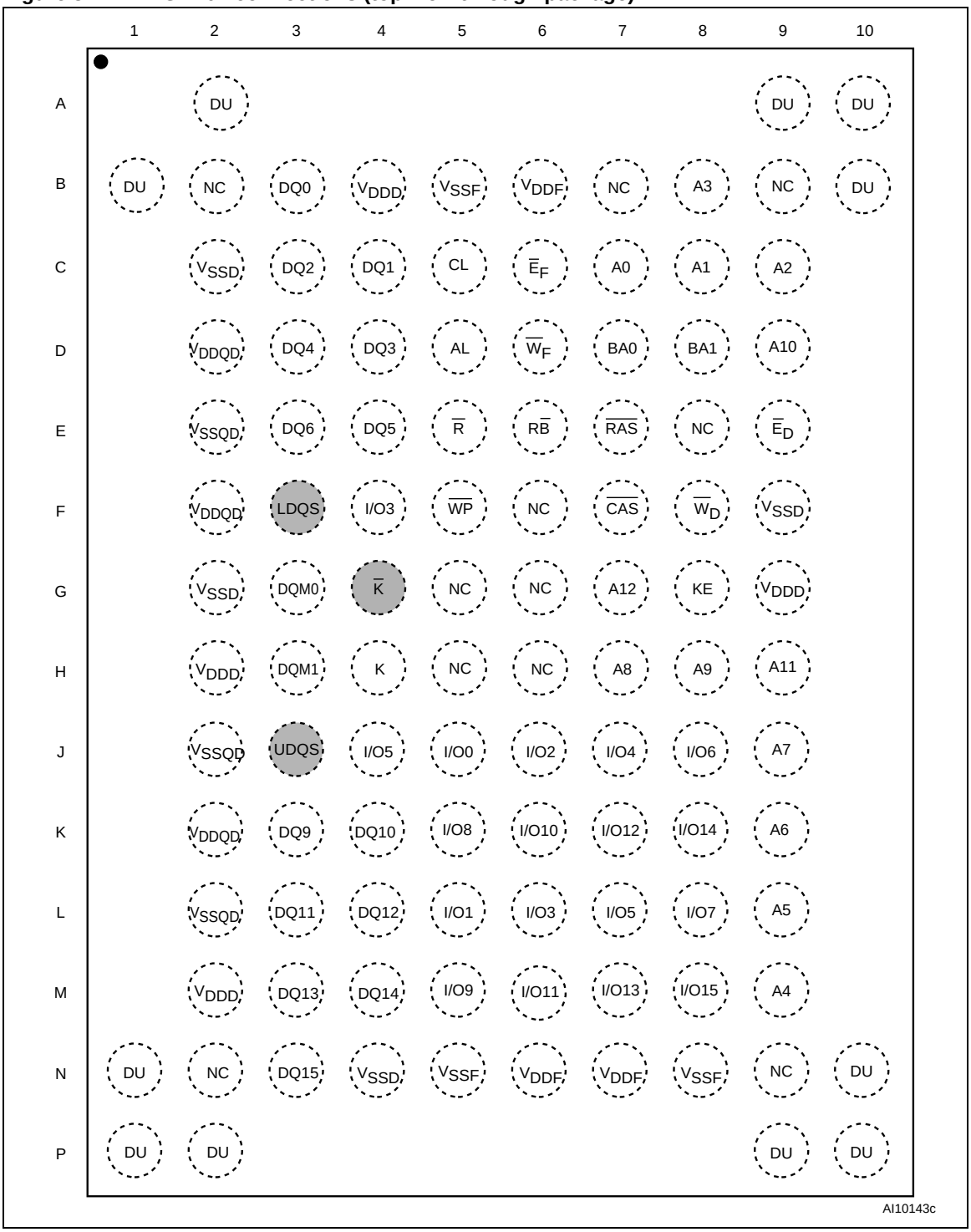
Table 4. Signal names (TFBGA107, TFBGA137 and TFBGA149 packages)

	Signal	Function	Direction
NAND flash memory	I/O0-I/O7	Data inputs/outputs for x8/x16 devices	Input/output
	I/O8-I/O15	Data inputs/outputs for x16 devices	Input/output
	AL	Address Latch Enable	Input
	CL	Command Latch Enable	Input
	$\overline{E}_F$	Chip Enable	Input
	$\overline{R}$	Read Enable	Input
	$R\overline{B}$	Ready/Busy (open-drain output)	Output
	$\overline{W}_F$	Write Enable	Input
	$\overline{WP}$	Write Protect	Input
	V_{DDF}	Supply voltage	Power supply
	V_{SSF}	Ground	Ground
LPSDRAM	A0-A12	Row address: A0-A12 Column address: – A0-A8 (256 Mbits and 512 Mbits x32) – A0-A9 (512 Mbits x16) Auto-precharge flag: A10	Input
	BA0-BA1	Bank address	Input
	DQ0-DQ15	Data inputs/outputs, ×16/×32	Input/output
	DQ16-DQ31	Data inputs/outputs, ×32	Input/output
	K, $\overline{K}$	Clock	Input
	KE	Clock Enable	Input
	$\overline{E}_D$	Chip Select	Input
	$\overline{W}_D$	Write Enable	Input
	$\overline{RAS}$	Row Address Strobe	Input
	$\overline{CAS}$	Column Address Strobe	Input
	DQM0	DQ Mask Enable (controls DQ0-DQ7, ×16/×32)	Input/output
	DQM1	DQ Mask Enable (controls DQ8-DQ15, ×16/×32)	Input/output
	DQM2	DQ Mask Enable (controls DQ16-DQ23, ×32)	Input/output
	DQM3	DQ Mask Enable (controls DQ24-DQ31, ×32)	Input/output
	UDQM	Upper Data Read Strobe (DDR x16)	Input/output
	LDQM	Lower Data Write Strobe (DDR x16)	Input/output
	V_{SSD}	Ground	Ground
	V_{SSQD}	Input/output ground	Ground
	NC	Not connected internally	N/A

Table 5. Signal names (TFBGA152 package)

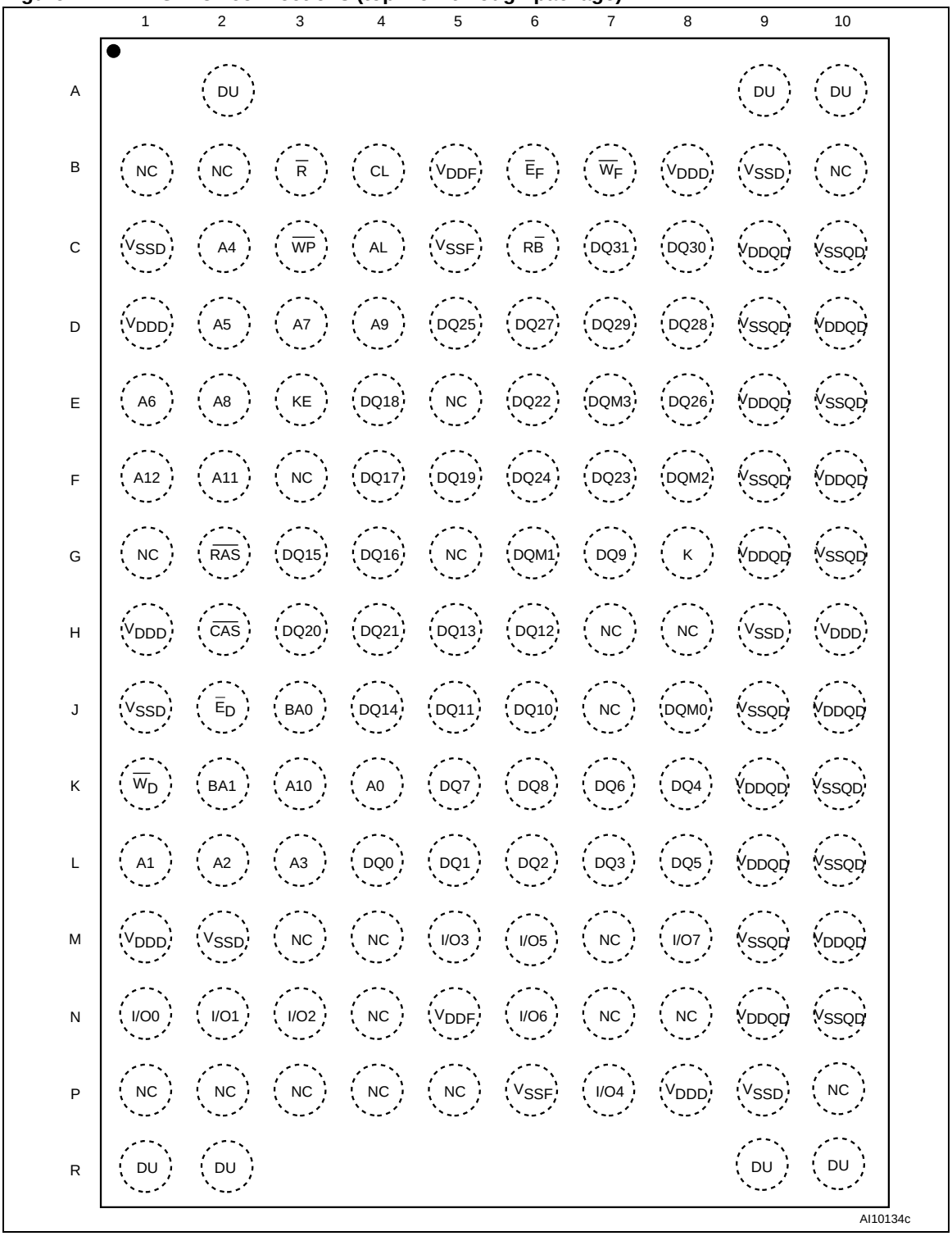
	Signal	Function	Direction
NAND flash memory	I/O0-I/O7	Data Input/Outputs for x8 and x16 devices	Input/output
	AL	Address Latch Enable	Input
	CL	Command Latch Enable	Input
	$\overline{E}_F$	Chip Enable	Input
	$\overline{R}$	Read Enable	Input
	R$\overline{B}$	Ready/Busy (open-drain output)	Output
	$\overline{W}_F$	Write Enable	Input
	$\overline{WP}$	Write Protect	Input
	V_{DDF}	Supply voltage	Power supply
LPSDRAM	A0-A12	Row address: A0-A12 Column address: A0-A8 Auto-precharge flag: A10	Ground
	BA0-BA1	Bank Select inputs	Input
	DQ0-DQ15	Data inputs/outputs	Input/output
	K	Clock	Input
	KE	Clock Enable	Input
	$\overline{E}_D$	Chip Select	Input
	$\overline{W}_D$	Write Enable	Input
	$\overline{RAS}$	Row Address Strobe	Input
	$\overline{CAS}$	Column Address Strobe	Input
	DQM0	DQ Mask Enable (controls DQ0-DQ7)	Input
	DQM1	DQ Mask Enable (controls DQ8-DQ15)	Input
	V_{DDD}	Supply voltage	Power supply
	V_{DDQD}	Input/output supply voltage	Power supply
	V_{SS}	Common NAND Flash and LPSDRAM ground	Ground
	NC	Not connected internally	N/A
	DU	Do not use	N/A

Figure 3. TFBGA107 connections (top view through package)



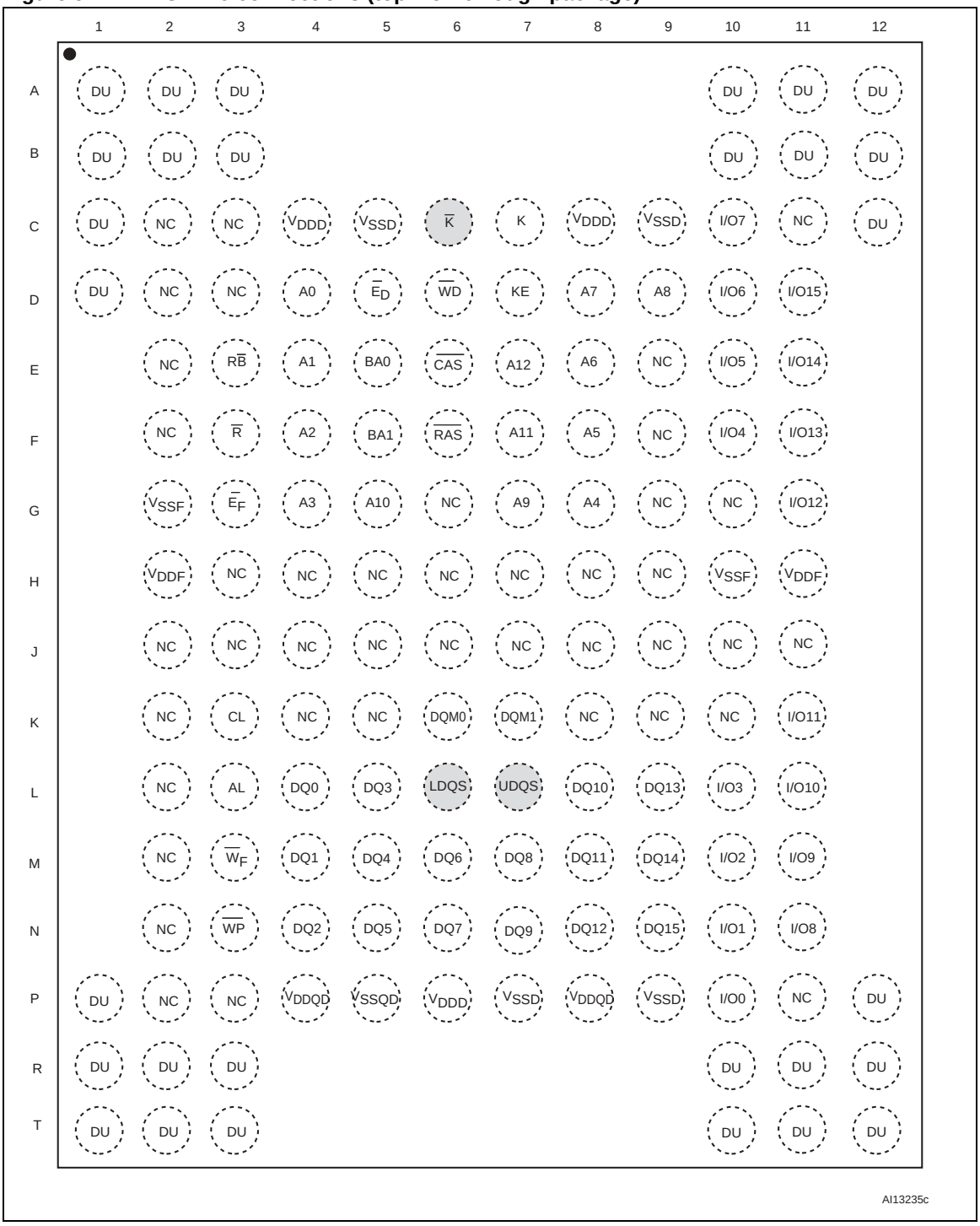
1. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.
2. Balls shaded in gray are only used for NAND + DDR devices.

Figure 4. TFBGA137 connections (top view through package)



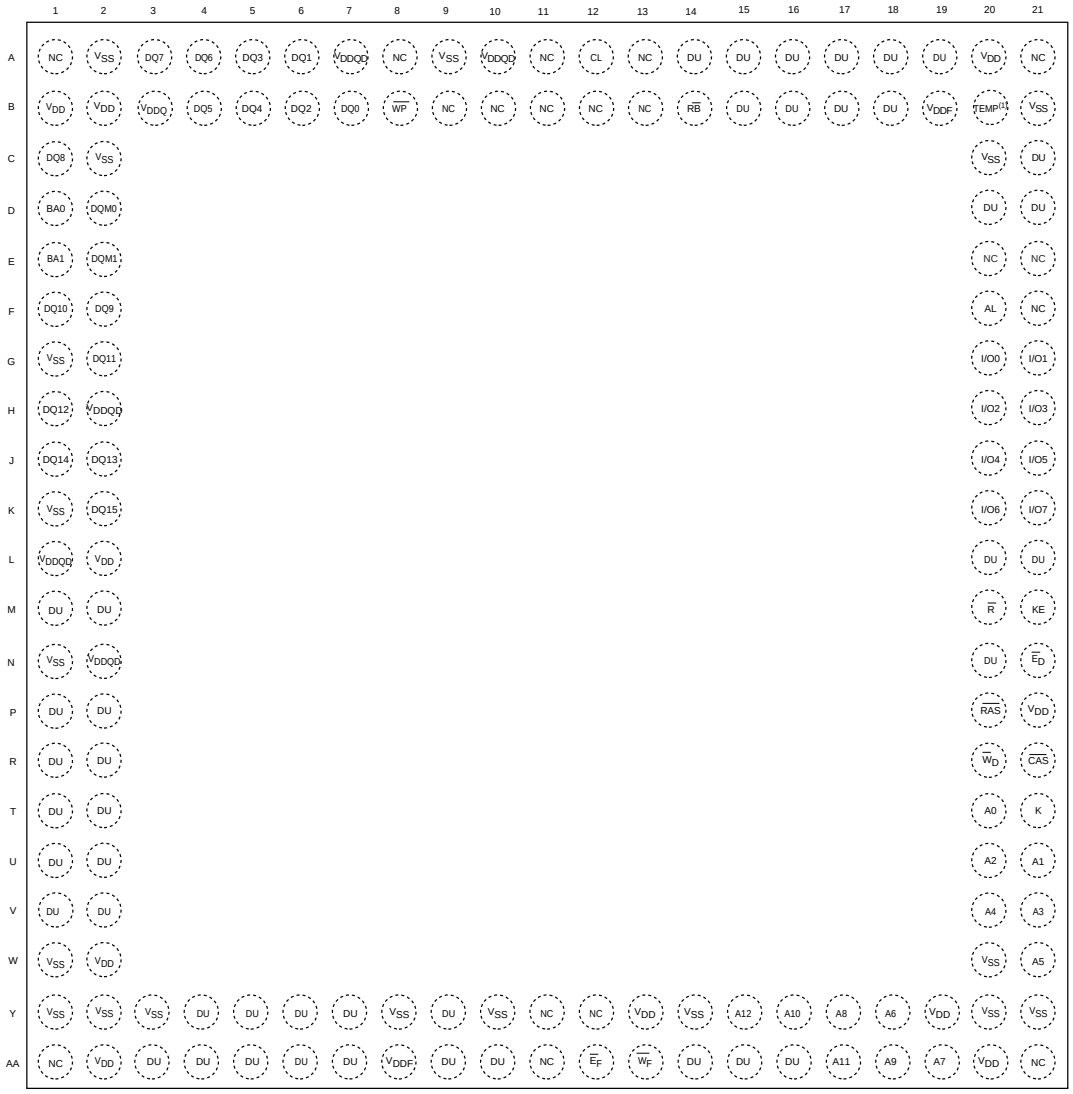
1. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.

Figure 5. TFBGA149 connections (top view through package)



1. Balls shaded in gray are only used for NAND + DDR devices.
2. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.

Figure 6. TFBGA152 connections (top view through package)



1. Ball B20 is the SDRAM temperature flag.
2. All voltage balls must be connected to the power supply (the internal connection is not guaranteed). All ground balls must be connected to the ground.

2 Signals description

Figure 1 and *Figure 2*, in conjunction with *Table 4* and *Table 5*, provide a brief overview of the signals connected to NANDxxxxMx devices. This section provides further information on the signals.

For additional details on the signals, refer to the NAND flash memory and the LPSDRAM datasheets.

2.1 Flash memory inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 are used by the flash memory to input the selected address, output the data during a read operation, or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

2.2 Flash memory inputs/outputs (I/O8-I/O15)

Input/outputs 8 to 15 are only available in x16 NAND flash devices. They are used to output the data during a read operation or input data during a write operation. Command and address inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

2.3 Flash memory Address Latch Enable (AL)

The Address Latch Enable, AL, activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable.

2.4 Flash memory Command Latch Enable (CL)

The Command Latch Enable, CL, activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable.

2.5 Flash memory Chip Enable ($\overline{E}_F$)

The Chip Enable input, $\overline{E}_F$, activates the memory control logic, input buffers, decoders, and read circuitry. When Chip Enable is Low, V_{IL}, the device is selected.

If Chip Enable goes High (V_{IH}) while the device is busy, the device remains selected and does not go into standby mode.

2.6 Flash memory Read Enable ($\overline{R}$)

The Read Enable, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

2.7 Flash memory Write Enable ($\overline{W}_F$)

The Write Enable input, $\overline{W}_F$, controls writing to the command interface, input address, and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down, a minimum recovery time of 10 µs is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

2.8 Flash memory Write Protect ($\overline{WP}$)

The Write Protect pin is an input that provides hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

2.9 Flash memory Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the P/E/R controller is currently active.

When Ready/Busy is Low, V_{OL}, this signifies that a read, program, or erase operation is in progress. When the operation completes, Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low then indicates that one or more of the memories is busy.

2.10 Flash memory V_{DDF} supply voltage

V_{DDF} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program, and erase).

An internal voltage detector disables all functions whenever V_{DDF} is below the V_{LKO} threshold to protect the device from any involuntary program/erase operations during power transitions.

Each device in a system should have V_{DDF} decoupled with a 0.1 µF capacitor, and the PCB track widths should be sufficient to carry the required program and erase currents

2.11 Flash memory V_{SSF} ground

Ground, V_{SSF}, is the reference for the power supply. It must be connected to the system ground.

2.12 LPSDRAM address inputs (A0-A12)

The A0-A12 address inputs are used to select the row or column to be made active. If a row is selected, all thirteen address inputs, A0-A12, are used. If a column is selected, only the least significant address inputs, A0-A8 (256-Mbit device and 512-Mbit x32 device) or A0-A9 (512-Mbit x16 device), are used. In this latter case, A10 determines whether auto precharge is used. If A10 is High (set to '1') during read or write, the operation includes an auto precharge cycle. If A10 is Low (set to '0') during read or write, the cycle does not include an auto precharge cycle.

2.13 LPSDRAM bank select address inputs (BA0-BA1)

The select address inputs of the BA0 and BA1 banks are used to select the bank to be made active.

The following are the necessary settings when selecting the addresses:

- The device must be enabled
- Row Address Strobe, $\overline{RAS}$, must be Low, V_{IL}
- Column Address Strobe, $\overline{CAS}$, must be High, V_{IH}
- $\overline{W}$ must be High, V_{IH}

The address inputs are latched on the rising edge of the clock signal, K.

2.14 LPSDRAM data inputs/outputs (DQ0-DQ15 and DQ16-DQ31)

The DQ16-DQ31 data inputs/outputs are available only in the NAND99W3M1 and NANDA9W3M1, where the bus width is ×32.The data inputs/outputs output the data stored at the selected address during a read operation, or are used to input the data during a write operation.

2.15 LPSDRAM Chip Select ($\overline{E}_D$)

The Chip Select input, $\overline{E}_D$, activates the memory state machine, address buffers, and decoders when driven Low, V_{IL}. When High, V_{IH}, the device is not selected.

2.16 LPSDRAM Column Address Strobe ($\overline{CAS}$)

The Column Address Strobe, $\overline{CAS}$, is used in conjunction with address inputs A8-A0 (256-Mbit device and 512-Mbit x32 device) or A9-A0 (512-Mbit x16 device) and BA1-BA0, to select the starting column location prior to a read or write operation.

2.17 LPSDRAM Row Address Strobe ($\overline{RAS}$)

The Row Address Strobe, $\overline{RAS}$, is used in conjunction with address inputs A12-A0 and BA1-BA0 to select the starting address location prior to a read or write operation.

2.18 LPSDRAM Write Enable ($\overline{W}_D$)

The Write Enable input, $\overline{W}_D$, controls writing.

2.19 LPSDRAM Clock Input (K)

The Clock signal, K, is used to clock the read and write cycles. During normal operation, the Clock Enable pin, KE, is High, V_{IH}. The Clock signal K can be suspended to switch the device to the self-refresh, power-down or deep power-down mode by driving KE Low, V_{IL}.

2.20 LPSDRAM Clock Input ($\overline{K}$)

The Clock signal, $\overline{K}$, is only available on the DDR LPSDRAM and is used in conjunction with the Clock signal, K.

All LPSDRAM input signals except DQM0/DQM1/DQM2/DQM3, UDQS/LDQS and DQ0-DQ31 are referred to the crosspoint of K rising edge and $\overline{K}$ falling edge.

2.21 LPSDRAM Clock Enable (KE)

The Clock Enable, KE, pin is used to control the synchronization of the signals with Clock signal K. If KE is High, V_{IH}, the next Clock rising edge is valid. When KE is Low, V_{IL}, the signals are no longer clocked and data read and write cycles are extended. KE is also involved in switching the device to the self-refresh, power-down and deep power-down modes.

2.22 Lower/Upper Data Read/Write Strobe input/output (LDQS, UDQS)

LDQS and UDQS can be either input or output signals, and act as Write Data Strobe and Read Data Strobe respectively. LDQS and UDQS are the strobe signals for DQ0 to DQ7 and DQ8 to DQ15, respectively.

2.23 LPSDRAM data input/output mask pins (DQM0, DQM1, DQM2, DQM3)

DQM2 and DQM3 are available only in the NAND99W3M1 and NANDA9W3M1, where the bus width is ×32. The data input/output mask pins are input signals used to mask the read or write data. The DQM latency is two clock cycles for read operations and there is no latency for write operations.

2.24 LPSDRAM V_{DDD} supply voltage

V_{DDD} provides the power supply to the internal core of the memory device. It is the main power supply for all read and write operations.

2.25 LPSDRAM V_{DDQD} supply voltage

V_{DDQD} provides the power supply to the I/O pins and enables all outputs to be powered independently of V_{DDD}. V_{DDQD} can be tied to V_{DDD} or can use a separate supply.

It is recommended to power up and power down V_{DDD} and V_{DDQD} together to avoid conditions that would result in data corruption.

2.26 LPSDRAM V_{SSD} ground

V_{SSD} is the reference for the NAND flash power supply. It must be connected to the system ground.

2.27 V_{SSQD} ground

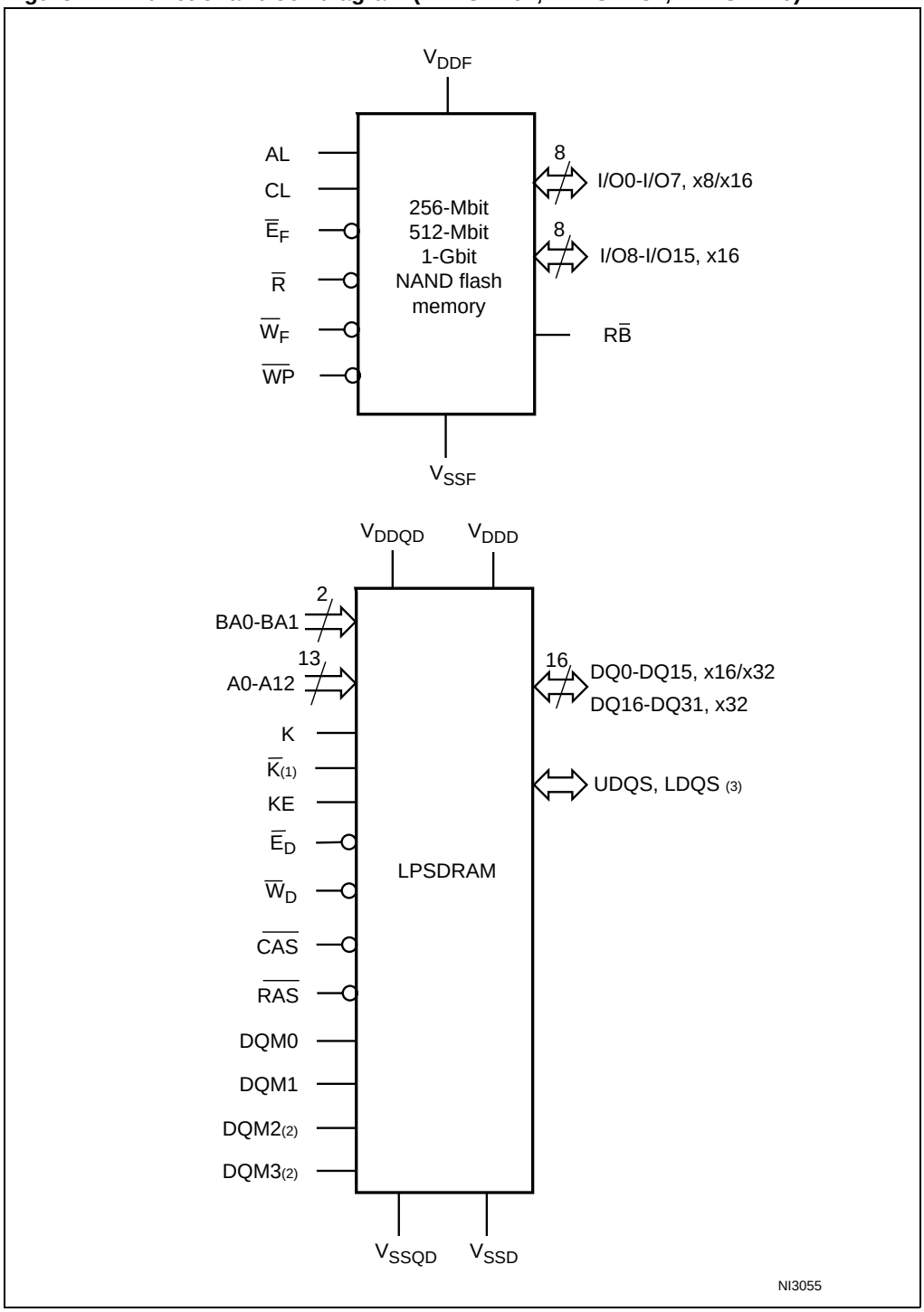
V_{SSQD} ground is the reference for the input/output circuitry driven by V_{DDQD}. V_{SSQD} must be connected to V_{SSD}.

Note: Each device in a system should have V_{DDD} and V_{DDQD} decoupled with a 0.1 µF ceramic capacitor close to the pin (high-frequency, inherently-low inductance capacitors should be as close as possible to the package).

3 Functional description

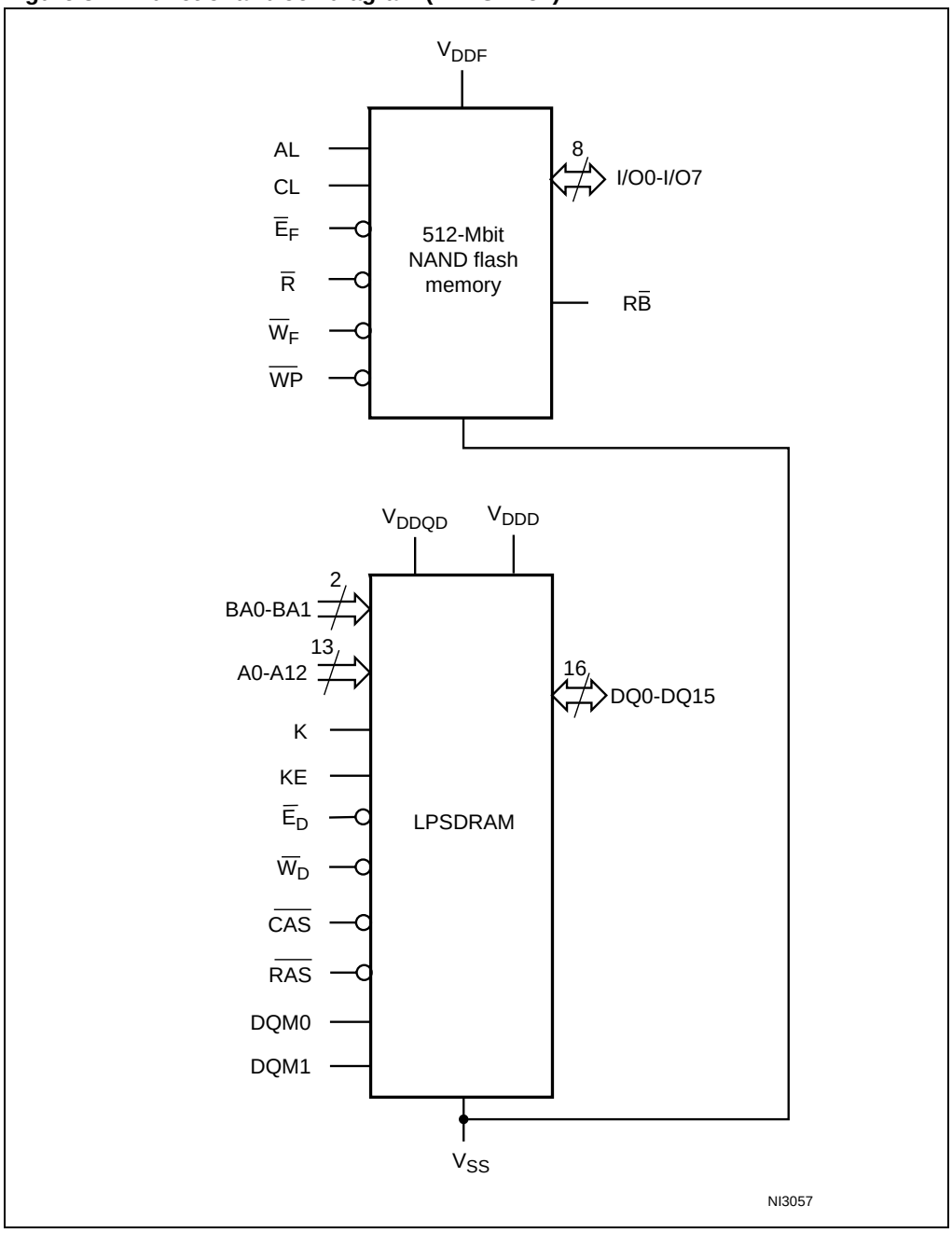
The NAND flash memory and LPSDRAM components have separate power supplies and, according to in which package they are delivered, they either share the same grounds or have separate grounds. They also have separate control signals, addresses, and data input/outputs, which allows simultaneous access to both devices at any moment. *Figure 7* and *Figure 8* show the functional block diagrams.

Figure 7. Functional block diagram (TFBGA107, TFBGA137, TFBGA149)



1. Only available in MCP with DDR.
2. Only available in MCP with SDR/DDR x32.
3. Only available in MCP with DDR x16.

Figure 8. Functional block diagram (TFBGA152)



4 Maximum ratings

Stressing the device above the rating listed in *Table 6: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the reliability of the device.

Table 6. Absolute maximum ratings

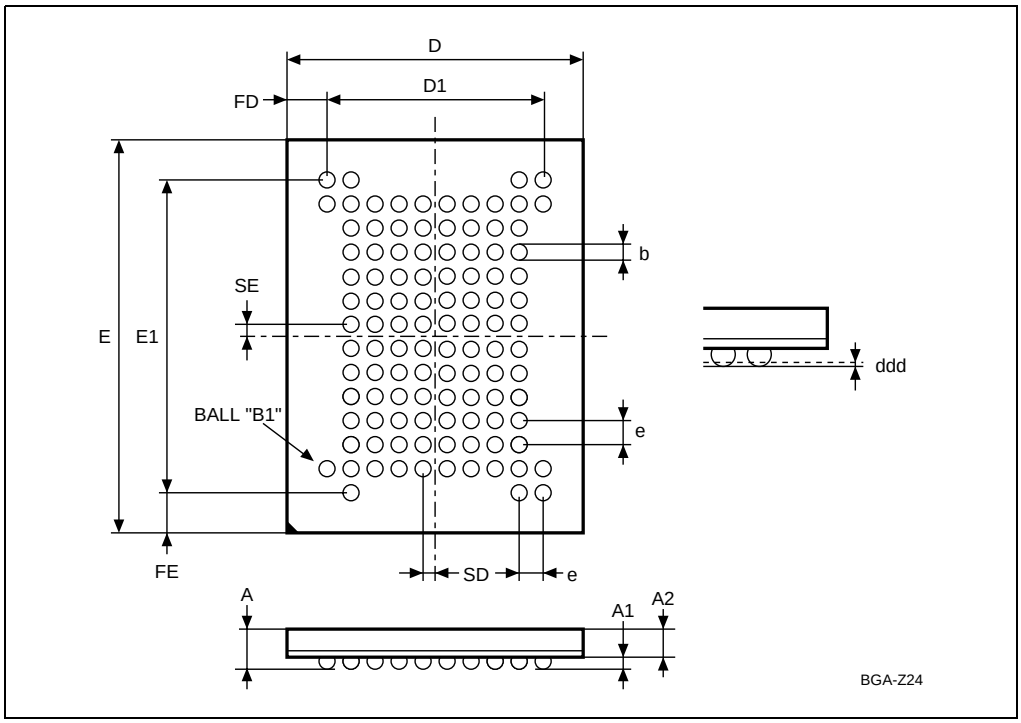
Symbol	Parameter		Value		Unit
			Min	Max	
T_A	Ambient operating temperature		-30	85	°C
T_{STG}	Storage temperature		-55	125	°C
V_{IO}(1)	NAND flash input or output voltage	1.8 V	-0.6	2.7	V
		2.6 V	-0.6	4.6	V
V_{DDQD}	LPSDRAM input or output voltage		-0.3	2.3	V
V_{DDF}	NAND flash supply voltage	1.8 V	-0.6	2.7	V
		2.6 V	-0.6	4.6	V
V_{DDD}	LPSDRAM supply voltage		-0.3	2.3	V
LPSDRAM short circuit output current	I_{OS}		50		mA

1. Minimum voltage may undershoot to -2 V for less than 20 ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2 V for less than 20 ns during transitions on I/O pins.

5 Package mechanical

To meet environmental requirements, Numonyx offers the devices in ECOPACK® packages, which are lead-free. In compliance with JEDEC Standard JESD97, the category of second-level interconnect is marked on the package and on the inner box label. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 9. TFBGA107 10.5 × 13 mm - 10 × 14 active ball array, 0.80 mm pitch, bottom outline

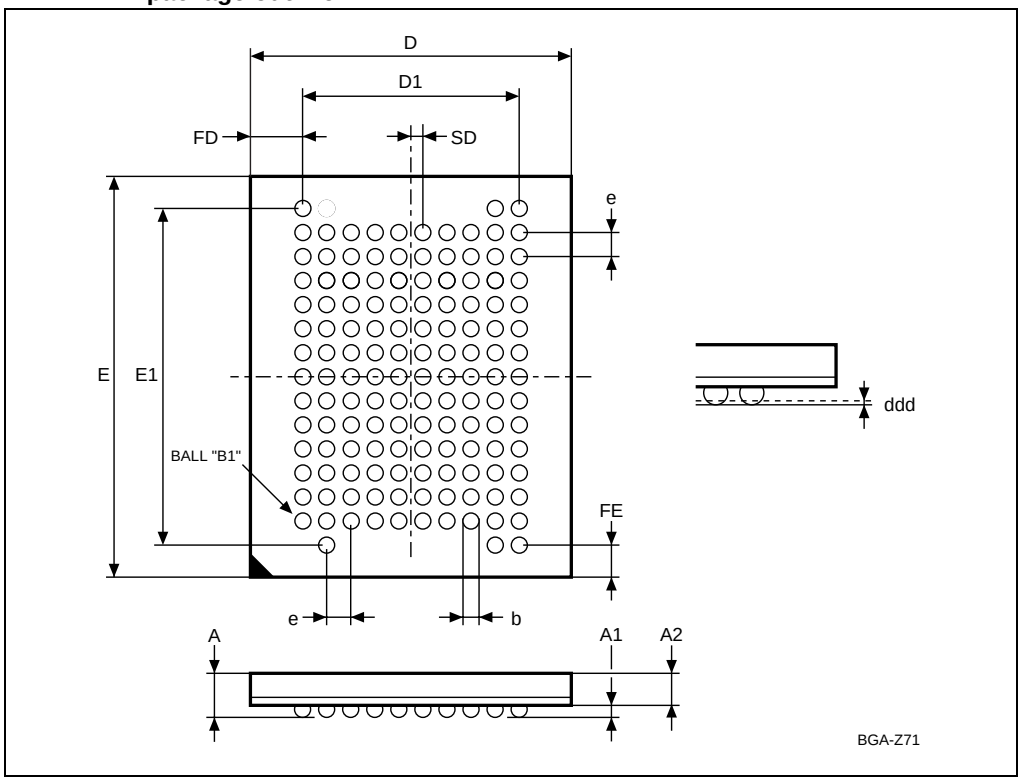


1. Drawing is not to scale.

Table 7. TFBGA107 10.5 × 13 mm - 10 × 14 active ball array, 0.80 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.20	–	–	0.047
A1	–	0.25	–	–	0.012	–
A2	0.80	–	–	0.032	–	–
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.50	10.40	10.60	0.413	0.411	0.415
D1	7.20	–	–	0.283	–	–
ddd	–	–	0.10	–	–	–
E	13.00	12.90	13.10	0.512	0.510	0.514
E1	10.40	–	–	0.409	–	–
e	0.80	–	–	0.031	–	–
FD	1.65	–	–	0.065	–	–
FE	1.30	–	–	0.051	–	–
SD	0.40	–	–	0.016	–	–
SE	0.40	–	–	0.016	–	–

Figure 10. TFBGA137 10.5 x 13 mm - 10 x 13 active ball array, 0.8 mm pitch, package outline



1. Drawing is not to scale.

Table 8. TFBGA137 10.5 x 13 mm - 10 x 15 active ball array, 0.80 mm pitch, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.20	–	–	0.047
A1	–	0.25	–	–	0.011	–
A2	0.80	–	–	0.031	–	–
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.50	10.40	10.60	0.413	0.409	0.417
D1	7.20	–	–	0.283	–	–
E	13.00	12.90	13.10	0.512	0.508	0.516
E1	11.20	–	–	0.441	–	–
e	0.80	–	–	0.031	–	–
FD	1.65	–	–	0.065	–	–
FE	0.90	–	–	0.035	–	–
SD	0.40	–	–	0.016	–	–

Figure 11. TFBGA149 10 × 13.5 mm - 12 × 16 active ball array, 0.80 mm pitch, bottom outline

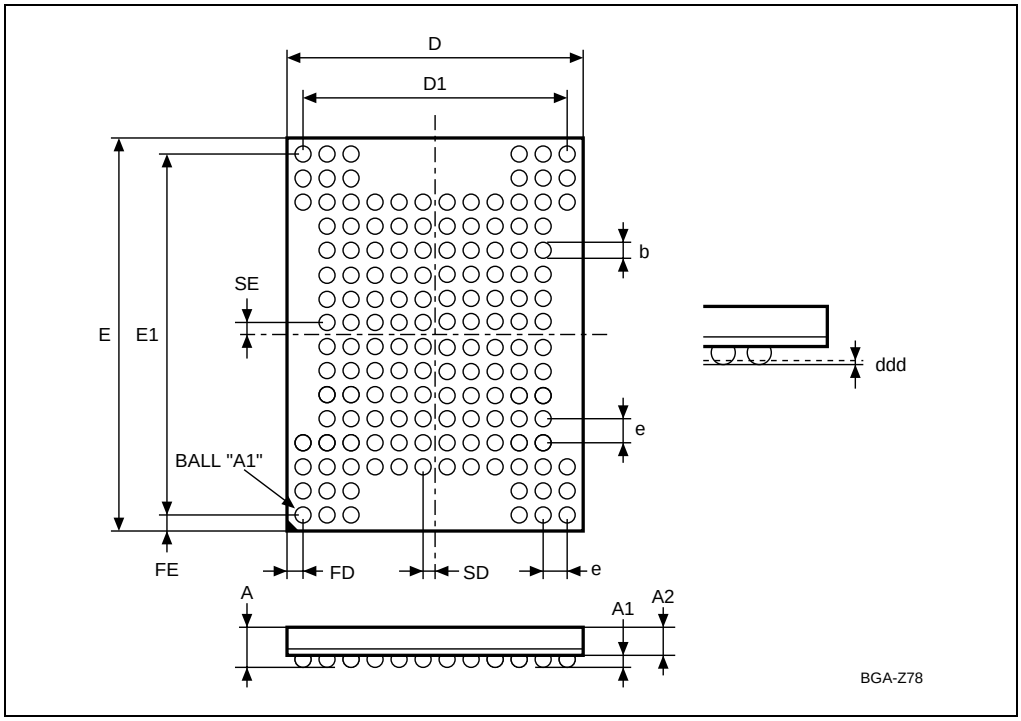
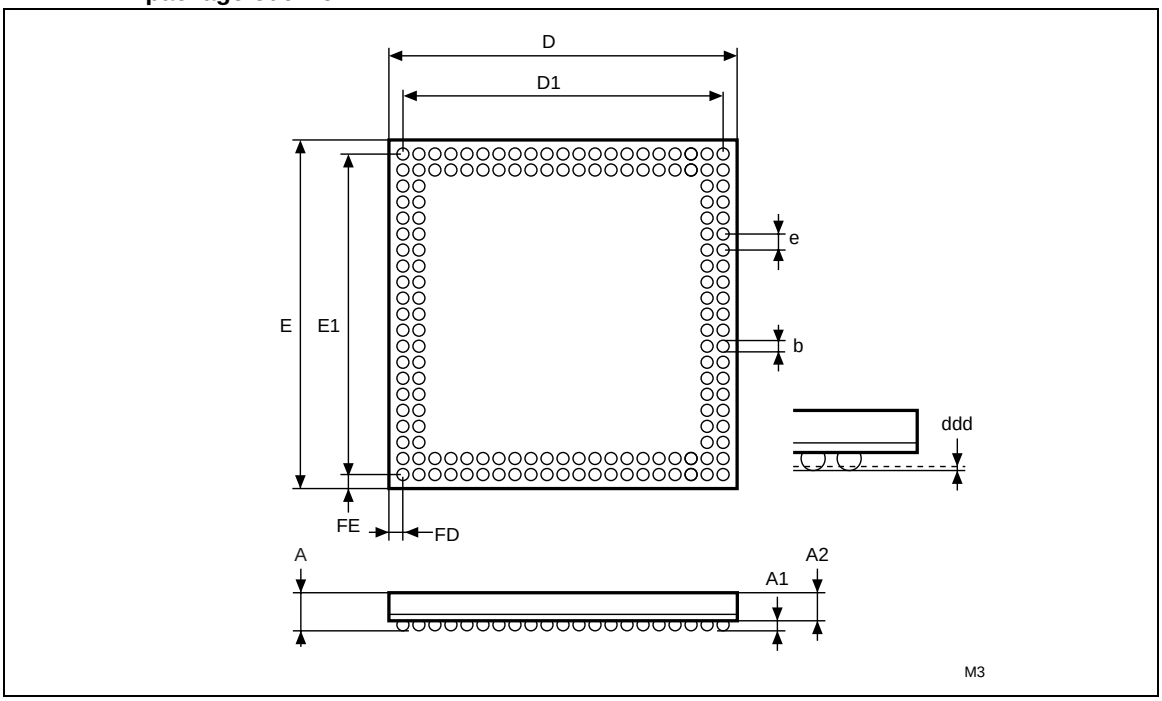


Table 9. TFBGA149 10 × 13.5 mm - 12 × 16 active ball array, 0.80 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.20	–	–	0.047
A1	–	0.25	–	–	0.012	–
A2	0.80	–	–	0.031	–	–
b	0.45	0.40	0.50	0.018	0.016	0.020
D	10.00	9.90	10.10	0.394	0.390	0.398
D1	8.80	–	–	0.346	–	–
ddd	–	–	0.10	–	–	–
E	13.50	13.40	13.60	0.531	0.528	0.535
E1	12.00	–	–	0.472	–	–
e	0.80	–	–	0.031	–	–
FD	0.60	–	–	0.024	–	–
FE	0.75	–	–	0.029	–	–
SD	0.40	–	–	0.016	–	–
SE	0.40	–	–	0.016	–	–

Figure 12. TFBGA152 - 2-row perimeter matrix 2R21 x 21 14 × 14 mm, 0.65 mm pitch, package outline



1. Drawing is not to scale.

Table 10. TFBGA152 - 2-row perimeter matrix 2R21 x 21 14 x 14 mm, 0.65 mm pitch, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.10	–	–	0.043
A1	–	0.32	–	–	0.013	–
A2	0.63	–	–	0.025	–	–
b	0.42	0.37	0.47	0.016	0.015	0.018
ddd	–	–	0.10	–	–	0.004
D	14.00	13.90	14.10	0.551	0.547	0.555
D1	13.00	–	–	0.512	–	–
E	14.00	13.90	14.10	0.551	0.547	0.555
E1	13.00	–	–	0.512	–	–
e	0.65	–	–	0.026	–	–
F	0.50	–	–	0.020	–	–

6 Ordering information

Table 11. Ordering information scheme

Example: NAND8 8 R 3 M 0 A ZBB 5 E

Device type
NAND flash memory

NAND flash density
8 = 256 Mbits
9 = 512 Mbits
A = 1 Gbit

DRAM density
8 = 256 Mbits
9 = 512 Mbits

NAND flash operating voltage
R = 1.7 V to 1.95 V
W = 2.5 V to 3.6 V

NAND bus width
3 = x8
4 = x16

Family identifier
M = 528-byte page NAND flash memory

DRAM options
0 = SDR, x16, 133 MHz
1 = SDR, ×32, 133 MHz
2 = DDR, x16, 133 MHz

Product version
A
B
C

Package
ZBA = TFBGA149, 10 × 13.5 mm
ZBB = TFBGA107 10.5 × 13 mm
ZBC = TFBGA137 10.5 x 13 mm
ZPA = TFBGA152, 14 × 14 mm x 1.1 mm

Temperature
5 = –30 °C to 85 °C

Option
E = ECOPACK® package, standard packing
F = ECOPACK® package, tape and reel packing

Note: Devices are shipped from the factory with the flash memory content bits, in valid blocks, erased to '1'. For further information on any aspect of this device, please contact your nearest Numonyx sales office.

7 Revision history

Table 12. Document revision history

Date	Version	Changes
29-Jun-2006	1	Initial release.
20-Jul-2006	2	NAND99R3M0 root part number added. TFBGA137 package added. LPSDRAM input or output voltage and V_{DDD}, V_{DDQD} updated in *Table 6: Absolute maximum ratings*.
12-Sep-2006	3	Added NAND99R3M0 to title; updated *Table 2: Product list* to show that NAND98R3M0 is also delivered in package TFBGA149.
19-Sep-2006	4	Added 'x32' to title description on page 1
10-Oct-2006	5	Root part numbers corrected in *Section 1.2: LPSDRAM component* updated.
18-Dec-2006	6	NAND99W3M0 and NAND99W3M1 root part numbers added. TFBGA152 Package on Package (PoP) added. V_{IO} and V_{DDF} at 3V added in *Table 6: Absolute maximum ratings*.
19-Feb-2007	7	DQM0, DQM2, DQM3 and DQM4 definition updated in *Table 4: Signal names (TFBGA107, TFBGA137 and TFBGA149 packages)*.
12-Jun-2007	8	Added NANDA9W3M1 root part number and added all respective data in *Table 2*, *Figure 1*, *Figure 2*, *Figure 7*, and *Figure 8*. *Table 3: LPSDRAM details* is a new table that outlines the information on the LPSDAM components.
7-Aug-2007	9	Added NAND99R4M2 root part number and added/modified all associated data in *Table 1*, *Table 2*, *Table 3*, *Figure 1*, *Table 4*, *Figure 5*, *Figure 7*, *Figure 8*; added the following new sections: *Section 2.2*, *Section 2.22*; modified values in *Table 6*, *Table 7*, *Table 8*, and *Table 9*. Updated the part ordering information in *Table 11*.
22-Jan-2008	10	Added NAND99R3M2, NAND98W3M1, and NAND98R3M1 part numbers and added/modified all associated data in *Table 1*, *Table 2*, *Table 3*, *Figure 1*, and *Figure 5*. Applied Numonyx branding.
24-Jul-2008	11	Added NAND98R3M2 root part number. Minor text changes.

Please Read Carefully: