256K (32K x 8) Static RAM

Features

- **Temperature Ranges**
  - **Commercial: 0°C to 70°C**
  - **Industrial: –40°C to 85°C**
  - **Automotive-A: –40°C to 85°C**
  - **Automotive-E: –40°C to 125°C**
- **Speed: 70 ns**
- **Low voltage range: 2.7V–3.6V**
- **Low active power and standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in standard Pb-free and non Pb-free 28-lead (300-mil) narrow SOIC, 28-lead TSOP-I and 28-lead Reverse TSOP-I packages**

Functional Description[1]

The CY62256VN family is composed of two high-performance CMOS static RAM's organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and tri-state drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.
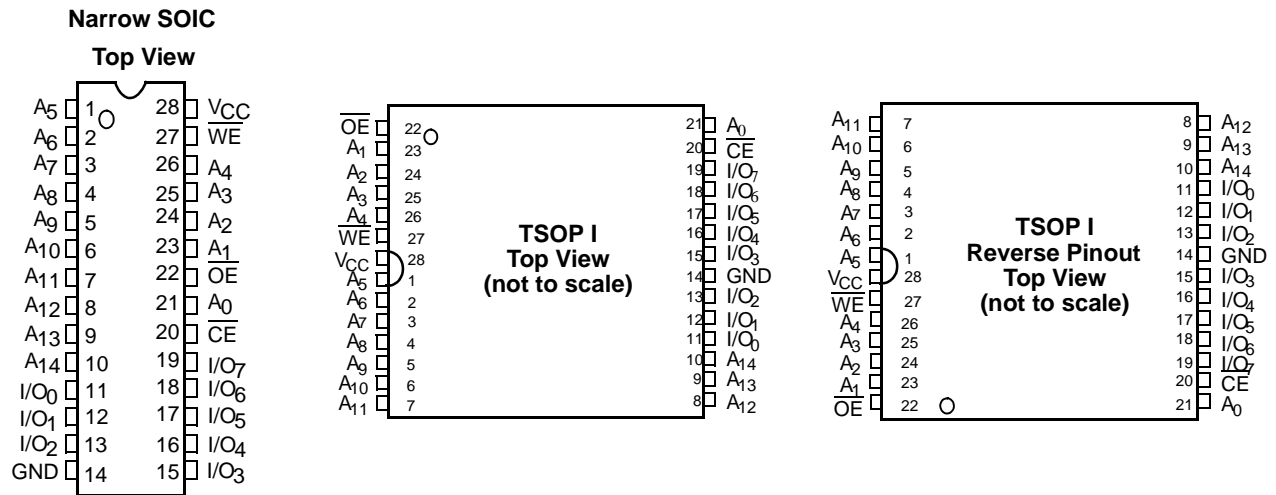
Logic Block Diagram
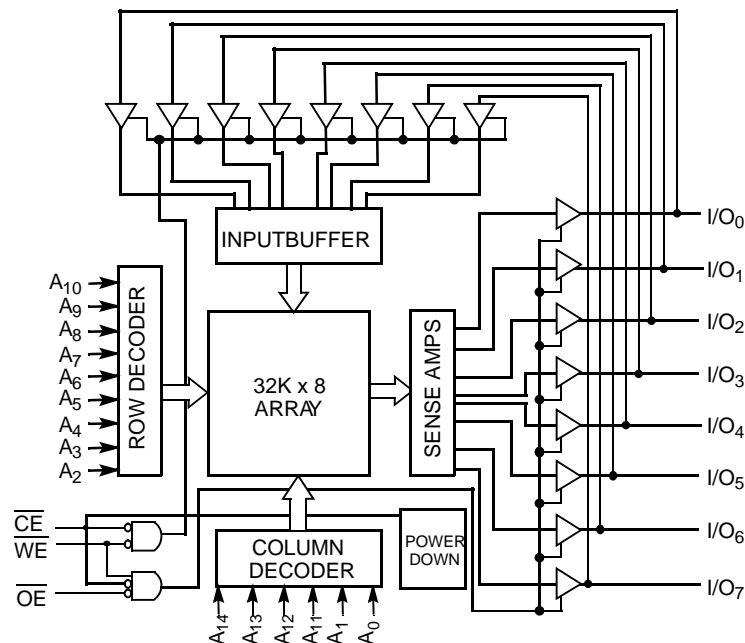
Note:
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

[+] Feedback

Product Portfolio

Product	Range	V_{CC} Range (V)			Power Dissipation			
					Operating, I_{CC} (mA)		Standby, I_{SB2} (μA)	
		Min.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.
CY62256VNLL	Com'l	2.7	3.0	3.6	11	30	0.1	5
CY62256VNLL	Ind'l	2.7	3.0	3.6	11	30	0.1	10
CY62256VNLL	Automotive-A	2.7	3.0	3.6	11	30	0.1	10
CY62256VNLL	Automotive-E	2.7	3.0	3.6	11	30	0.1	130

Pin Configurations

Narrow SOIC Top View

TSOP I Top View (not to scale)

TSOP I Reverse Pinout Top View (not to scale)

Pin Definitions

Pin Number	Type	Description
1–10, 21, 23–26	Input	A_0–A_{14}. Address Inputs
11–13, 15–19	Input/Output	I/O_0–I/O_7. Data lines. Used as input or output lines depending on operation
27	Input/Control	$\overline{WE}$. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
20	Input/Control	$\overline{CE}$. When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	$\overline{OE}$. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
14	Ground	**GND**. Ground for the device
28	Power Supply	V_{CC}. Power supply for the device

Note:
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ., T_A = 25°C, and t_{AA} = 70 ns.

Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature .... –65°C to + 150°C

Ambient Temperature with
Power Applied... –55°C to + 125°C

Supply Voltage to Ground Potential
(Pin 28 to Pin 14) .... −0.5V to + 4.6V

DC Voltage Applied to Outputs
in High-Z State[3] .... –0.5V to V_{CC} + 0.5V

DC Input Voltage[3] .... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage... > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current.. > 200 mA

Operating Range

Device	Range	Ambient Temperature (T_A)[4]	V_{CC}
CY62256VN	Commercial	0°C to +70°C	2.7V to 3.6V
	Industrial	−40°C to +85°C	
	Automotive-A	−40°C to +85°C	
	Automotive-E	−40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-70			Unit
				Min.	Typ.[2]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = −1.0 mA	V_{CC} = 2.7V	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 2.7V			0.4	V
V_{IH}	Input HIGH Voltage			2.2		V_{CC} + 0.3V	V
V_{IL}	Input Leakage Voltage			−0.5		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	Com'l/Ind'l/Auto-A	−1		+1	µA
			Auto-E	−10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{IN} ≤ V_{CC}, Output Disabled	Com'l/Ind'l/Auto-A	−1		+1	µA
			Auto-E	−10		+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = 3.6V, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{RC}	All Ranges		11	30	mA
I_{SB1}	Automatic CE Power down Current - TTL Inputs	V_{CC} = 3.6V, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	All Ranges		100	300	µA
I_{SB2}	Automatic CE Power-down Current- CMOS Inputs	V_{CC} = 3.6V, $\overline{CE}$ ≥ V_{CC} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0	Com'l		0.1	5	µA
			Ind'l/Auto-A			10	
			Auto-E			130	

Notes:
3. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
4. T_A is the "Instant-On" case temperature

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, $f = 1$ MHz, $V_{CC} = 3.0V$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance[5]

Parameter	Description	Test Conditions	SOIC	TSOPI	RTSOPI	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	68.45	87.62	87.62	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		26.94	23.73	23.73	°C/W

AC Test Loads and Waveforms
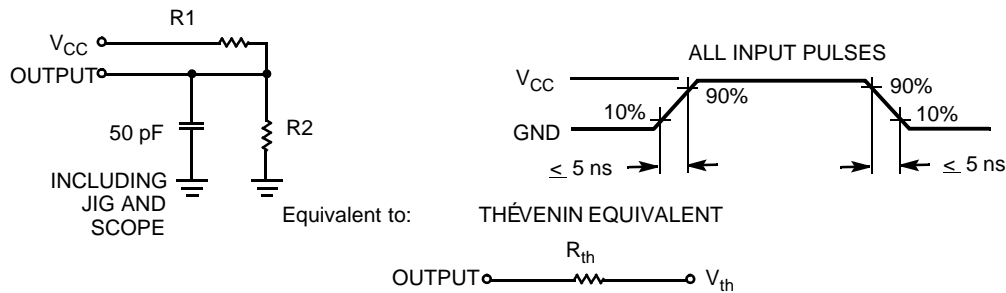
Parameter	Value	Units
R1	1100	Ohms
R2	1500	Ohms
RTH	645	Ohms
VTH	1.750	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions[6]		Min.	Typ.[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.4			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.4V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	Com'l		0.1	3	μA
			Ind'l/Auto-A			6	
			Auto-E			50	
t_{CDR}[6]	Chip Deselect to Data Retention Time			0			ns
t_R[5]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform
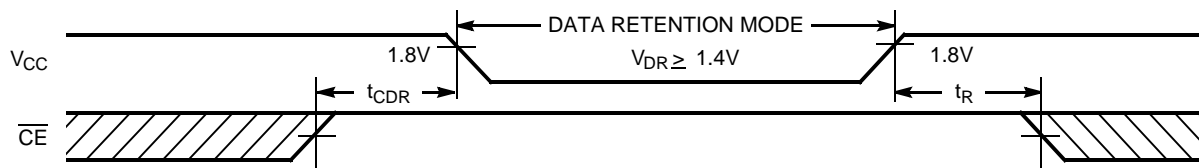
Note:
5. Tested initially and after any design or process changes that may affect these parameters.
6. No input may exceed $V_{CC} + 0.3V$.

[+] Feedback

Switching Characteristics Over the Operating Range[7]

| Parameter	Description	CY62256VN-70 Min.	CY62256VN-70 Max.	Unit
Read Cycle				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[8]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8, 9]		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[8]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[8, 9]		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		70	ns
Write Cycle[10, 11]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		ns
t_{AW}	Address Set-up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{SD}	Data Set-up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[8, 9]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[8]	10		ns

Notes:
7. Test conditions assume signal transition time of 5 ns or less timing reference levels of $V_{CC}/2$, input pulse levels of 0 to V_{CC}, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
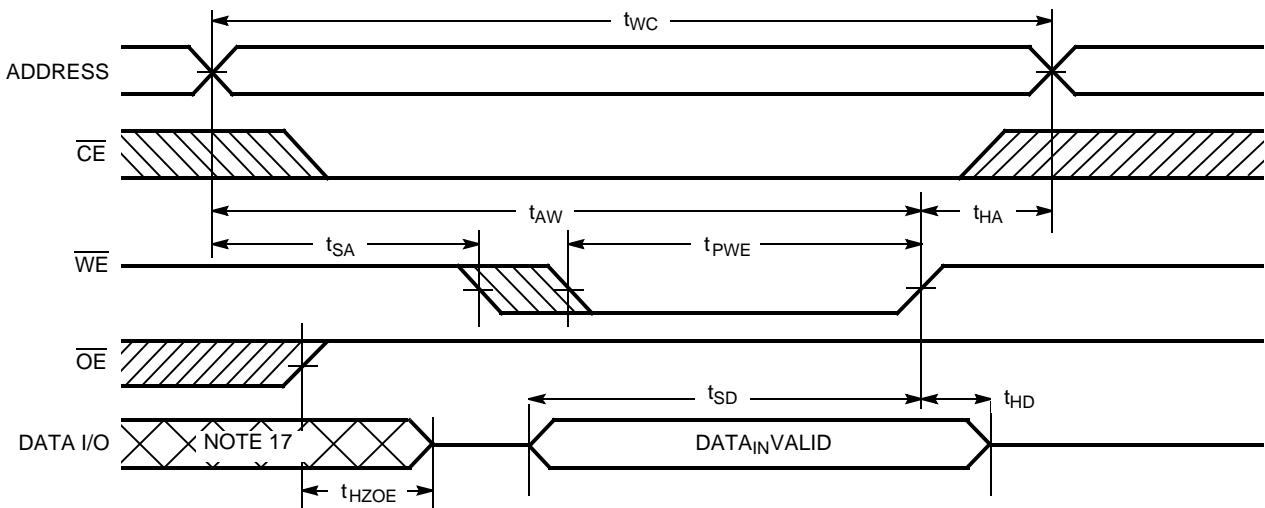
[+] Feedback

Switching Waveforms

Read Cycle No. 1[12, 13]
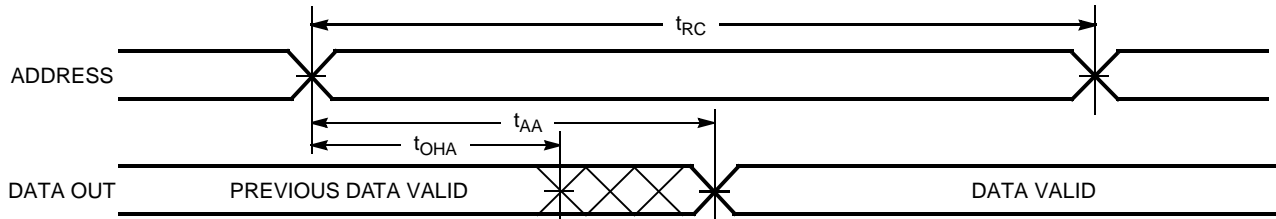
Read Cycle No. 2[13, 14]
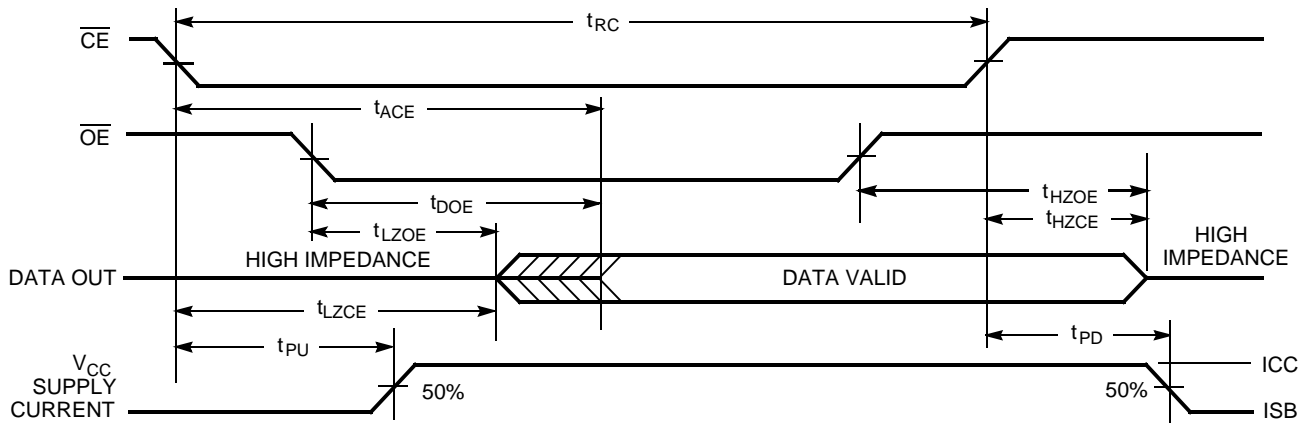
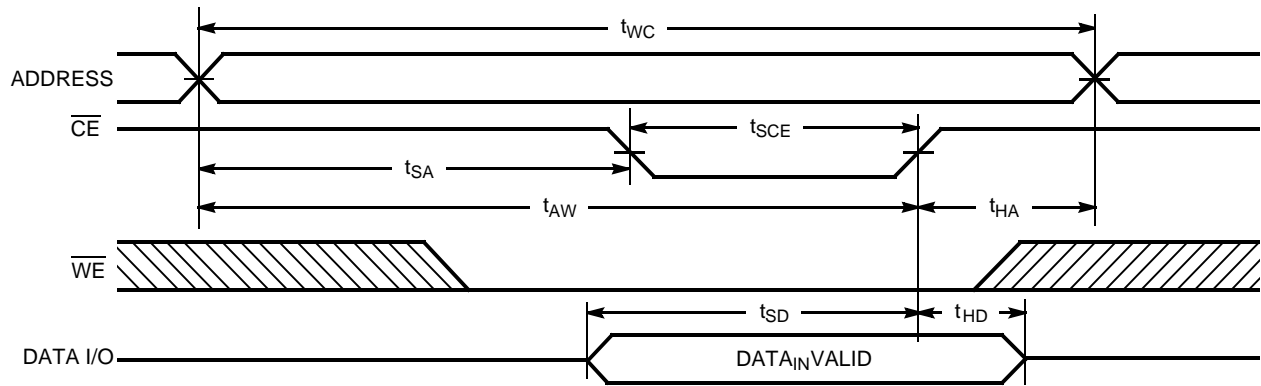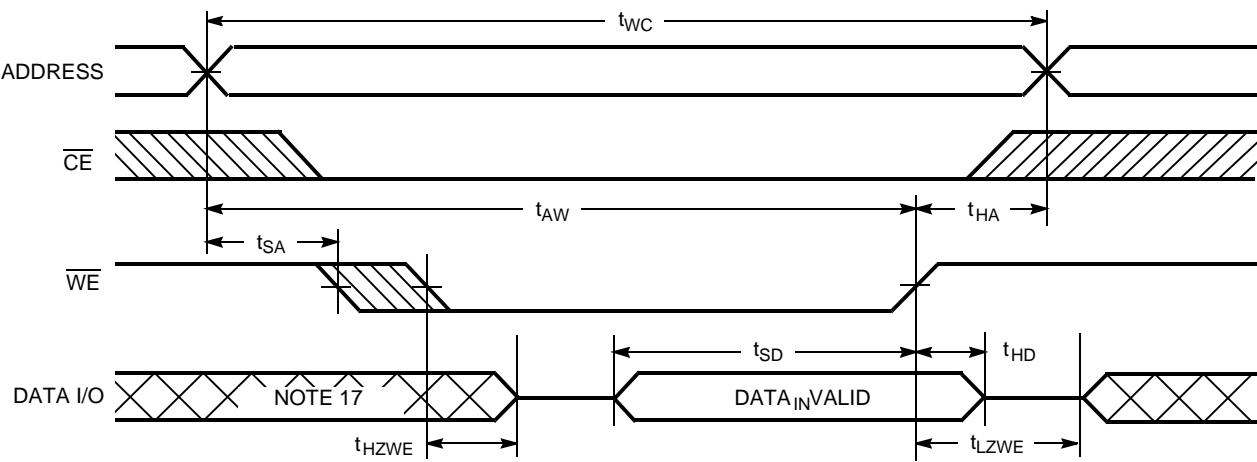**Write Cycle No. 1 ($\overline{WE}$ Controlled)**[10, 15, 16]

Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.
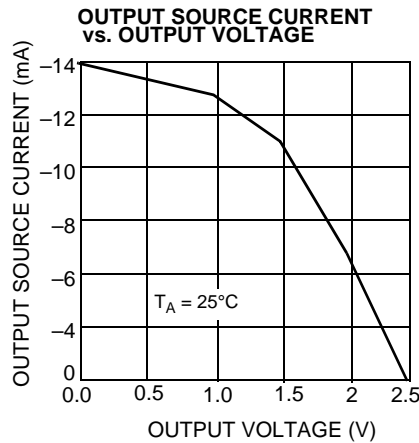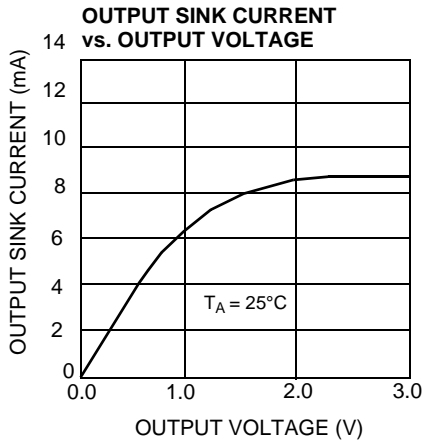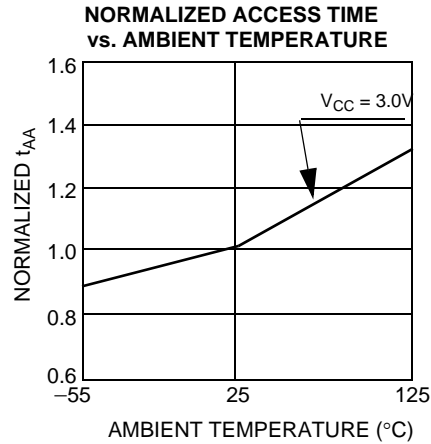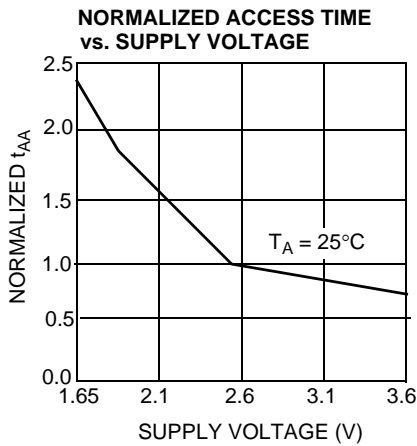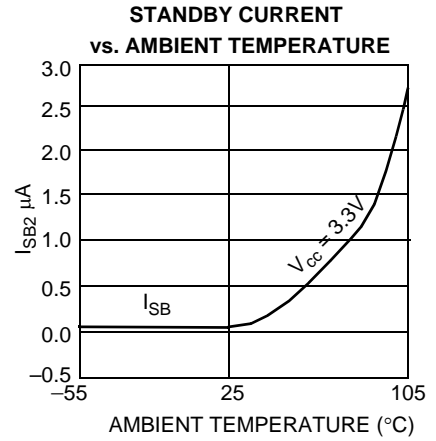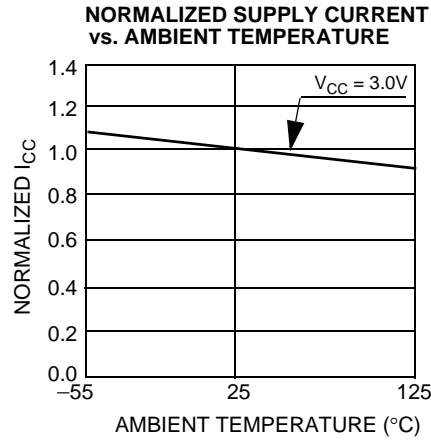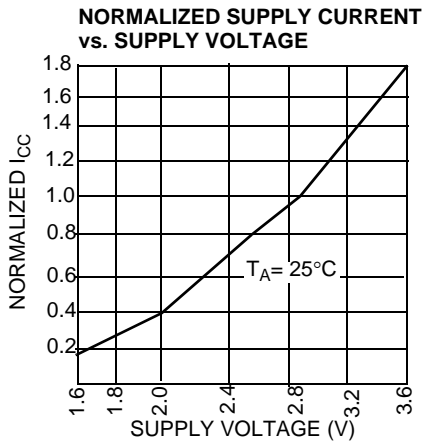
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 15, 16]

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[11, 16]

Document #: 001-06512 Rev. *A

Typical DC and AC Characteristics

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

T_A = 25°C

NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

V_{CC} = 3.0V

STANDBY CURRENT vs. AMBIENT TEMPERATURE

V_{CC} = 3.3V

I_{SB}

NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

T_A = 25°C

NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

V_{CC} = 3.0V

OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

T_A = 25°C

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

T_A = 25°C

Typical DC and AC Characteristics (continued)

TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING

$T_A = 25°C$
$V_{CC} = 3V$

(Y-axis: DELTA t_{AA} (ns), X-axis: CAPACITANCE (pF))

NORMALIZED I_{CC} vs. CYCLE TIME

$V_{CC} = 3.0V$

$T_A = 25°C$
$V_{IN} = 0.5V$

(Y-axis: NORMALIZED I_{CC}, X-axis: CYCLE FREQUENCY (MHz))
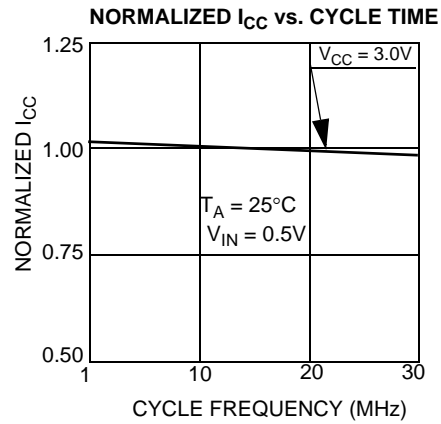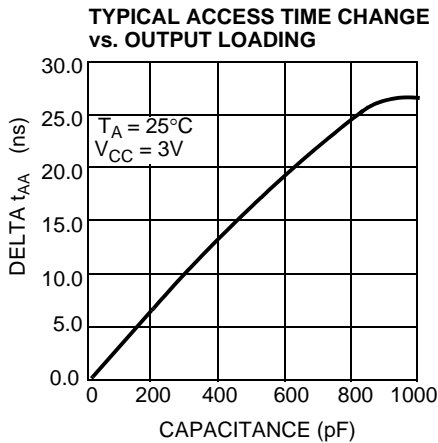
Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62256VNLL-70SNC	51-85092	28-lead (300-mil) Narrow SOIC	Commercial
	CY62256VNLL-70SNXC		28-lead (300-mil) Narrow SOIC (Pb-Free)	
	CY62256VNLL-70ZC	51-85071	28-lead TSOP I	
	CY62256VNLL-70ZXC		28-lead TSOP I (Pb-Free)	
	CY62256VNLL-70SNXI	51-85092	28-lead (300-mil) Narrow SOIC (Pb-Free)	Industrial
	CY62256VNLL-70ZI	51-85071	28-lead TSOP I	
	CY62256VNLL-70ZXI		28-lead TSOP I (Pb-Free)	
	CY62256VNLL-70ZRI	51-85074	28-lead Reverse TSOP I	
	CY62256VNLL-70ZRXI		28-lead Reverse TSOP I (Pb-Free)	
	CY62256VNLL-70ZXA	51-85071	28-lead TSOP I (Pb-Free)	Automotive-A
	CY62256VNLL-70SNXE	51-85092	28-lead (300-mil) Narrow SOIC (Pb-Free)	Automotive-E
	CY62256VNLL-70ZXE	51-85071	28-lead TSOP I (Pb-Free)	
	CY62256VNLL-70ZRXE	51-85074	28-lead Reverse TSOP I (Pb-Free)	

Please contact your local Cypress sales representative for availability of other parts

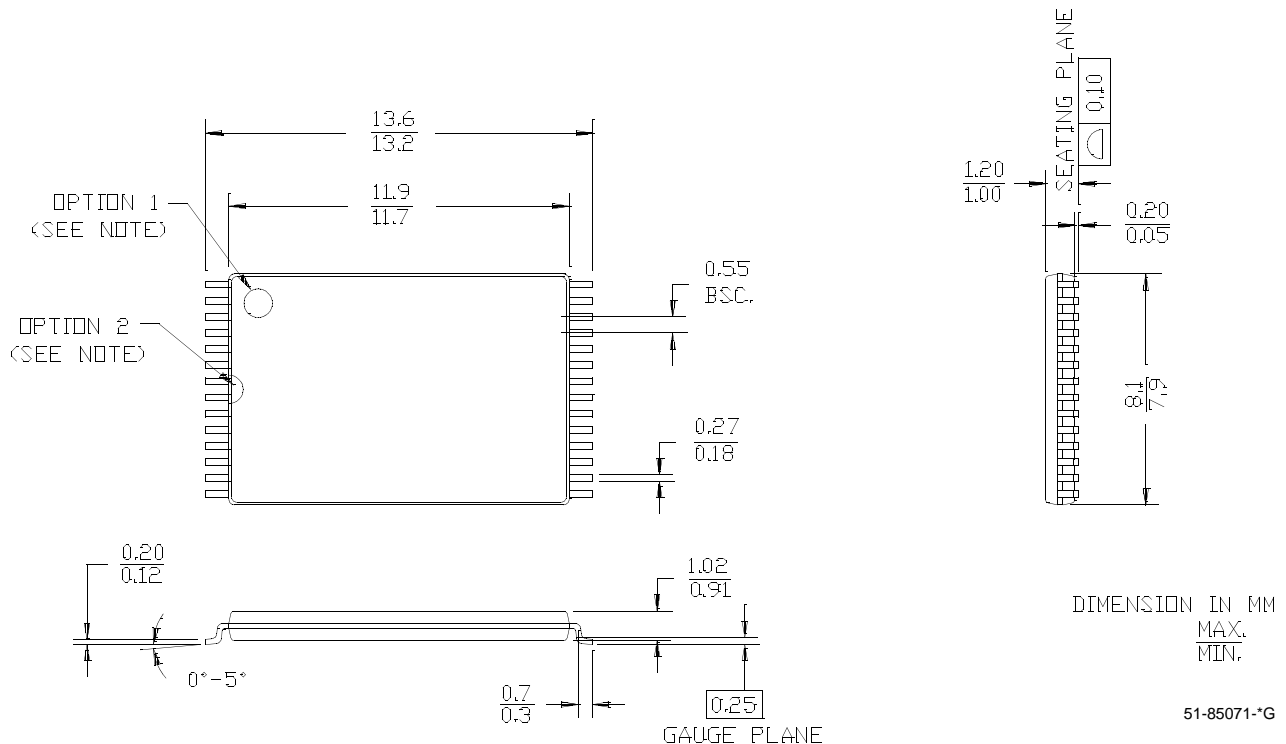[+] Feedback

Package Diagrams

28-lead (300-mil) SNC (Narrow Body) (51-85092)

51-85092-*B

28-lead TSOP 1 (8 × 13.4 mm) (51-85071)

51-85071-*G

[+] Feedback

Package Diagrams (continued)

28-lead Reverse TSOP 1 (8 × 13.4 mm) (51-85074)

NOTE: ORIENTATION I.D MAY BE LOCATED EITHER
       AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM
$\frac{MAX.}{MIN.}$

SEATING PLANE

$\frac{13.6}{13.2}$

$\frac{11.9}{11.7}$

$\frac{0.55}{B.S.C}$

OPTION 2
(SEE NOTE)

$\frac{0.27}{0.18}$

OPTION 1
(SEE NOTE)

$\frac{1.20}{1.00}$

$\frac{0.20}{0.05}$

$\frac{8.1}{7.9}$

$\frac{0.20}{0.12}$

$\frac{1.02}{0.91}$

0°–5°

$\frac{0.7}{0.3}$

51-85074-*F
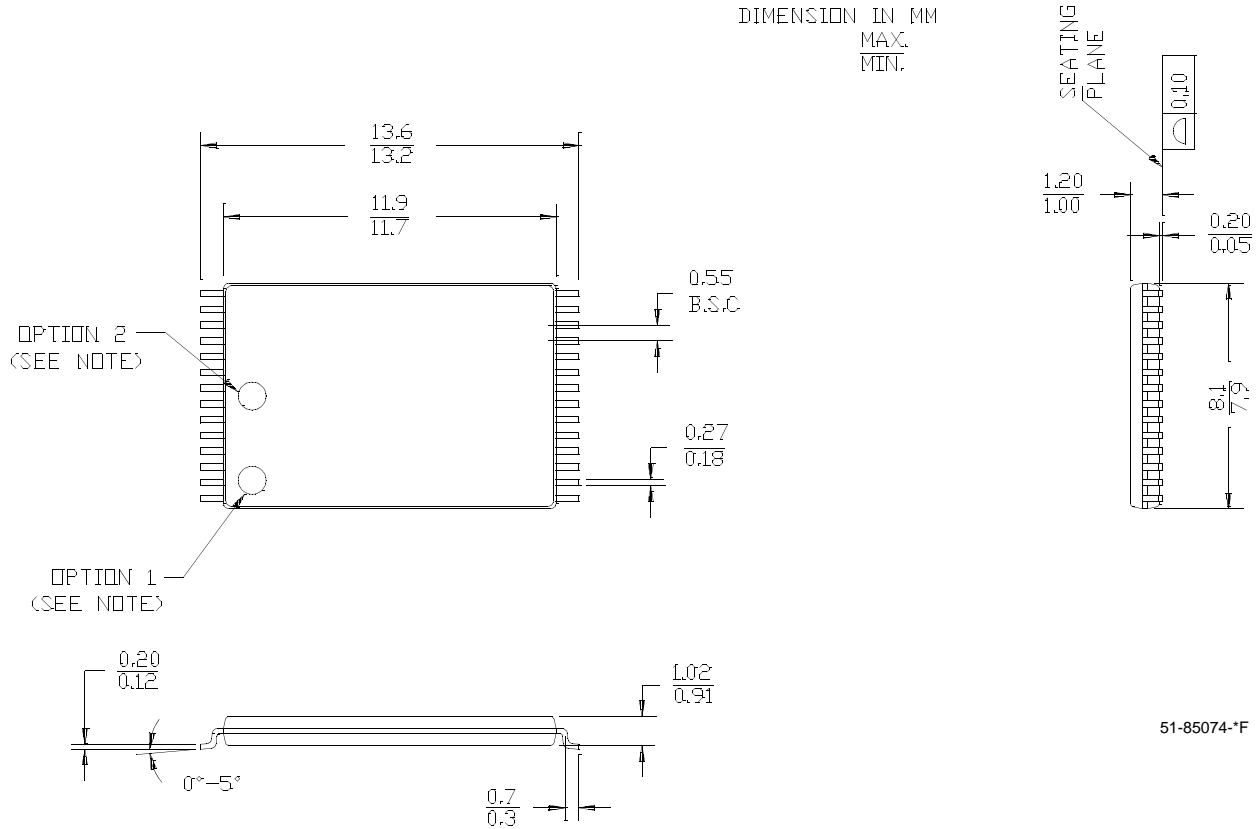
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Document History Page

Document Title: CY62256VN 256K (32K x 8) Static RAM Document Number: 001-06512				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	426504	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated ordering Information table