8-Mbit (512K x 16) Static RAM

Features

- **Very high speed: 45 ns**
- **Wide voltage range: 4.5V–5.5V**
- **Ultra-low standby power**
  - **—Typical Standby current: 2 μA**
  - **—Maximum Standby current: 8 μA (Industrial)**
- **Ultra-low active power**
  - **— Typical active current: 1.8 mA @ f = 1 MHz**
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free 44-pin TSOP II and 48-ball VFBGA package**

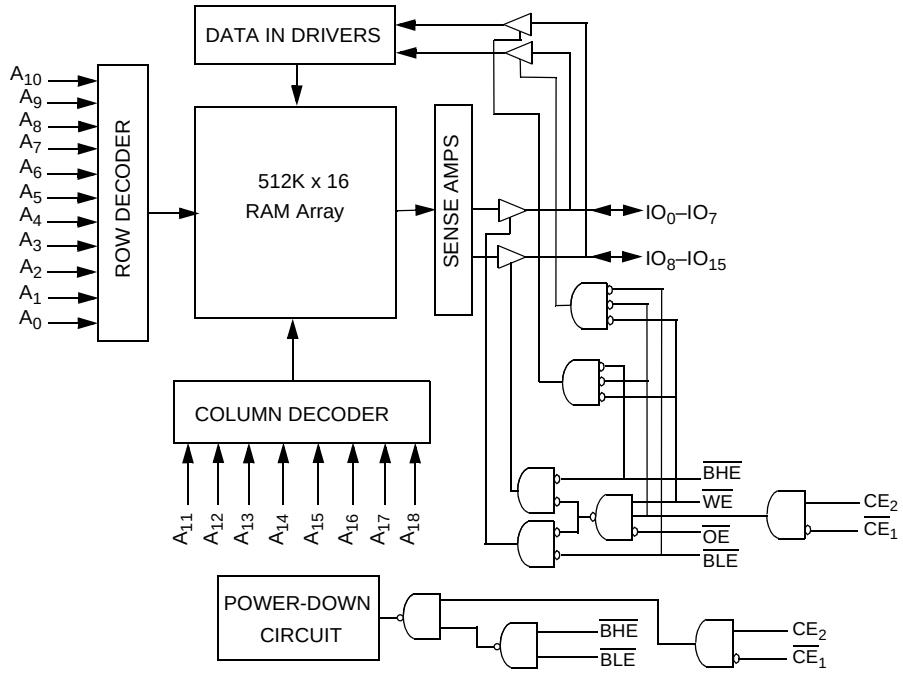
Functional Description[1]

The CY62157E is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (IO_0 through IO_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}_1$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from IO pins (IO_0 through IO_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from IO pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on IO_0 to IO_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on IO_8 to IO_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

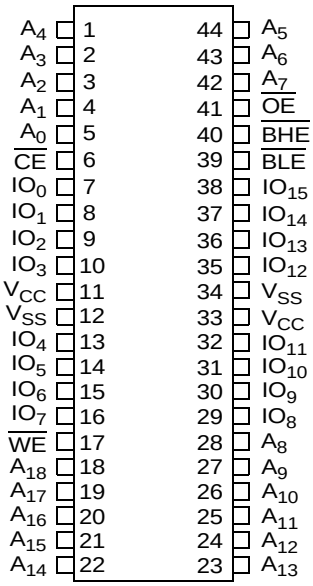
Logic Block Diagram



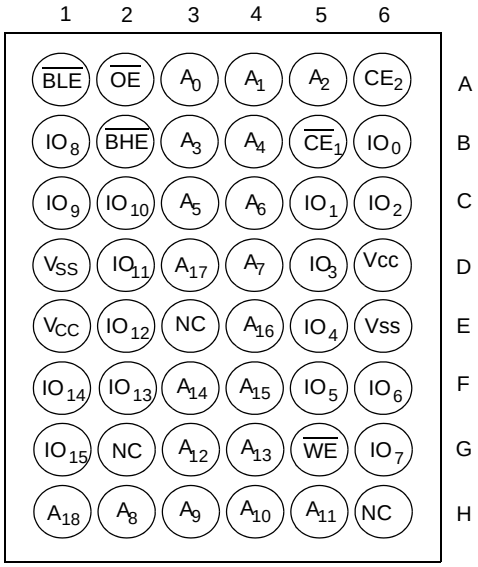
Note:
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

Pin Configuration[2, 3]

TSOP II
Top View



VFBGA
Top View



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
						f = 1MHz		f = f_{max}			
		Min	Typ[4]	Max		Typ[4]	Max	Typ[4]	Max	Typ[4]	Max
CY62157E-45	Ind'l	4.5	5.0	5.5	45	1.8	3	18	25	2	8
CY62157E-55[5]	Auto	4.5	5.0	5.5	55	1.8	4	18	35	2	30

Notes:
2. NC pins are not connected on the die.
3. The 44-pin TSOP II package has only one chip enable ($\overline{CE}$) pin.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.
5. Automotive product information is Preliminary.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied .....–55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.5V to 6.0V

DC Voltage Applied to Outputs in High Z State[6, 7] ..... –0.5V to 6.0V

DC Input Voltage[6, 7] .....–0.5V to 6.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage .....> 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[8]
CY62157E	Industrial	–40°C to +85°C	4.5V to 5.5V
	Automotive	–40°C to +125°C	

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		45 ns (Industrial)			55 ns (Automotive)			Unit
				Min	Typ[4]	Max	Min	Typ[4]	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –1 mA	V_{CC} = 4.5V	2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 4.5V			0.4			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 4.5V to 5.5V		2.2		V_{CC} + 0.5	2.2		V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage	V_{CC} = 4.5V to 5.5V		–0.5		0.8	–0.5		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{max} = 1/t_{RC}	V_{CC} = V_{CCmax}, I_{OUT} = 0 mA CMOS levels		18	25		18	35	mA
		f = 1 MHz			1.8	3		1.8	4	
I_{SB1}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2V, CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V, f = f_{max} (Address and Data Only), f = 0 (OE, BHE, BLE and WE), V_{CC} = 3.60V			2	8		2	30	µA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60V			2	8		2	30	µA

Capacitance[9]

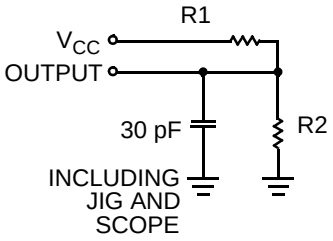
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

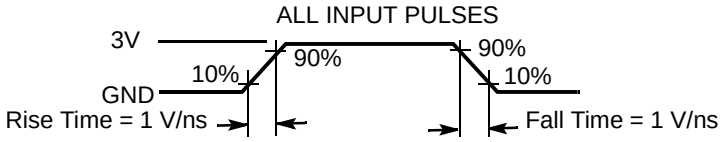
Notes:
6. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns for I < 30 mA.
7. $V_{IH(max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
8. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
9. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance[9]

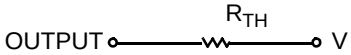
Parameter	Description	Test Conditions	TSOP II	VFBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	77	72	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		13	8.86	°C/W

AC Test Loads and Waveforms





Equivalent to: THEVENIN EQUIVALENT

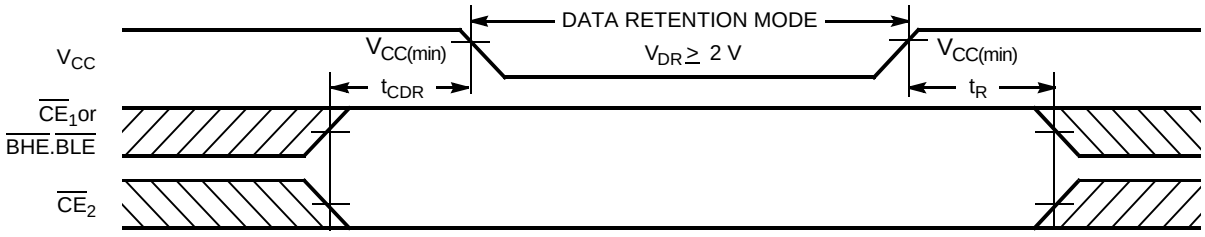


Parameters	Values	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min	Typ[4]	Max	Unit
V_{DR}	V_{CC} for Data Retention			2			V
I_{CCDR}	Data Retention Current	V_{CC}=2V, $\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Industrial			8	µA
			Automotive			30	
t_{CDR}[9]	Chip Deselect to Data Retention Time			0			ns
t_R[10]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform[11]



Notes:
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
11. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

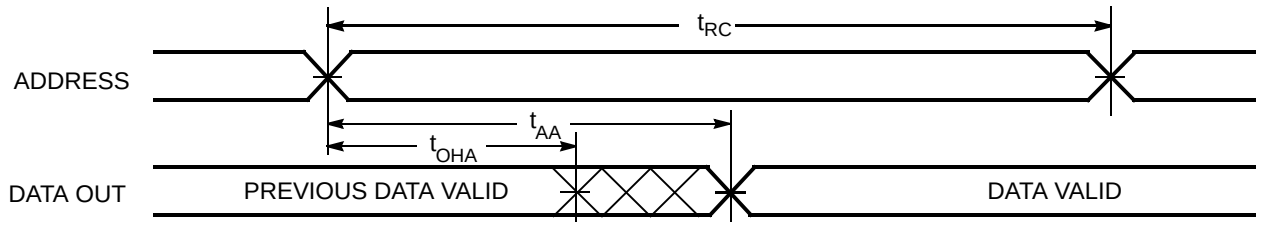
Switching Characteristics Over the Operating Range [12]

Parameter	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read Cycle Time	45		55		ns
t_{AA}	Address to Data Valid		45		55	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22		25	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[13]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[13, 14]		18		20	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[13]	10		10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[13, 14]		18		20	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power-Up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power-Down		45		55	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45		55	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[13]	10		10		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[13, 14]		18		20	ns
Write Cycle[15]						
t_{WC}	Write Cycle Time	45		55		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	35		40		ns
t_{AW}	Address Set-Up to Write End	35		40		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		40		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	35		40		ns
t_{SD}	Data Set-Up to Write End	25		25		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[13, 14]		18		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[13]	10		10		ns

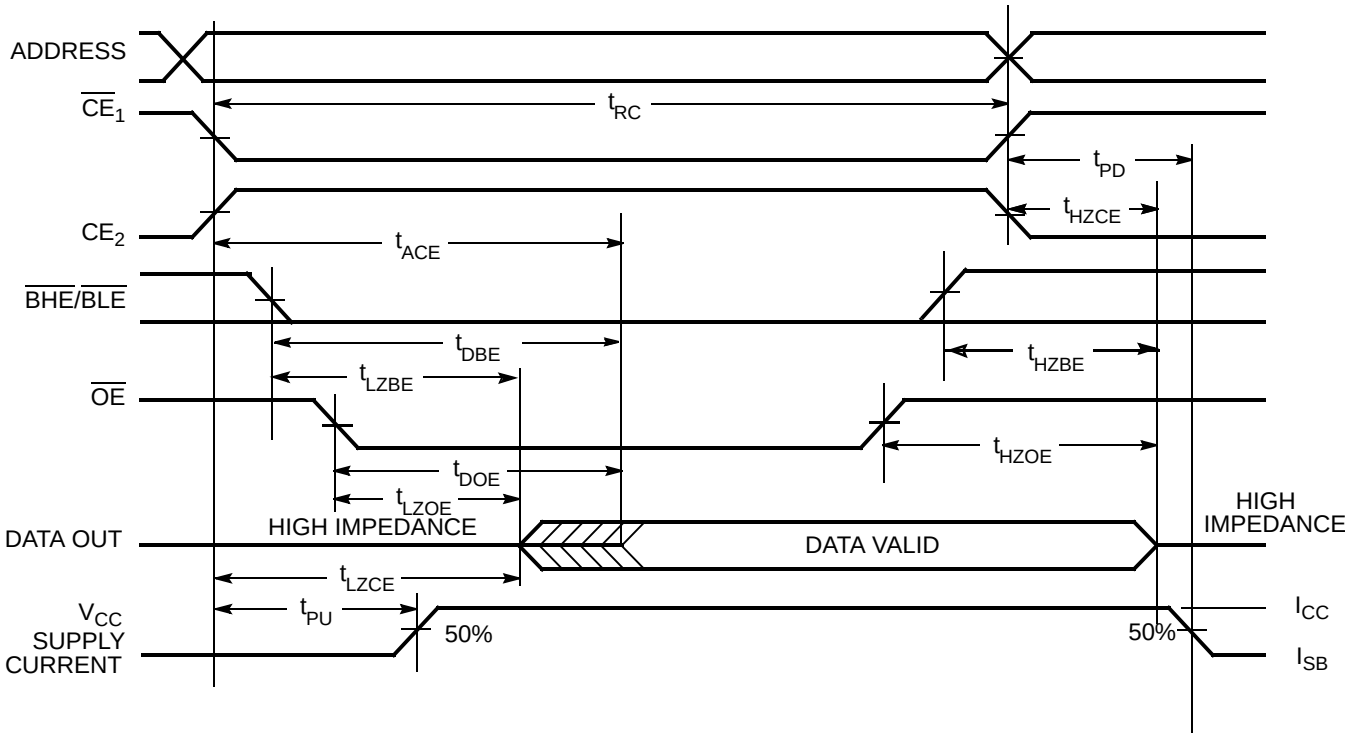
Notes:
12. Test conditions for all parameters other than Tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the “AC Test Loads and Waveforms” section.
13. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
14. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
15. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[16, 17]



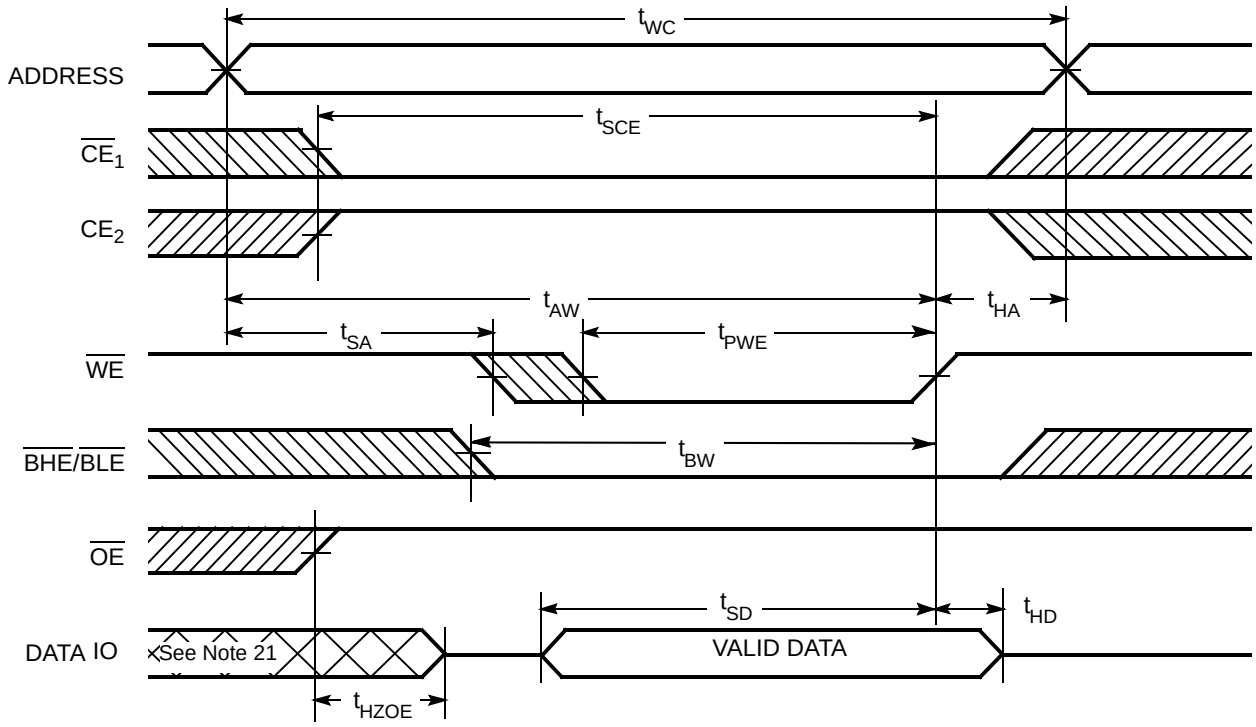
Read Cycle 2 ($\overline{OE}$ Controlled)[17, 18]



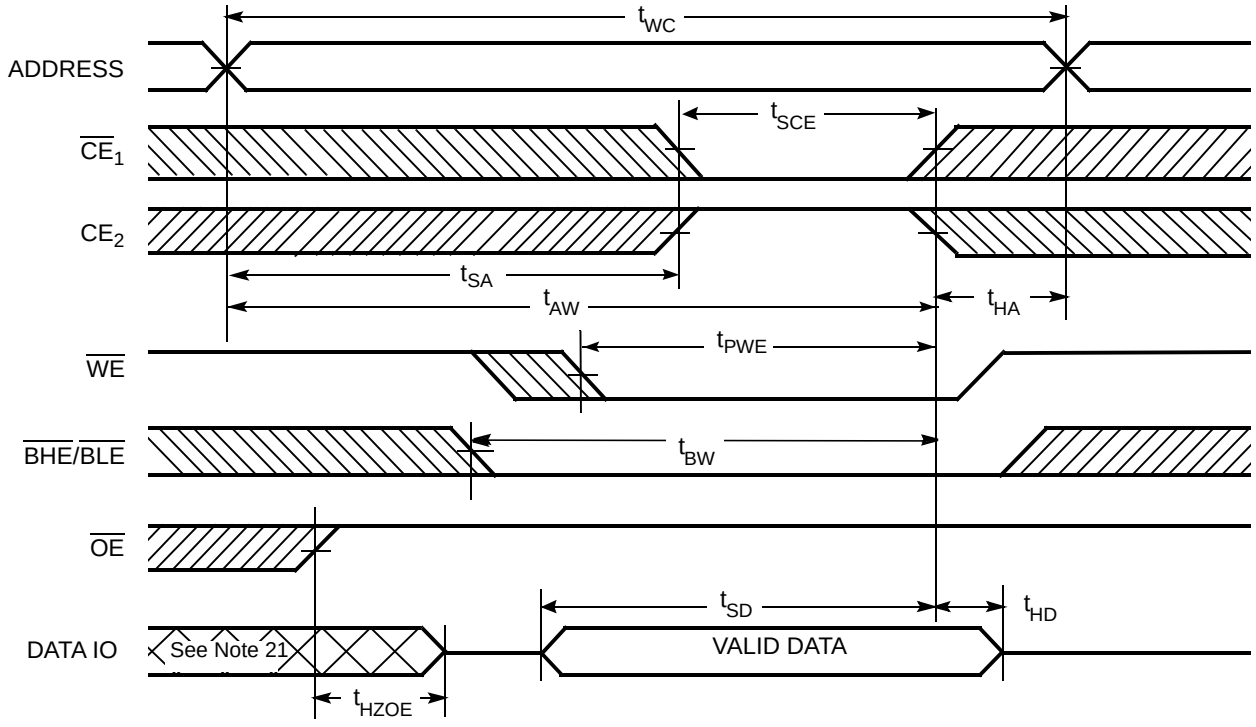
Notes:
16. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
17. $\overline{WE}$ is HIGH for read cycle.
18. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle 1 (WE Controlled)[15, 19, 20, 21]



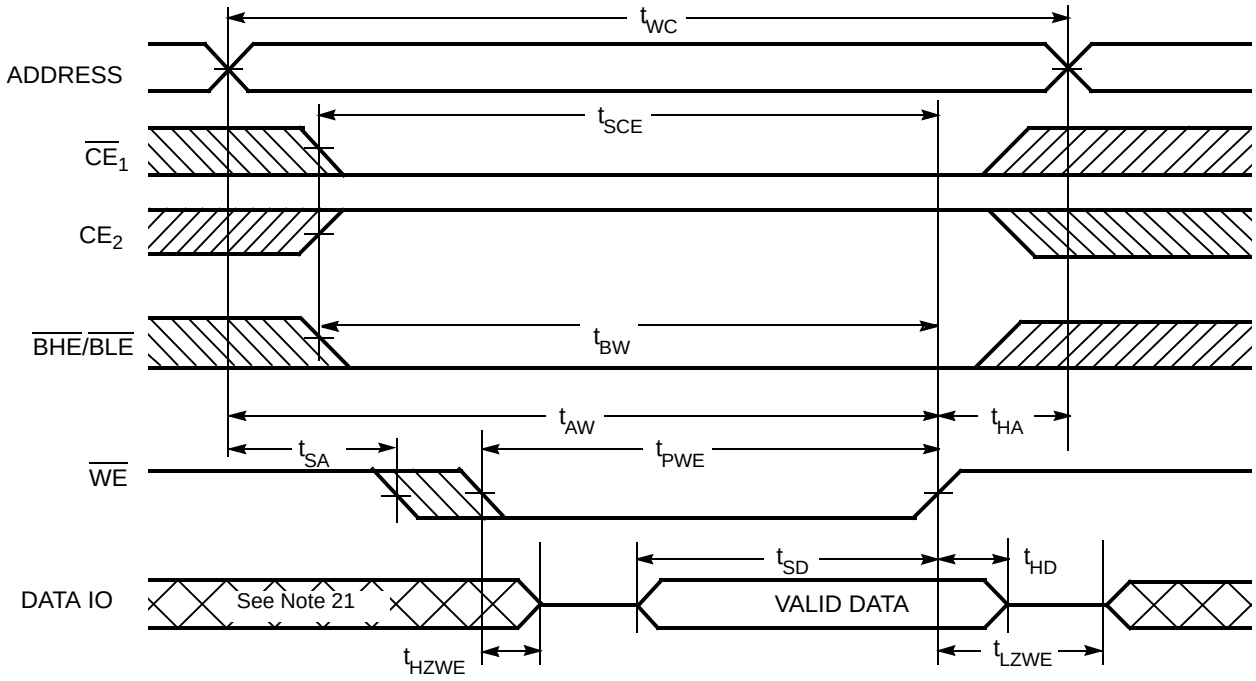
Write Cycle 2 (CE1 or CE2 Controlled)[15, 19, 20, 21]



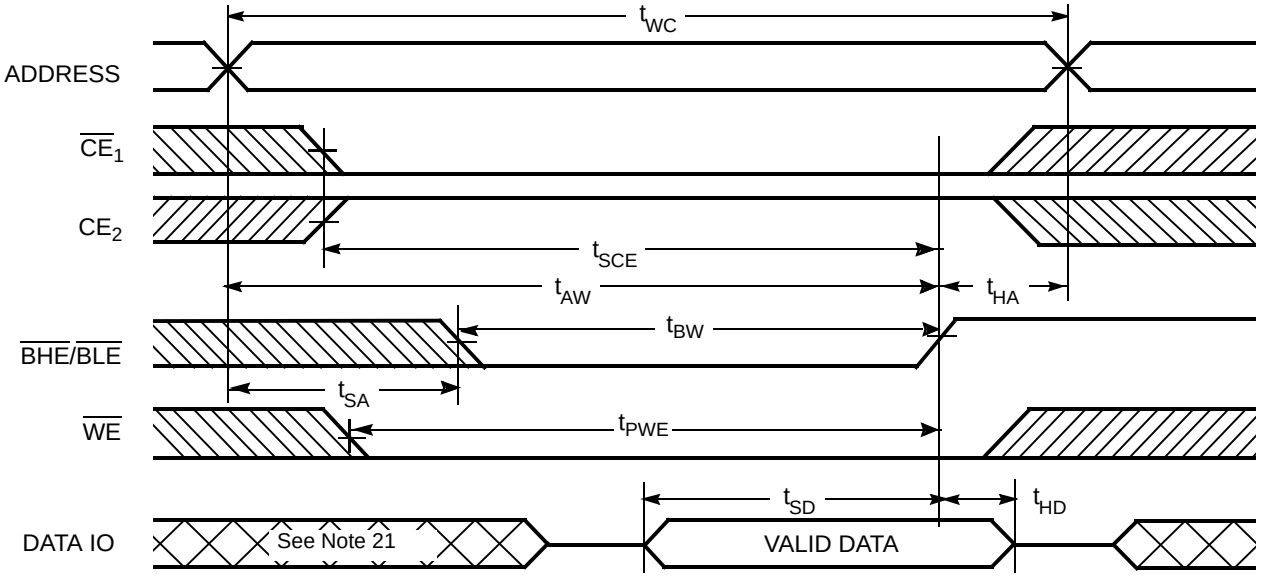
Notes:
19. Data IO is high impedance if $\overline{OE} = V_{IH}$.
20. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
21. During this period, the IOs are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 (WE Controlled, OE LOW)[20, 21]



Write Cycle 4 (BHE/BLE Controlled, OE LOW)[20, 21]



Truth Table

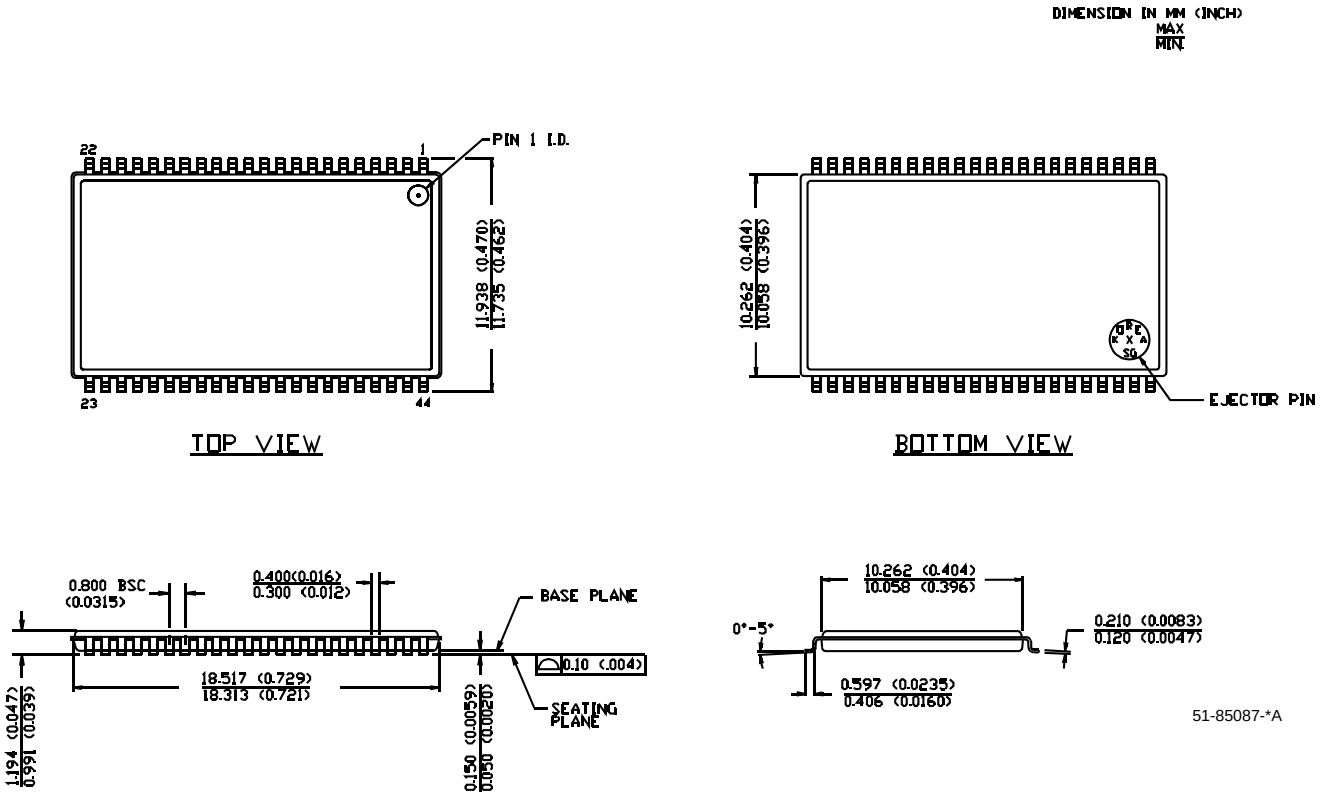
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (IO_0–IO_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (IO_0–IO_7); High Z (IO_8–IO_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (IO_0–IO_7); Data Out (IO_8–IO_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (IO_0–IO_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (IO_0–IO_7); High Z (IO_8–IO_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (IO_0–IO_7); Data In (IO_8–IO_{15})	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157ELL-45ZSXI	51-85087	44-pin Thin Small Outline Package Type II (Pb-free)	Industrial
55	CY62157ELL-55ZSXE	51-85087	44-pin Thin Small Outline Package Type II (Pb-free)	Automotive
	CY62157ELL-55BVXE	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	

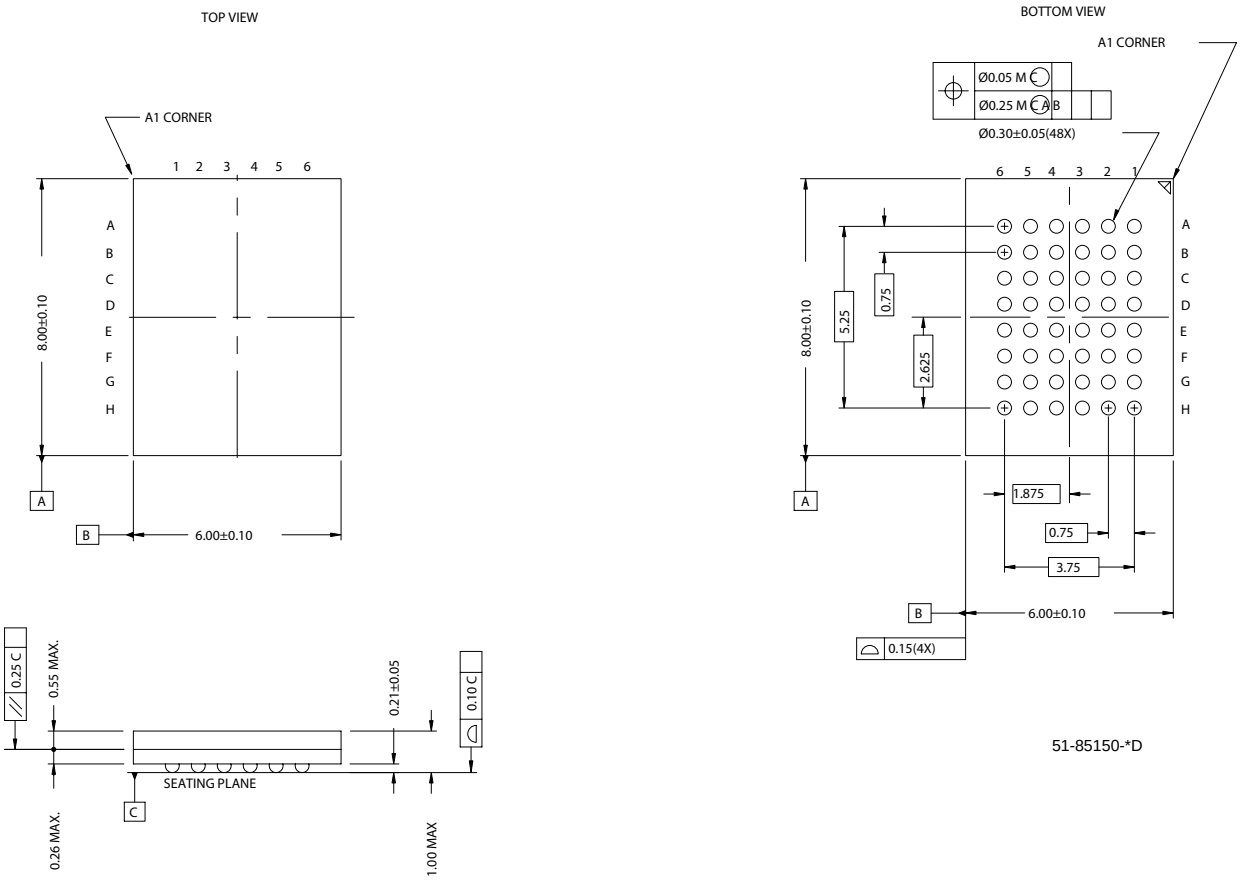
Package Diagrams

44-pin TSOP II (51-85087)



Package Diagrams (continued)

48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



MoBL is a registered trademark, and More Battery Life is a trademark, of Cypress Semiconductor Corporation. All product and company names mentioned in this document are the trademarks of their respective holders.

Document History Page

Document Title: CY62157E MoBL®, 8-Mbit (512K x 16) Static RAM Document Number: 38-05695				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	291273	See ECN	PCI	New data sheet
*A	457689	See ECN	NXR	Added Automotive Product Removed Industrial Product Removed 35 ns and 45 ns speed bins Removed “L” bin Updated AC Test Loads table Corrected t_R in Data Retention Characteristics from 100 µs to t_{RC} ns Updated the Ordering Information and replaced the Package Name column with Package Diagram
*B	467033	See ECN	NXR	Added Industrial Product (Final Information) Removed 48 ball VFBGA package and its relevant information Changed the $I_{CC(typ)}$ value of Automotive from 2 mA to 1.8 mA for f = 1MHz Changed the $I_{SB2(typ)}$ value of Automotive from 5 µA to 1.8 µA Modified footnote #4 to include current limit Updated the Ordering Information table
*C	569114	See ECN	VKN	Added 48 ball VFBGA package Updated Logic Block Diagram Added footnote #3 Updated the Ordering Information table