2-Mbit (256K x 8) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.20V–3.60V
- Pin compatible with CY62138CV25/30/33
- Ultra low standby power
  - — Typical standby current: 1 μA
  - — Maximum standby current: 5 μA
- Ultra low active power
  - — Typical active current: 1.6 mA @ f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 36-ball VFBGA, 32-pin TSOP II, 32-pin SOIC, 32-pin TSOP I and 32-pin STSOP packages

Functional Description [1]

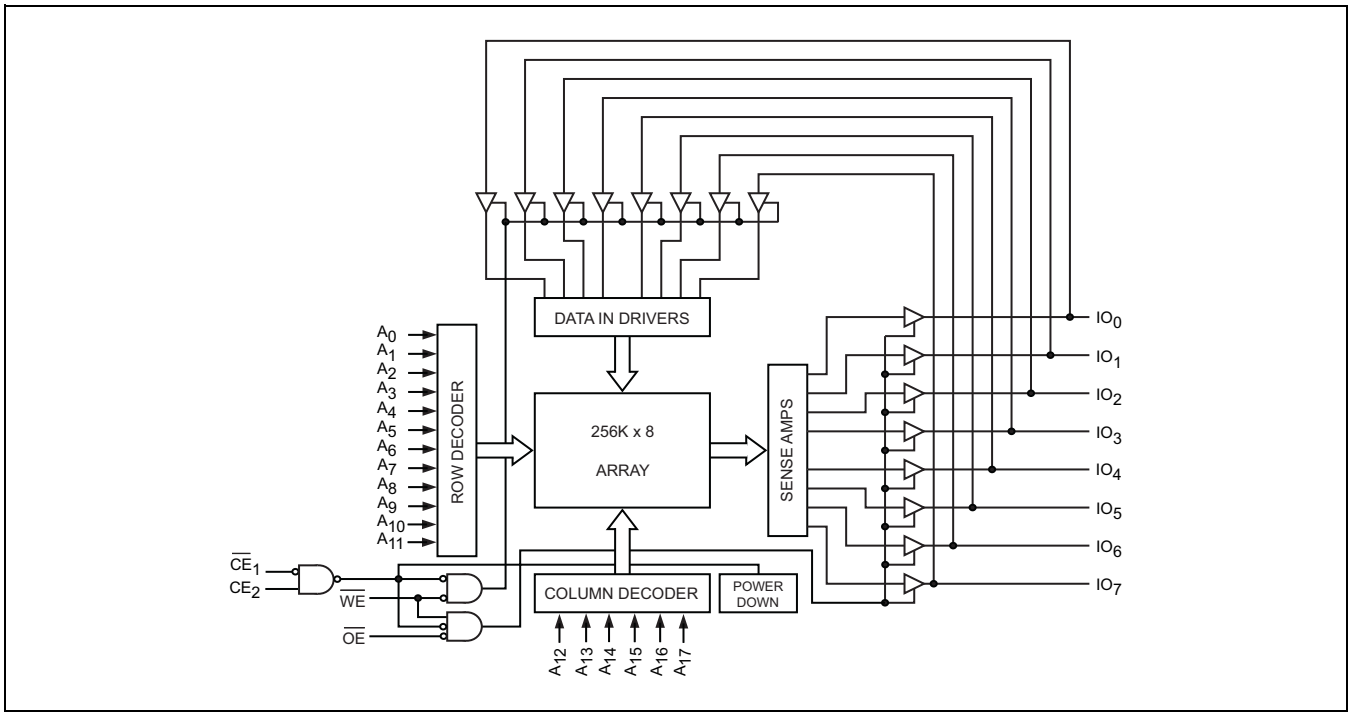
The CY62138FV30 is a high performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Place the device into standby mode reducing power consumption when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW).

To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight IO pins (IO_0 through IO_7) is then written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins.

The eight input and output pins (IO_0 through IO_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW).

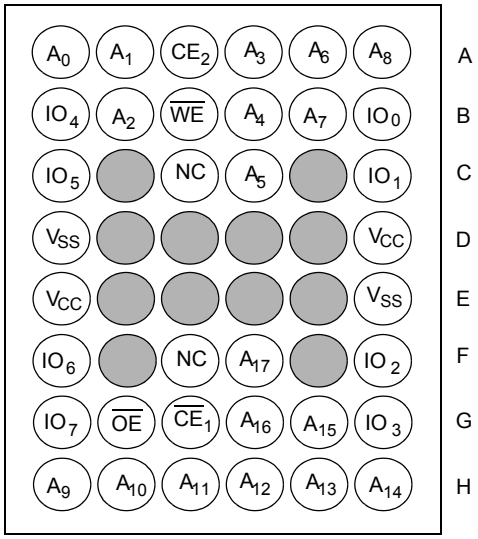
Logic Block Diagram



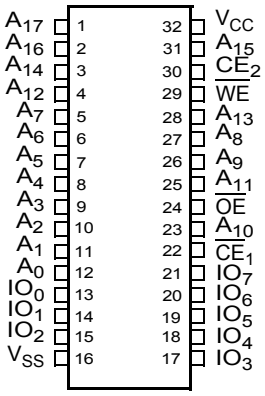
Note
1. For best practice recommendations, refer to the Cypress application note *"System Design Guidelines"* at http://www.cypress.com.

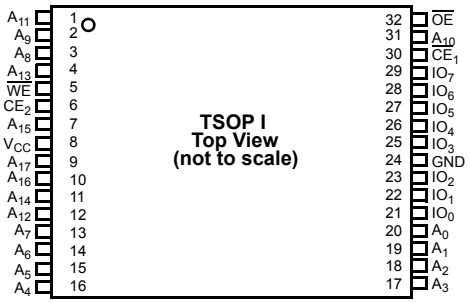
Pin Configuration [2]

36-Ball VFBGA
Top View



32-Pin SOIC/TSOP II
Top View





Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ [3]	Max		Typ [3]	Max	Typ [3]	Max	Typ [3]	Max
CY62138FV30LL	2.2	3.0	3.6	45	1.6	2.5	13	18	1	5

Note
2. NC pins are not connected on the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... 55°C to +125°C

Supply Voltage to Ground Potential..... –0.3V to 3.9V

DC Voltage Applied to Outputs in High-Z State [4, 5]..... –0.3V to 3.9V

DC Input Voltage [4, 5]..... –0.3V to 3.9V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Product	Range	Ambient Temperature	V_{CC} [6]
CY62138FV30LL	Industrial	–40°C to +85°C	2.2V to 3.6V

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ [3]	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA		2.0			V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70V		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA				0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70V				0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V		1.8		V_{CC} + 0.3V	V
		V_{CC}= 2.7V to 3.6V		2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V	For BGA package	–0.3		0.6	V
		V_{CC}= 2.7V to 3.6V		–0.3		0.8	V
		V_{CC} = 2.2V to 3.6V	For other packages	–0.3		0.6	V
I_{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$		–1		+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, output disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{max} = $1/t_{RC}$	V_{CC} = V_{CCmax}, I_{OUT} = 0 mA, CMOS levels		13	18	mA
		f = 1 MHz			1.6	2.5	
I_{SB1}	Automatic CE Power Down Current CMOS Inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2V or $CE_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V), f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), V_{CC} = 3.60V			1	5	µA
I_{SB2} [7]	Automatic CE Power Down Current CMOS Inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2V or $CE_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, f = 0, V_{CC} = 3.60V			1	5	µA

Capacitance (For all packages) [8]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ.)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

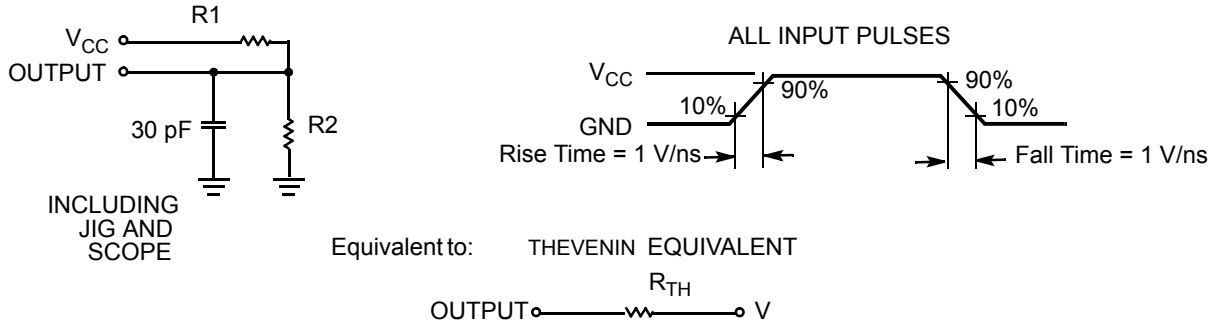
Notes

4. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = V_{CC}+0.75V for pulse durations less than 20 ns.
6. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
7. Only chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
8. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance [8]

Parameter	Description	Test Conditions	SOIC	VFBGA	TSOP II	STSOP	TSOP I	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 x 4.5 inch, two layer printed circuit board	44.53	38.49	44.16	59.72	50.19	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		24.05	17.66	11.97	15.38	14.59	°C/W

AC Test Loads and Waveforms

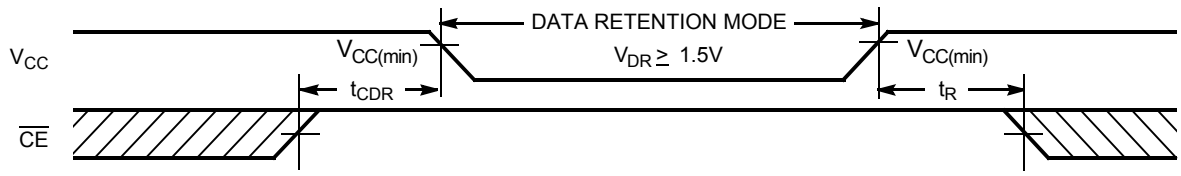


Parameters	2.5V (2.2V to 2.7V)	3.0V (2.7V to 3.6V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ [3]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR} [7]	Data Retention Current	V_{CC} = 1.5V, $\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		1	4	µA
t_{CDR} [8]	Chip Deselect to Data Retention Time		0			ns
t_R [9]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform [10]



Notes:
9. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
10. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Switching Characteristics (Over the Operating Range) [11]

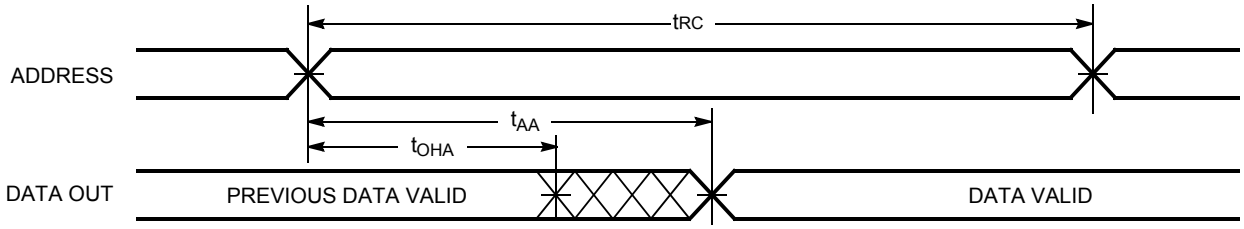
Parameter	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	45		ns
t_{AA}	Address to Data Valid		45	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z [12]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z [12,13]		18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z [12]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High-Z [12, 13]		18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power Down		45	ns
Write Cycle [14]				
t_{WC}	Write Cycle Time	45		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	35		ns
t_{AW}	Address Setup to Write End	35		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		ns
t_{SD}	Data Setup to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z [12, 13]		18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z [12]	10		ns

Notes

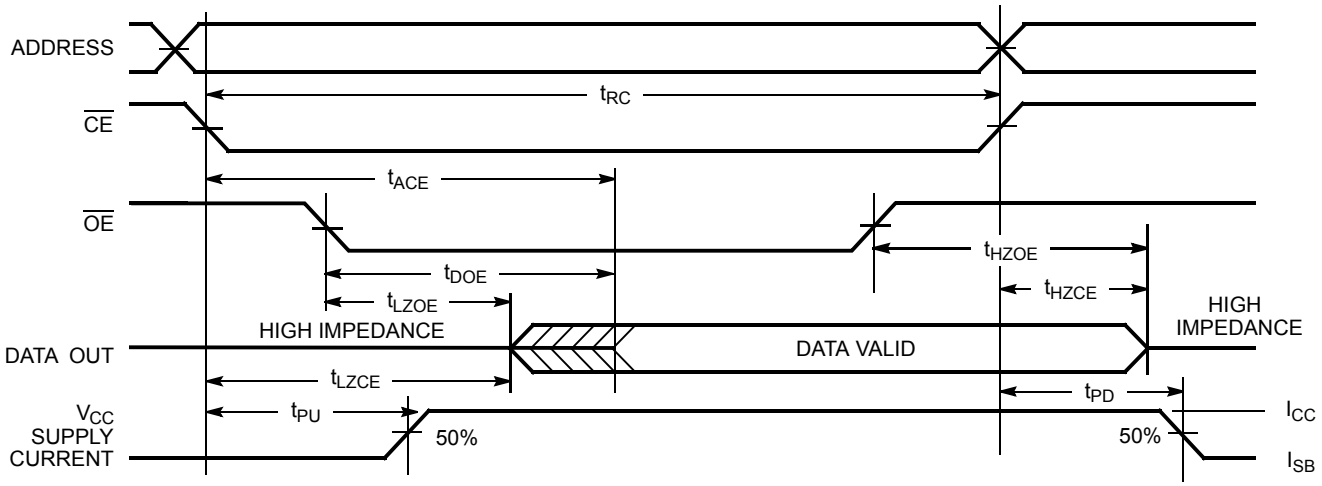
11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" on page 4 .
12. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
13. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enters a high impedance state.
14. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.

Switching Waveforms

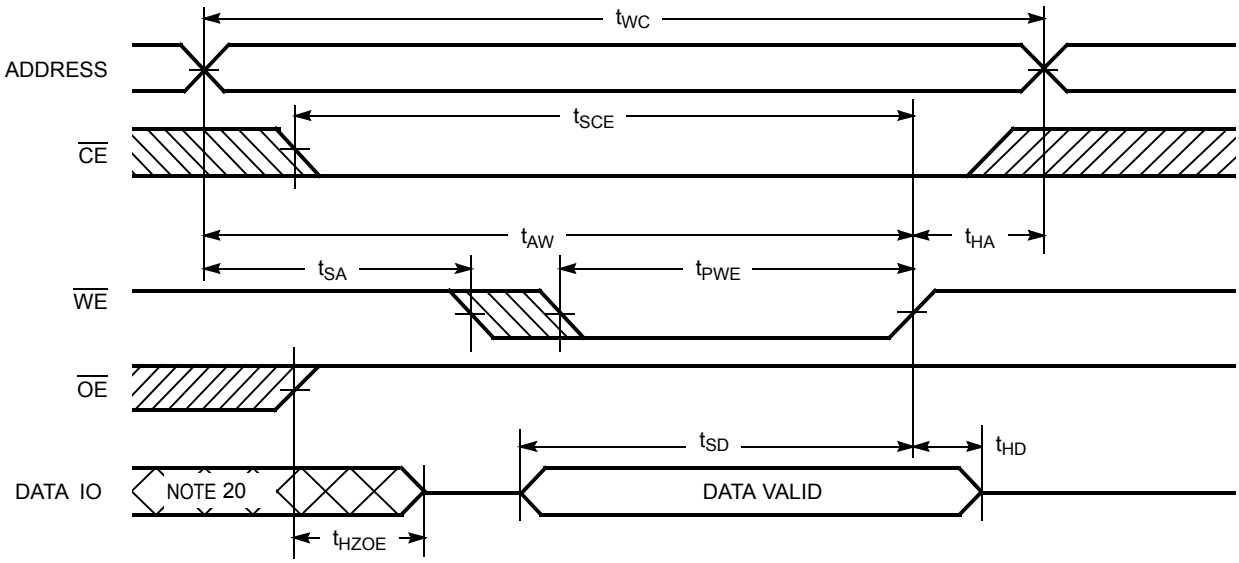
Read Cycle 1 (Address transition controlled) [15, 16]



Read Cycle No. 2 ($\overline{OE}$ controlled) [10, 16, 17]



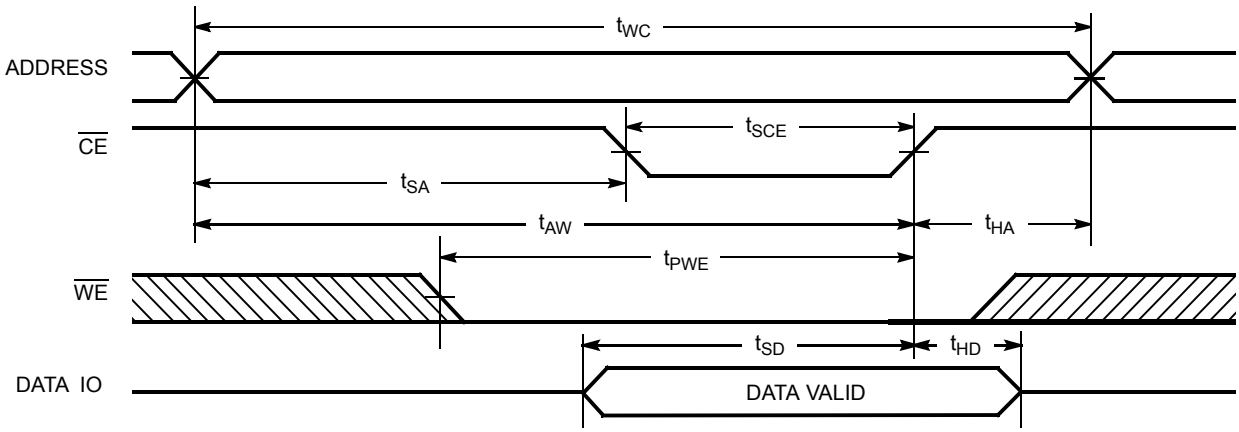
Write Cycle No. 1 ($\overline{WE}$ controlled) [10, 14, 18, 19]



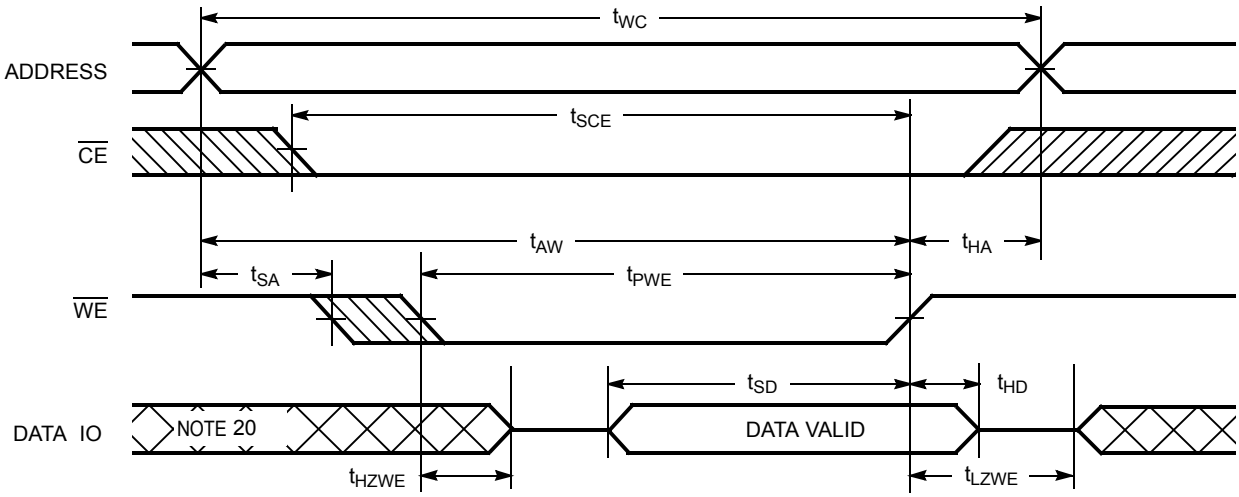
Notes:
15. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
16. $\overline{WE}$ is HIGH for read cycle.
17. Address valid before or similar to $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.
18. Data IO is high impedance if $\overline{OE}$ = V_{IH}.
19. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
20. During this period, the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE1}$ or CE2 controlled) [10, 14, 18, 19]



Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) [10, 19]



Truth Table

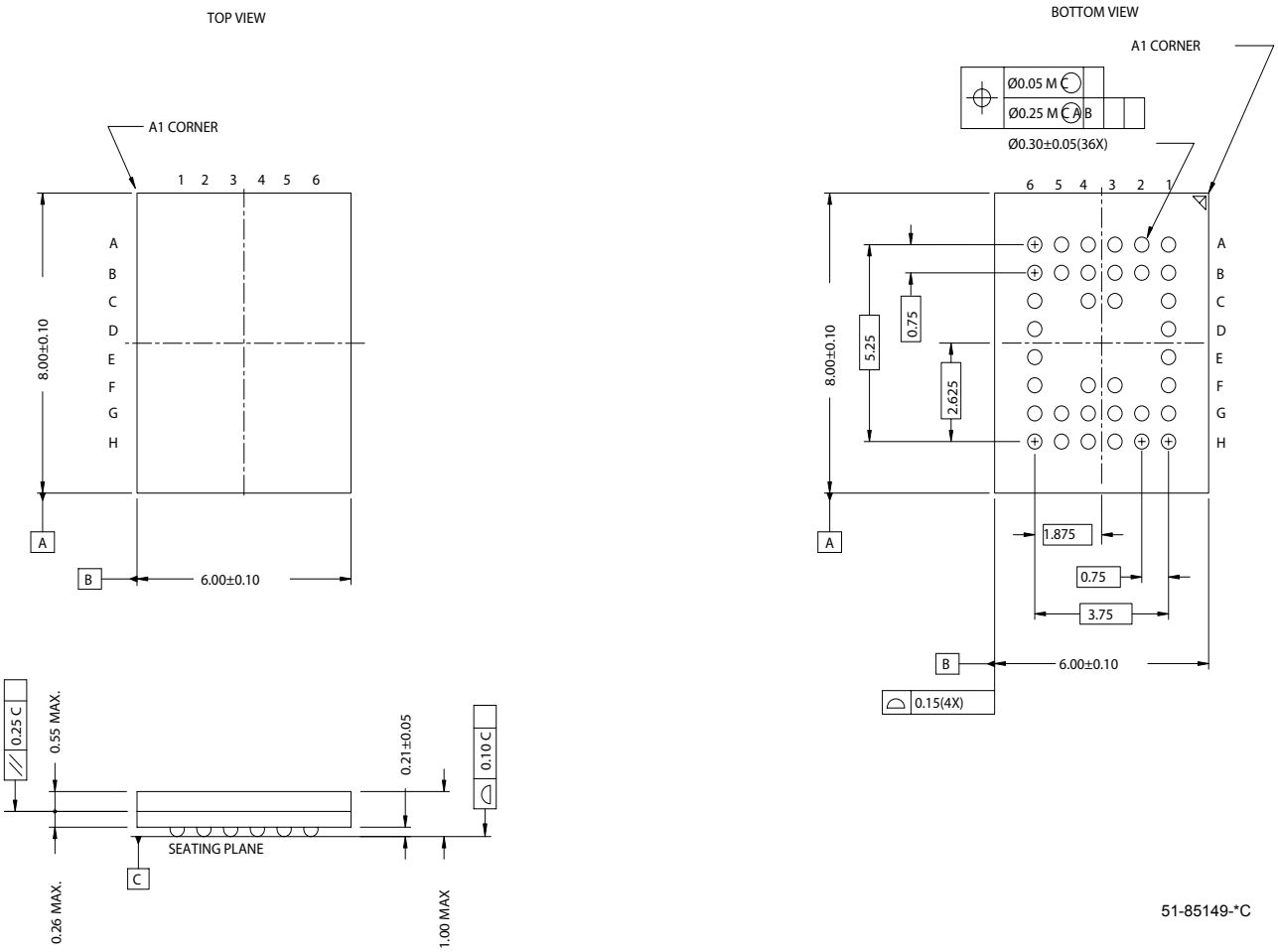
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High-Z	Deselect/Power Down	Standby (I_{SB})
X	L	X	X	High-Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	H	H	High-Z	Output Disabled	Active (I_{CC})
L	H	L	X	Data in	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138FV30LL-45BVXI	51-85149	36-ball VFBGA (Pb-free)	Industrial
	CY62138FV30LL-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
	CY62138FV30LL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	
	CY62138FV30LL-45ZXI	51-85056	32-pin TSOP I (Pb-free)	
	CY62138FV30LL-45SXI	51-85081	32-pin SOIC (Pb-free)	

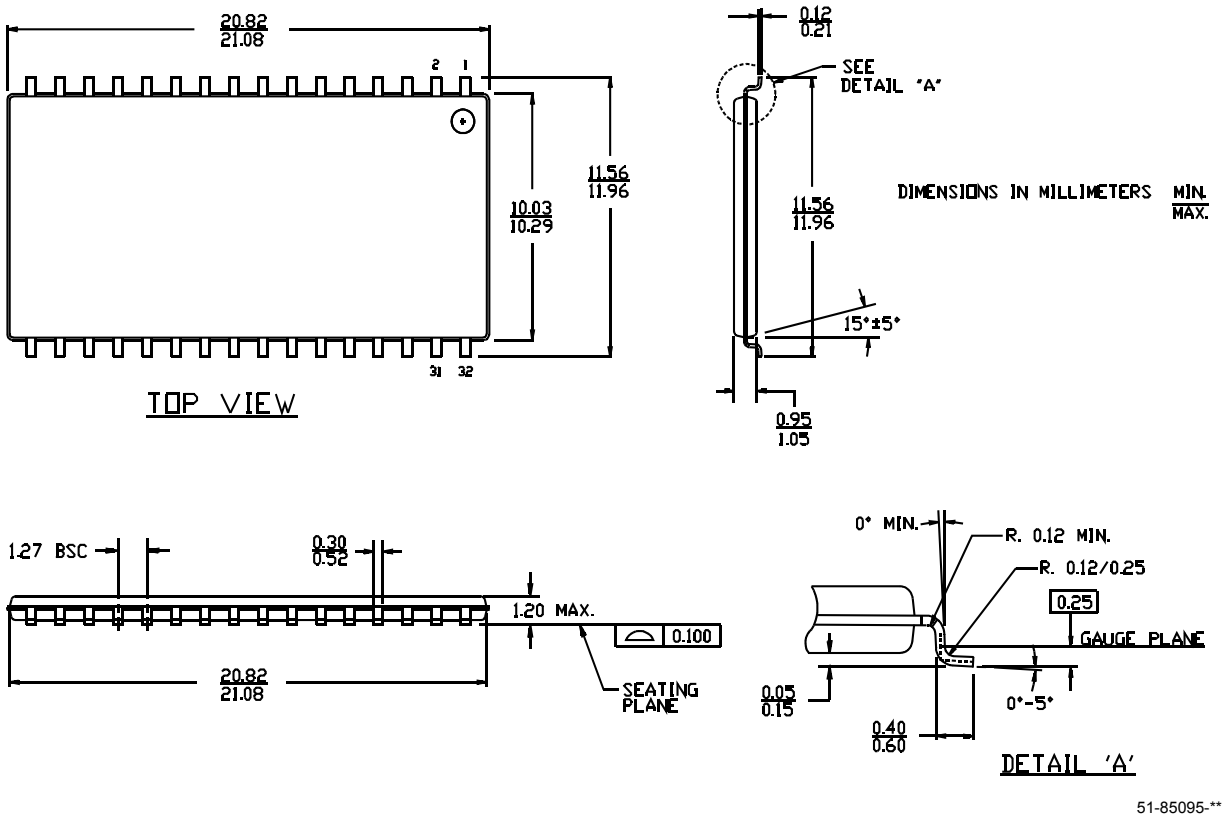
Package Diagrams

Figure 1. 36-ball VFBGA (6 x 8 x 1 mm), 51-85149



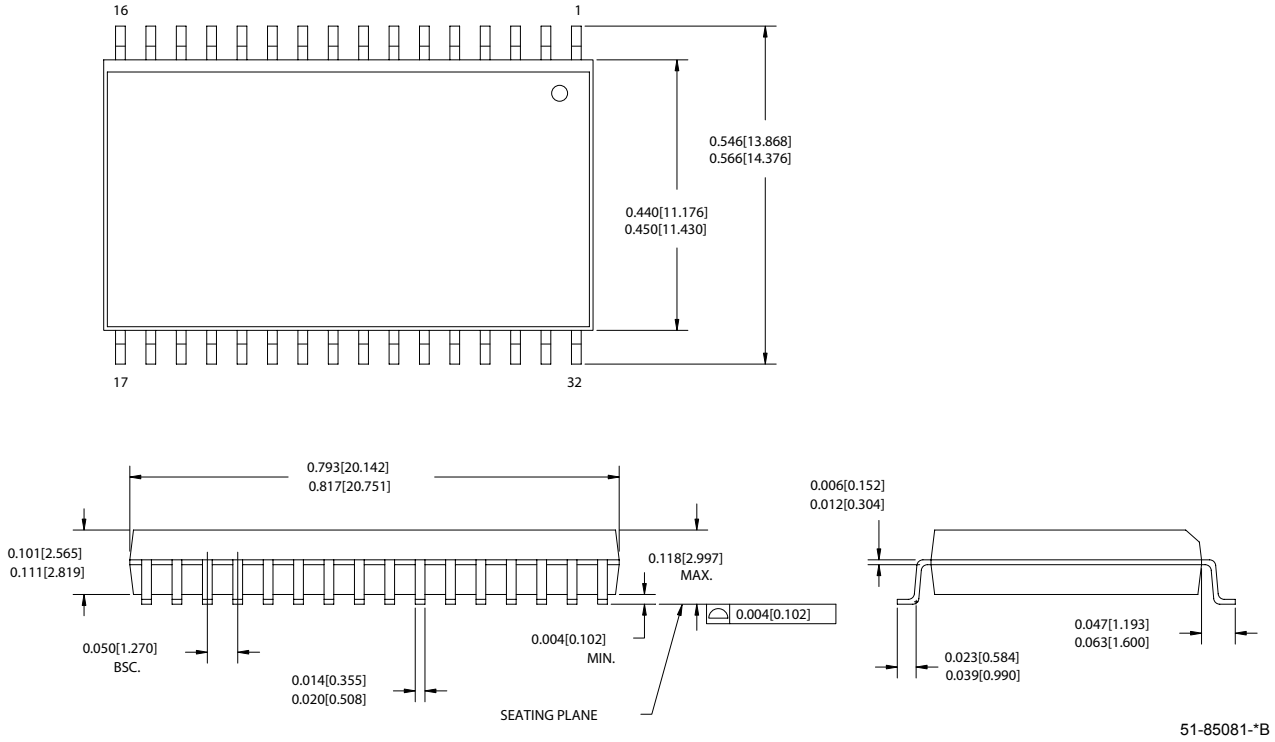
Package Diagrams (continued)

Figure 2. 32-pin TSOP II, 51-85095



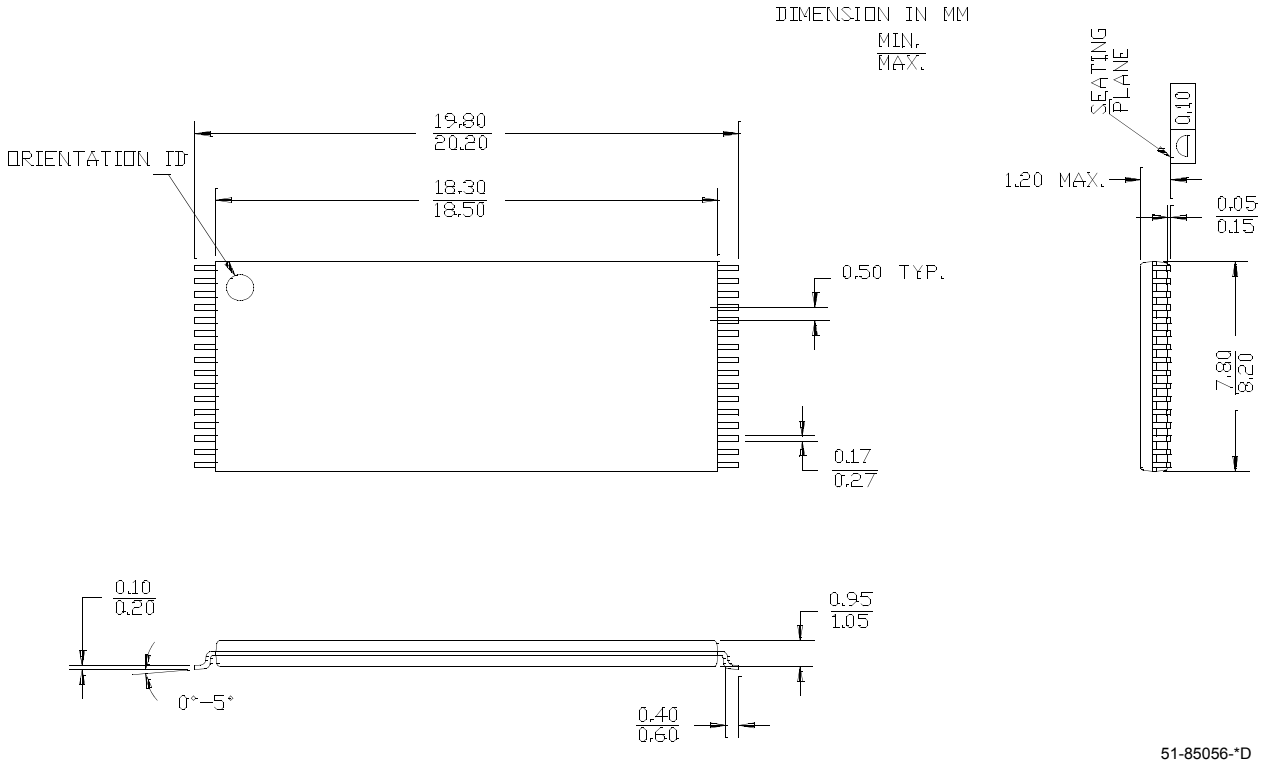
Package Diagrams (continued)

Figure 3. 32-pin (450 Mil) Molded SOIC, 51-85081



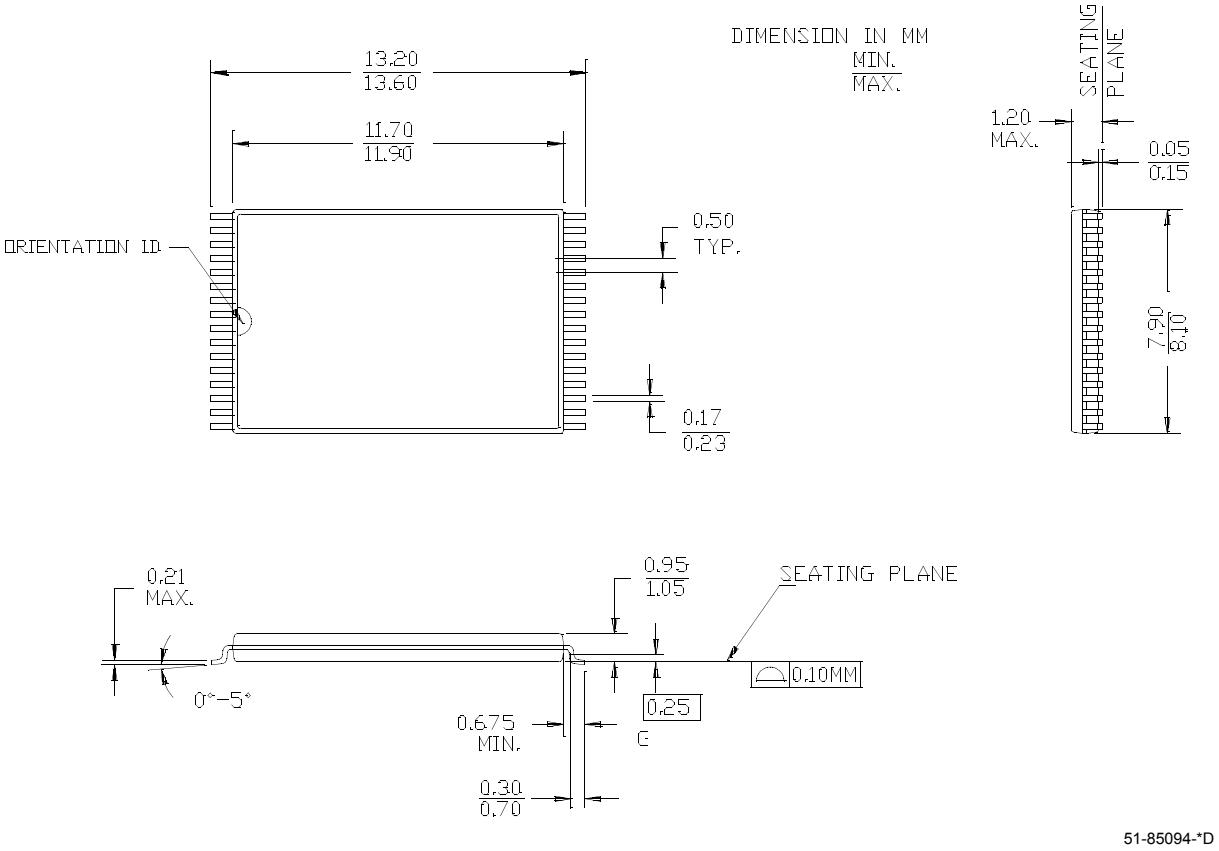
Package Diagrams (continued)

Figure 4. 32-pin TSOP I (8 x 20 mm), 51-85056



Package Diagrams (continued)

Figure 5. 32-pin STSOP (8 x 13.4 mm), 51-85094



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Document History Page

Document Title: CY62138FV30 MoBL®, 2-Mbit (256K x 8) Static RAM Document Number: 001-08029				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	463660	See ECN	NXR	New data sheet
*A	467351	See ECN	NXR	Added 32-pin TSOP II package, 32 pin TSOP I and 32 pin STSOP packages Changed ball A3 from NC to CE_2 in 36-ball FBGA pin out
*B	566724	See ECN	NXR	Converted from Preliminary to Final Corrected typo in 32 pin TSOP II pin configuration diagram on page #2 (changed pin 24 from CE_1 to OE and pin 22 from CE to CE_1) Changed the $I_{CC(max)}$ value from 2.25 mA to 2.5 mA for test condition f=1 MHz Changed the $I_{SB2(typ)}$ value from 0.5 µA to 1 µA Changed the $I_{SB2(max)}$ value from 2.5 µA to 5 µA Changed the $I_{CCDR(typ)}$ value from 0.5 µA to 1 µA and $I_{CCDR(max)}$ value from 2.5 µA to 4 µA
*C	797956	See ECN	VKN	Added 32-pin SOIC package Updated VIL spec for SOIC, TSOP-II, TSOP-I, and STSOP packages on Electrical characteristics table
*D	809101	See ECN	VKN	Corrected typo in the Ordering Information table
*E	940341	See ECN	VKN	Added footnote #7 related to I_{SB2} and I_{CCDR}