

## 4-Mbit (256K x 16) Static RAM

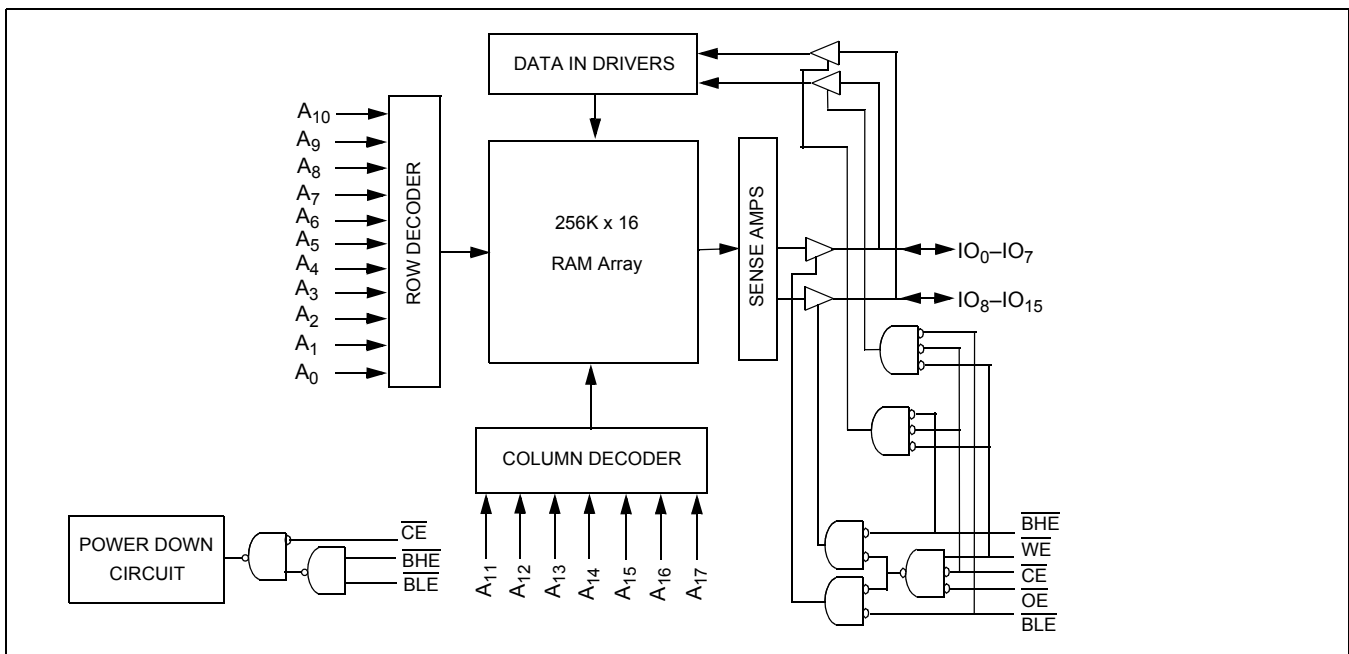
### Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: -40°C to +85°C
  - Automotive-A: -40°C to +85°C
  - Automotive-E: -40°C to +125°C
- Wide voltage range: 2.20V–3.60V
- Pin compatible with CY62147DV30
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 7  $\mu$ A (Industrial)
- Ultra low active power
  - Typical active current: 2 mA @ f = 1 MHz
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 48-ball VFBGA and 44-pin TSOPII packages
- Byte power down feature

### Functional Description <sup>[1]</sup>

The CY62147EV30 is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features

### Logic Block Diagram



#### Note

1. For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH or both  $\overline{BLE}$  and  $\overline{BHE}$  are HIGH). The input and output pins ( $IO_0$  through  $IO_{15}$ ) are placed in a high impedance state when:

- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH)
- Write operation is active ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW)

To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from IO pins ( $IO_0$  through  $IO_7$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from IO pins ( $IO_8$  through  $IO_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

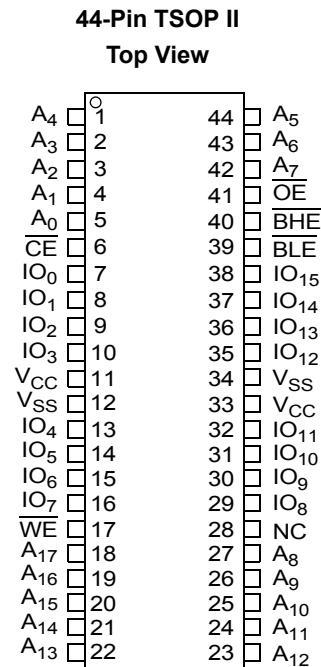
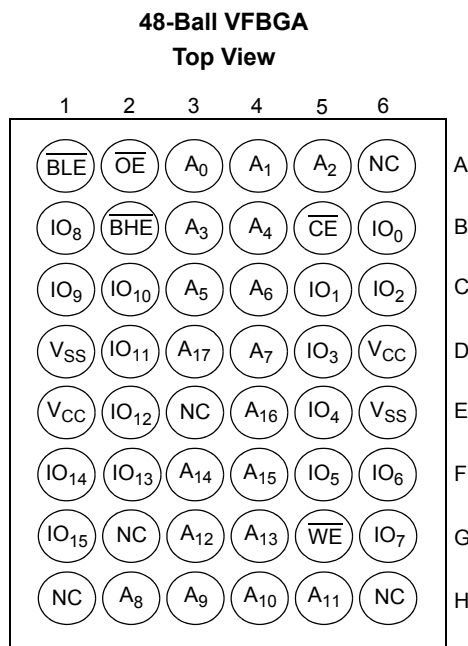
To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appear on  $IO_0$  to  $IO_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on  $IO_8$  to  $IO_{15}$ . See the "Truth Table" on page 9 for a complete description of read and write modes.

**Product Portfolio**

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
						f = 1MHz		f = f <sub>max</sub>			
Min	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max			
CY62147EV30LL	Ind'I/Auto-A	2.2	3.0	3.6	45 ns	2	2.5	15	20	1	7
CY62147EV30LL	Auto-E	2.2	3.0	3.6	55 ns	2	3	15	25	1	20

**Pin Configurations**

The figure that follows show the 48-ball VFBGA and 44-pin TSOP II pinouts.<sup>[3, 4]</sup>


**Notes**

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°.
- NC pins are not connected on the die.
- Pins H1, G2, and H6 in the BGA package are address expansion pins for 8 Mb, 16 Mb, and 32 Mb, respectively.

### Maximum Ratings

Exceeding the maximum ratings may shorten the battery life of the device. User guidelines are not tested.

Storage Temperature ..... -65°C to + 150°C  
 Ambient Temperature with Power Applied ..... -55°C to + 125°C  
 Supply Voltage to Ground Potential ..... -0.3V to + 3.9V ( $V_{CCmax} + 0.3V$ )  
 DC Voltage Applied to Outputs in High-Z State <sup>[5, 6]</sup> ..... -0.3V to 3.9V ( $V_{CCmax} + 0.3V$ )  
 DC Input Voltage <sup>[5, 6]</sup> ..... -0.3V to 3.9V ( $V_{CCmax} + 0.3V$ )

Output Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... >2001V (MIL-STD-883, Method 3015)  
 Latch up Current..... >200 mA

### Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[7]</sup>
CY62147EV30LL	Ind'I/Auto-A	-40°C to +85°C	2.2V to 3.6V
	Auto-E	-40°C to +125°C	

### Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Ind'I/Auto-A)			55 ns (Auto-E)			Unit
			Min	Typ <sup>[2]</sup>	Max	Min	Typ <sup>[2]</sup>	Max	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	2.0			2.0			V
		I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> ≥ 2.70V	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA			0.4			0.4	V
		I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 2.70V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.2V to 2.7V	1.8		V <sub>CC</sub> + 0.3	1.8		V <sub>CC</sub> + 0.3	V
		V <sub>CC</sub> = 2.7V to 3.6V	2.2		V <sub>CC</sub> + 0.3	2.2		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.2V to 2.7V	-0.3		0.6	-0.3		0.6	V
		V <sub>CC</sub> = 2.7V to 3.6V	-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-4		+4	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-4		+4	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>max</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = V <sub>CC(max)</sub> I <sub>OUT</sub> = 0 mA CMOS levels		15	20		15	25	mA
		f = 1 MHz		2	2.5		2	3	
I <sub>SB1</sub>	Automatic CE Power Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V, V_{IN} \leq 0.2V$ f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, BHE, BLE and WE), V <sub>CC</sub> = 3.60V		1	7		1	20	μA
I <sub>SB2</sub> <sup>[8]</sup>	Automatic CE Power Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , f = 0, V <sub>CC</sub> = 3.60V		1	7		1	20	μA

### Capacitance

For all packages.<sup>[9]</sup>

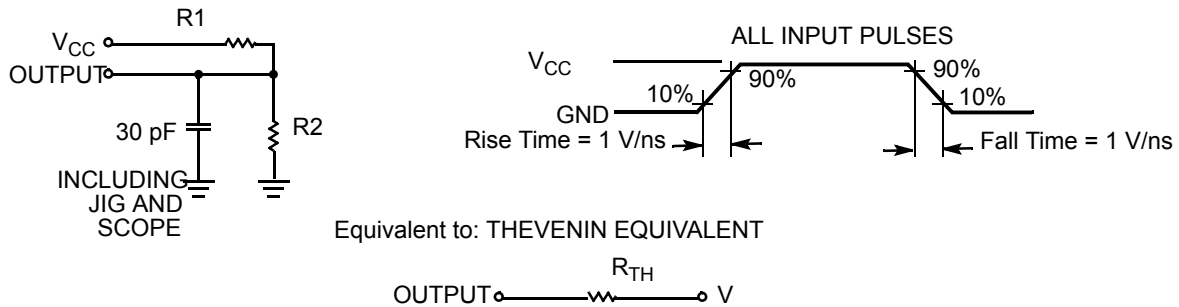
Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ)</sub>		

#### Notes

- V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
- Only chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.

**Thermal Resistance<sup>[9]</sup>**

Parameter	Description	Test Conditions	VFPGA Package	TSOP II Package	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	77	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		10	13	°C/W

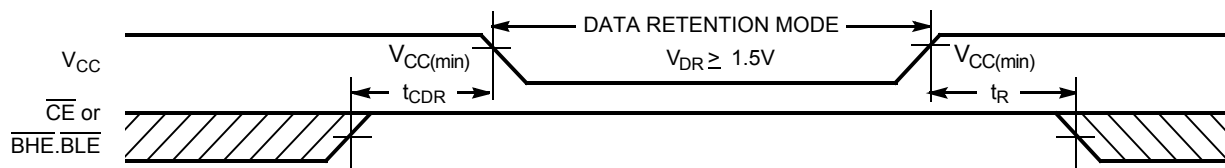
**AC Test Loads and Waveforms**
**Figure 1. AC Test Load and Waveforms**


Parameters	2.50V	3.0V	Unit
R1	16667	1103	$\Omega$
R2	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

**Data Retention Characteristics**

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[2]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5			V
$I_{CCDR}$ <sup>[8]</sup>	Data Retention Current	$V_{CC} = 1.5V, \overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Ind'I/Auto-A	0.8	7	$\mu A$
			Auto-E			12
$t_{CDR}$ <sup>[9]</sup>	Chip Deselect to Data Retention Time		0			ns
$t_R$ <sup>[10]</sup>	Operation Recovery Time		$t_{RC}$			ns

**Data Retention Waveform<sup>[11]</sup>**
**Figure 2. Data Retention Waveform**

**Notes**

 10. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100 \mu s$  or stable at  $V_{CC(min)} \geq 100 \mu s$ .

11. BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling both BHE and BLE.

**Switching Characteristics**

 Over the Operating Range <sup>[12, 13]</sup>

Parameter	Description	45 ns (Ind'l/Auto-A)		55 ns (Auto-E)		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	45		55		ns
t <sub>AA</sub>	Address to Data Valid		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		45		55	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		22		25	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[14]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[14, 15]</sup>		18		20	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[14]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[14, 15]</sup>		18		20	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power Down		45		55	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45		55	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[14]</sup>	10		10		ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z <sup>[14, 15]</sup>		18		20	ns
<b>Write Cycle<sup>[16]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	45		55		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	35		40		ns
t <sub>AW</sub>	Address Setup to Write End	35		40		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	35		40		ns
t <sub>BW</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Write End	35		40		ns
t <sub>SD</sub>	Data Setup to Write End	25		25		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[14, 15]</sup>		18		20	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[14]</sup>	10		10		ns

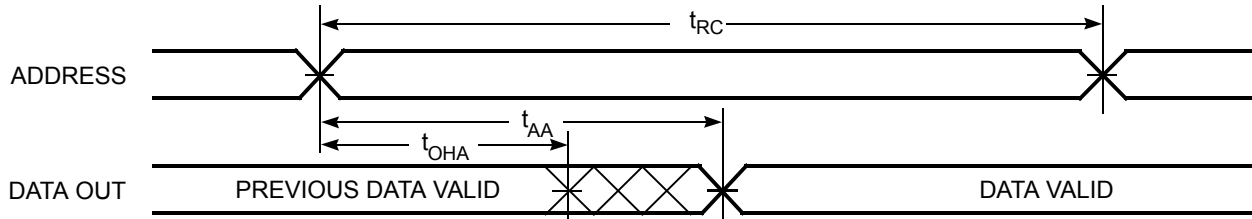
**Notes**

12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" on page 4.
13. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See application note AN13842 for further clarification.
14. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.
15. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
16. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

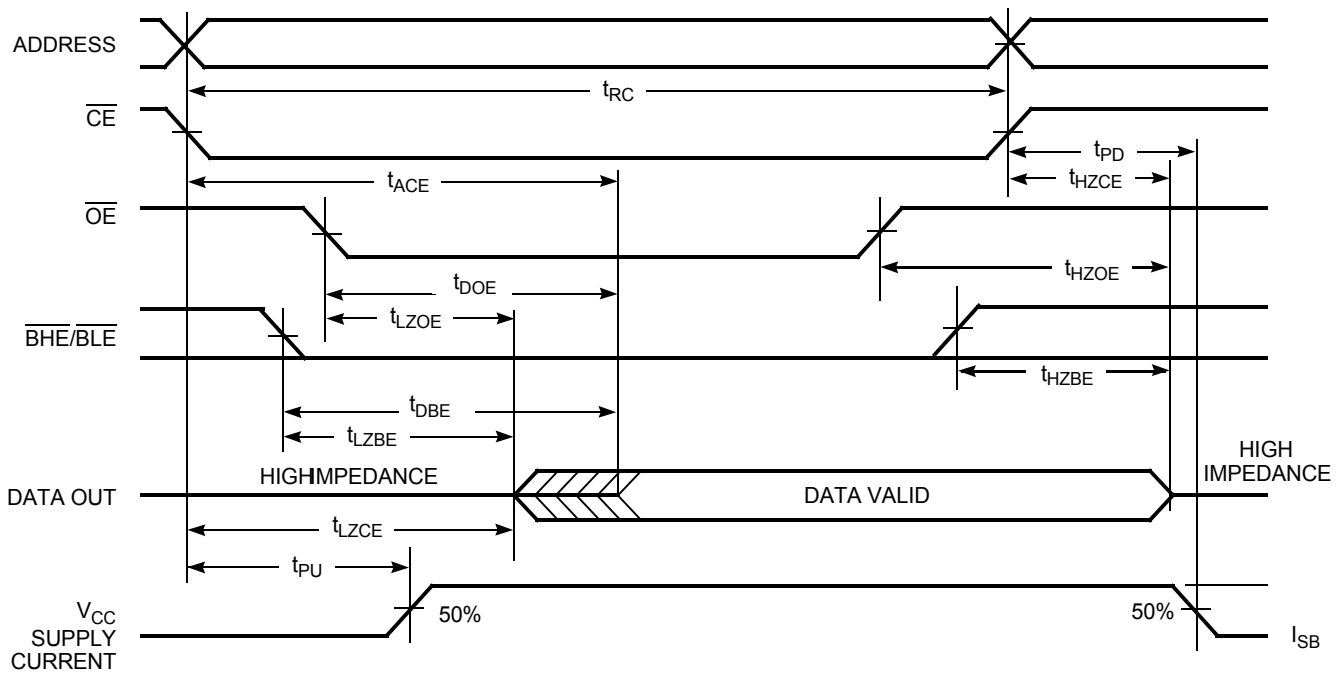
Read Cycle No. 1 (Address Transition Controlled)<sup>[17, 18]</sup>

Figure 3. Read Cycle No. 1



Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[18, 19]</sup>

Figure 4. Read Cycle No. 2



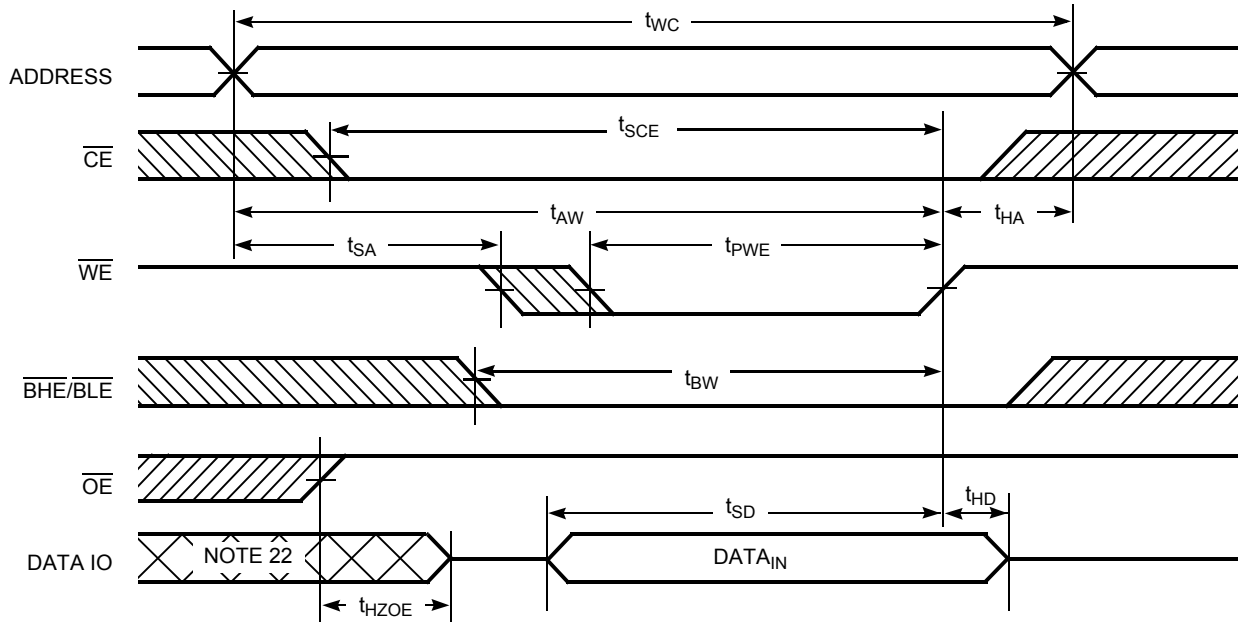
**Notes**

- 17. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ .
- 18.  $\overline{WE}$  is HIGH for read cycle.
- 19. Address valid before or similar to  $\overline{CE}$  and  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

**Switching Waveforms (continued)**

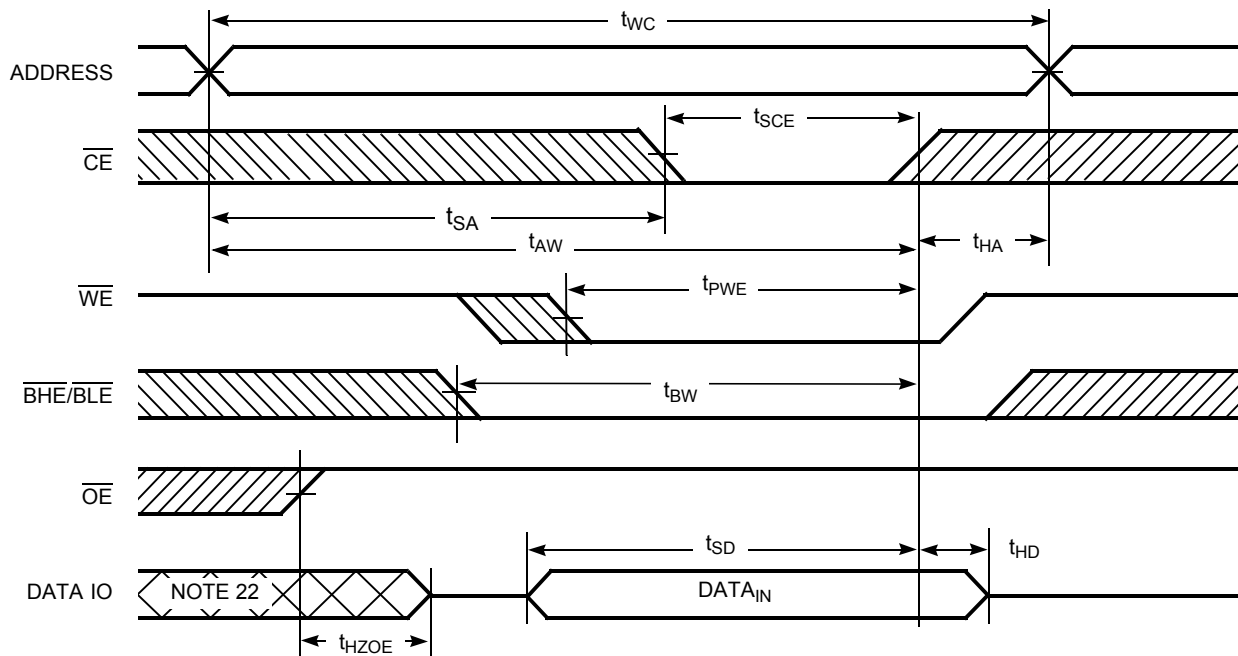
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[16, 20, 21]</sup>**

**Figure 5. Write Cycle No. 1**



**Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[16, 20, 21]</sup>**

**Figure 6. Write Cycle No. 2**



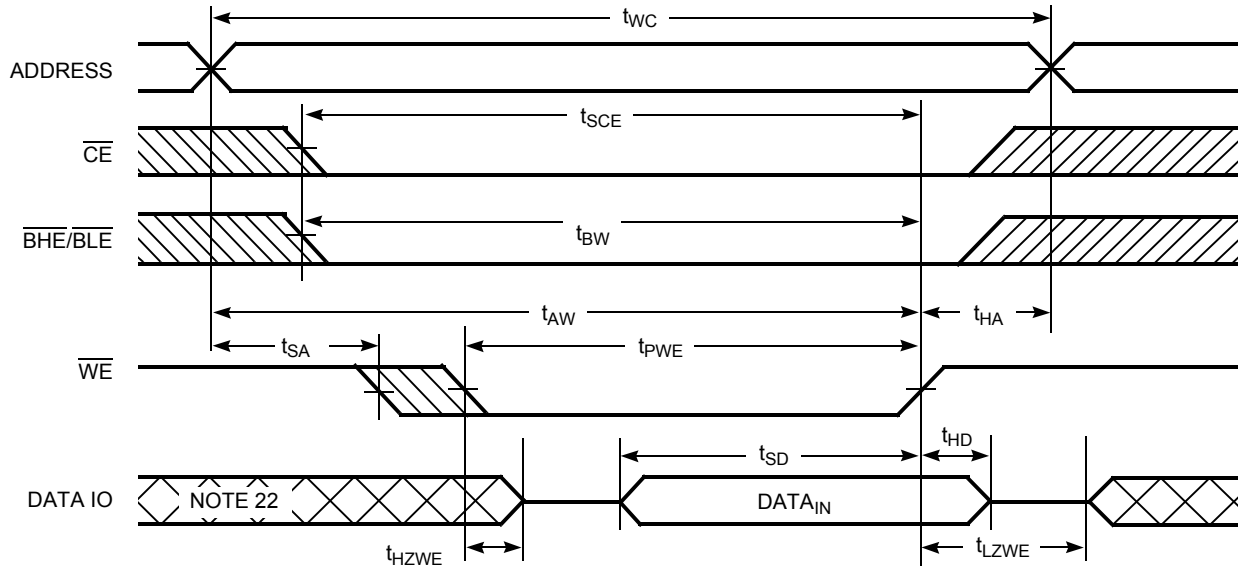
**Notes**

- 20. Data IO is high impedance if  $\overline{OE} = V_{IH}$ .
- 21. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 22. During this period, the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

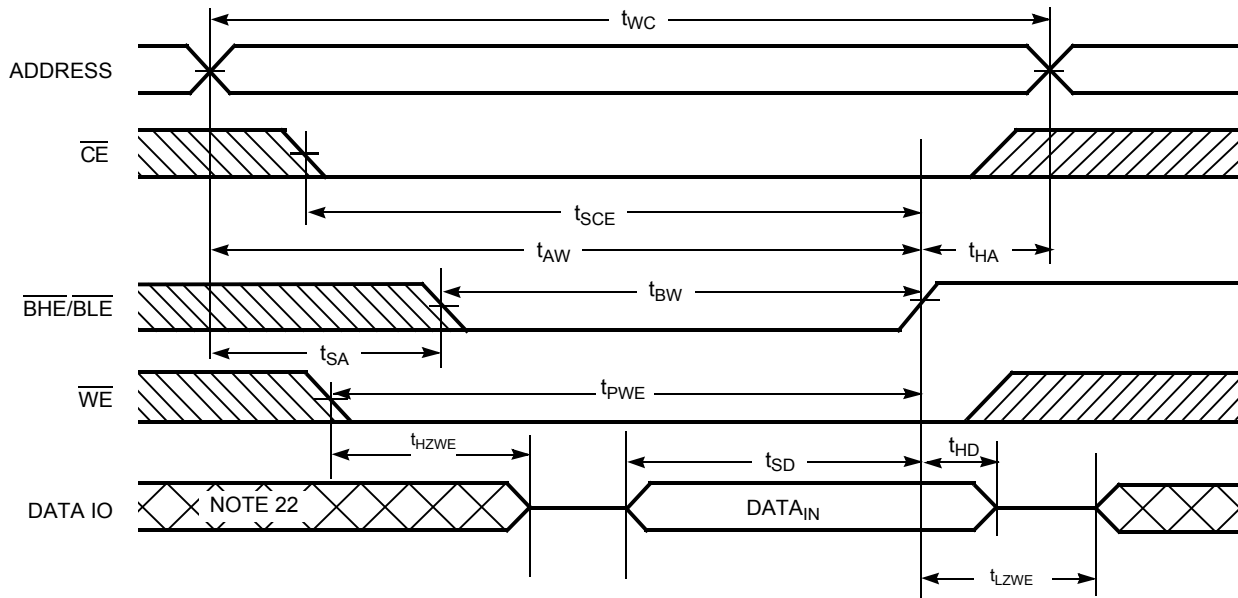
Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[21]</sup>

Figure 7. Write Cycle No. 3



Write Cycle No. 4 ( $\overline{BHE/BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[21]</sup>

Figure 8. Write Cycle No. 4





**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	IOs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power down	Standby ( $I_{\text{SB}}$ )
L	X	X	H	H	High Z	Deselect/Power down	Standby ( $I_{\text{SB}}$ )
L	H	L	L	L	Data Out ( $\text{IO}_0\text{--}\text{IO}_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	L	H	L	Data Out ( $\text{IO}_0\text{--}\text{IO}_7$ ); $\text{IO}_8\text{--}\text{IO}_{15}$ in High Z	Read	Active ( $I_{\text{CC}}$ )
L	H	L	L	H	Data Out ( $\text{IO}_8\text{--}\text{IO}_{15}$ ); $\text{IO}_0\text{--}\text{IO}_7$ in High Z	Read	Active ( $I_{\text{CC}}$ )
L	H	H	L	L	High Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	H	H	L	High Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	H	H	L	H	High Z	Output Disabled	Active ( $I_{\text{CC}}$ )
L	L	X	L	L	Data In ( $\text{IO}_0\text{--}\text{IO}_{15}$ )	Write	Active ( $I_{\text{CC}}$ )
L	L	X	H	L	Data In ( $\text{IO}_0\text{--}\text{IO}_7$ ); $\text{IO}_8\text{--}\text{IO}_{15}$ in High Z	Write	Active ( $I_{\text{CC}}$ )
L	L	X	L	H	Data In ( $\text{IO}_8\text{--}\text{IO}_{15}$ ); $\text{IO}_0\text{--}\text{IO}_7$ in High Z	Write	Active ( $I_{\text{CC}}$ )

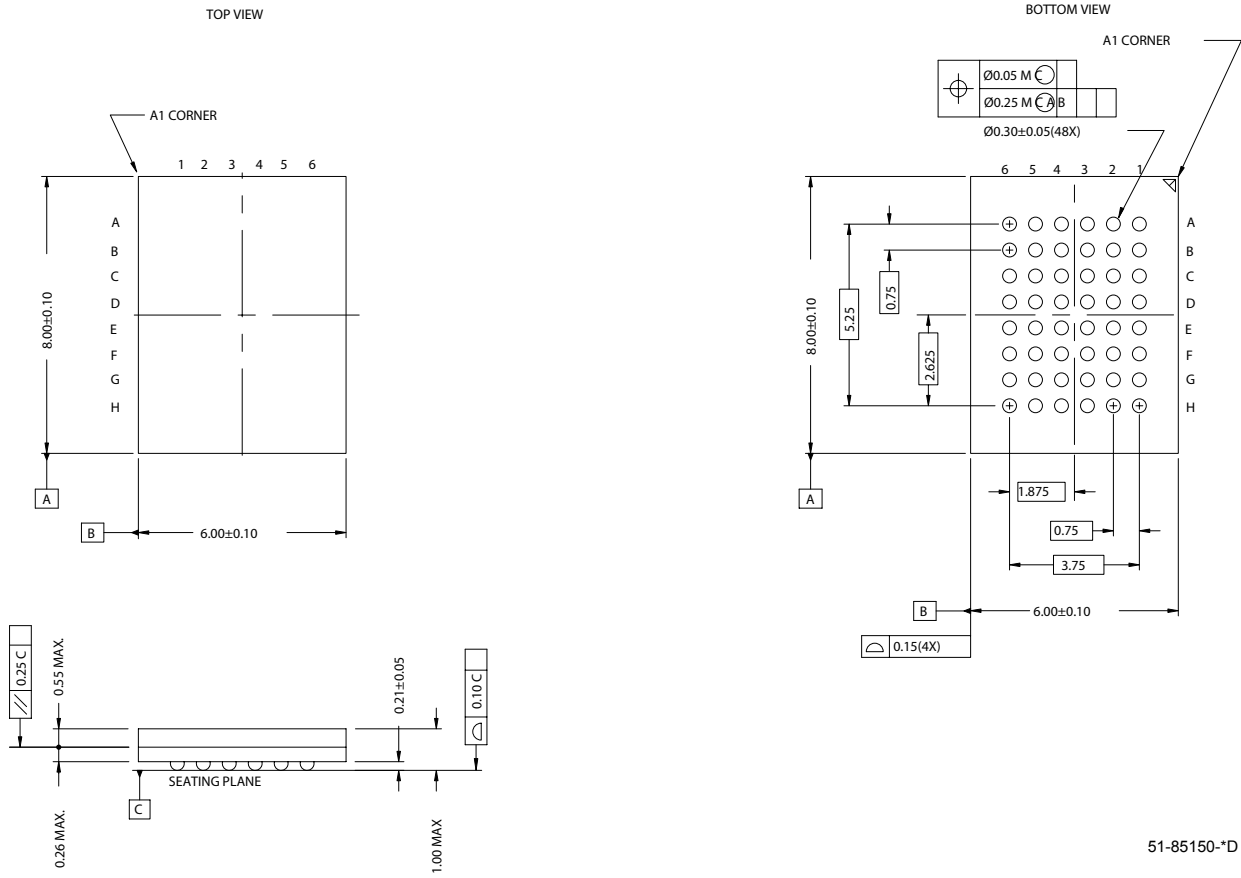
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62147EV30LL-45BVI	51-85150	48-ball Very Fine Pitch Ball Grid Array	Industrial
	CY62147EV30LL-45BVXI	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	
	CY62147EV30LL-45ZSXI	51-85087	44-pin Thin Small Outline Package II (Pb-free)	
45	CY62147EV30LL-45BVXA	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	Automotive-A
55	CY62147EV30LL-55ZSXE	51-85087	44-pin Thin Small Outline Package II (Pb-free)	Automotive-E

Contact your local Cypress sales representative for availability of these parts.

Package Diagrams

Figure 9. 48-Ball VFBGA (6 x 8 x 1 mm), 51-85150

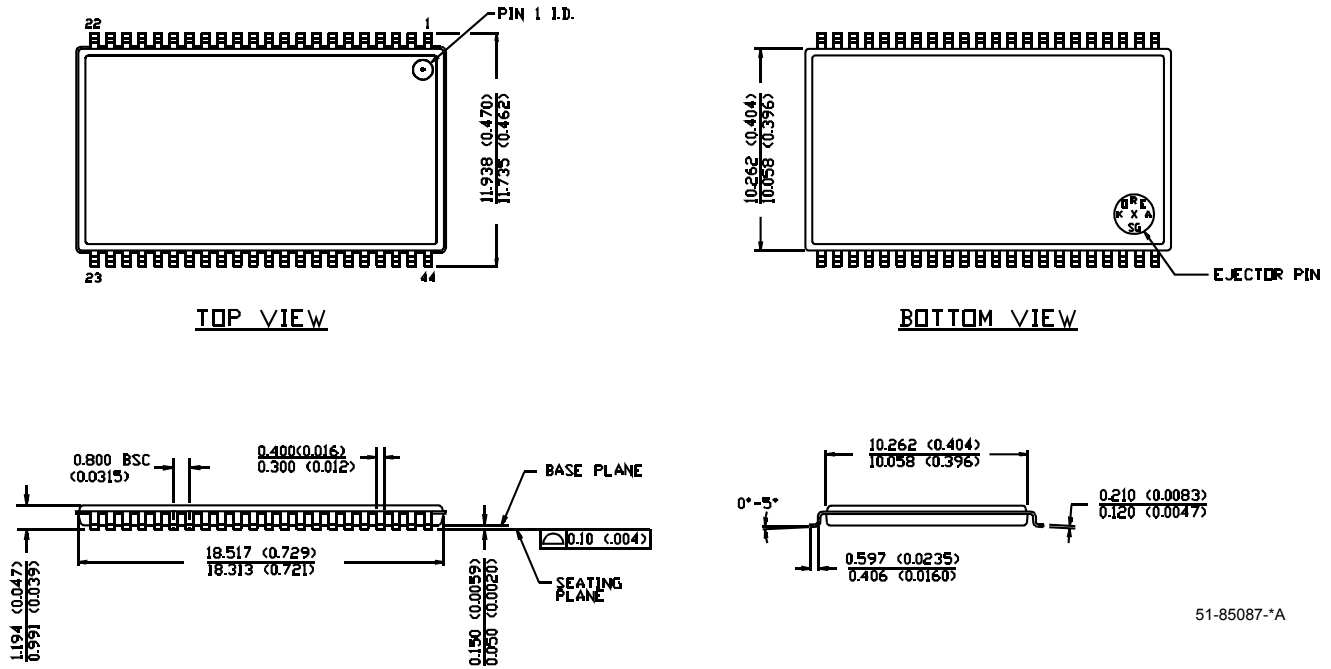


51-85150-\*D

Package Diagrams (continued)

Figure 10. 44-Pin TSOP II, 51-85087

DIMENSION IN MM (INCH)  
MAX  
MIN



51-85087-\*A

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**Document History Page**

Document Title: CY62147EV30 MoBL® 4-Mbit (256K x 16) Static RAM				
Document Number: 38-05440				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201861	01/13/04	AJU	New Data Sheet
*A	247009	See ECN	SYT	<p>Changed from Advanced Information to Preliminary</p> <p>Moved Product Portfolio to Page 2</p> <p>Changed Vcc stabilization time in footnote #8 from 100 <math>\mu</math>s to 200 <math>\mu</math>s</p> <p>Removed Footnote #15(<math>t_{LZBE}</math>) from Previous Revision</p> <p>Changed <math>I_{CCDR}</math> from 2.0 <math>\mu</math>A to 2.5 <math>\mu</math>A</p> <p>Changed <math>t_{\text{typ}}</math> in Data Retention Characteristics(<math>t_R</math>) from 100 <math>\mu</math>s to <math>t_{RC}</math> ns</p> <p>Changed <math>t_{OHA}</math> from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin</p> <p>Changed <math>t_{HZOE}</math>, <math>t_{HZBE}</math>, <math>t_{HZWE}</math> from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin</p> <p>Changed <math>t_{SCE}</math> and <math>t_{BW}</math> from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin</p> <p>Changed <math>t_{HZCE}</math> from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin</p> <p>Changed <math>t_{SD}</math> from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin</p> <p>Changed <math>t_{DOE}</math> from 15 to 18 ns for 35 ns Speed Bin</p> <p>Changed Ordering Information to include Pb-Free Packages</p>
*B	414807	See ECN	ZSD	<p>Changed from Preliminary information to Final</p> <p>Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed 35ns Speed Bin</p> <p>Removed "L" version of CY62147EV30</p> <p>Changed ball E3 from DNU to NC.</p> <p>Removed redundant foot note on DNU.</p> <p>Changed <math>I_{CC}</math> (Max) value from 2 mA to 2.5 mA and <math>I_{CC}</math> (Typ) value from 1.5 mA to 2 mA at <math>f=1</math> MHz</p> <p>Changed <math>I_{CC}</math> (Typ) value from 12 mA to 15 mA at <math>f = f_{\text{max}}</math></p> <p>Changed <math>I_{SB1}</math> and <math>I_{SB2}</math> Typ values from 0.7 <math>\mu</math>A to 1 <math>\mu</math>A and Max values from 2.5 <math>\mu</math>A to 7 <math>\mu</math>A.</p> <p>Changed <math>I_{CCDR}</math> from 2.5 <math>\mu</math>A to 7 <math>\mu</math>A.</p> <p>Added <math>I_{CCDR}</math> typical value.</p> <p>Changed AC test load capacitance from 50 pF to 30 pF on Page #4.</p> <p>Changed <math>t_{LZOE}</math> from 3 ns to 5 ns</p> <p>Changed <math>t_{LZCE}</math>, <math>t_{LZBE}</math> and <math>t_{LZWE}</math> from 6 ns to 10 ns</p> <p>Changed <math>t_{HZCE}</math> from 22 ns to 18 ns</p> <p>Changed <math>t_{PWE}</math> from 30 ns to 35 ns.</p> <p>Changed <math>t_{SD}</math> from 22 ns to 25 ns.</p> <p>Updated the package diagram 48-pin VFBGA from *B to *D</p> <p>Updated the ordering information table and replaced the Package Name column with Package Diagram.</p>
*C	464503	See ECN	NXR	<p>Included Automotive Range in product offering</p> <p>Updated the Ordering Information</p>
*D	925501	See ECN	VKN	<p>Added Preliminary Automotive-A information</p> <p>Added footnote #9 related to <math>I_{SB2}</math> and <math>I_{CCDR}</math></p> <p>Added footnote #14 related AC timing parameters</p>
*E	1045701	See ECN	VKN	Converted Automotive-A and Automotive -E specs from preliminary to final