

# 1-Mbit (64K x 16) Static RAM

## Features

- **Very high speed**
  - 55 ns
- **Temperature Ranges**
  - Industrial: -40°C to 85°C
  - Automotive: -40°C to 125°C
- **Wide voltage range**
  - 2.2V - 3.6V
- **Pin compatible with CY62126BV**
- **Ultra-low active power**
  - Typical active current: 0.85 mA @ f = 1 MHz
  - Typical active current: 5 mA @ f = f<sub>Max</sub> (55 ns speed)
- **Ultra-low standby power**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**
- **Automatic power-down when deselected**
- **Available in Pb-free and non Pb-free 48-ball VFBGA and 44-pin TSOP Type II packages**

## Functional Description<sup>[1]</sup>

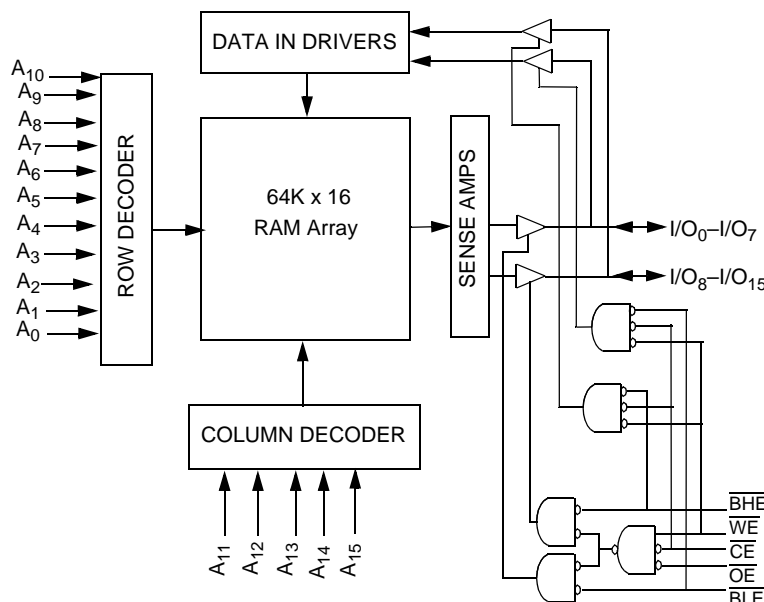
The CY62126DV30 is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features

advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{\text{CE}}$  HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{\text{CE}}$  HIGH), outputs are disabled ( $\overline{\text{OE}}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{\text{BHE}}$ , BLE HIGH) or during a write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

## Logic Block Diagram



### Note:

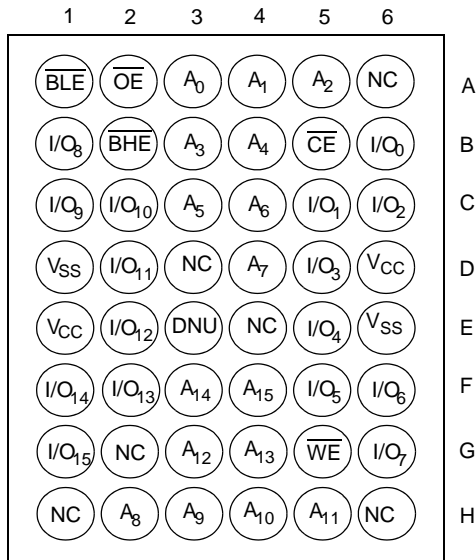
1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Product Portfolio**

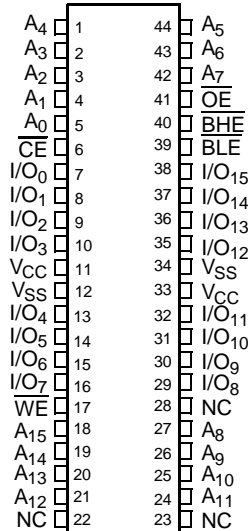
| Product       | Range      | V <sub>CC</sub> Range (V) |      |                      | Speed (ns) | Power Dissipation               |      |                     |      |                                |      |
|---------------|------------|---------------------------|------|----------------------|------------|---------------------------------|------|---------------------|------|--------------------------------|------|
|               |            |                           |      |                      |            | Operating, I <sub>CC</sub> (mA) |      |                     |      | Standby, I <sub>SB2</sub> (μA) |      |
|               |            | f = 1 MHz                 |      | f = f <sub>Max</sub> |            |                                 |      |                     |      |                                |      |
|               |            | Min.                      | Typ. | Max.                 |            | Typ. <sup>[2]</sup>             | Max. | Typ. <sup>[2]</sup> | Max. | Typ. <sup>[2]</sup>            | Max. |
| CY62126DV30L  | Automotive | 2.2                       | 3.0  | 3.6                  | 55         | 0.85                            | 1.5  | 5                   | 10   | 1.5                            | 15   |
| CY62126DV30LL | Industrial |                           |      |                      | 55         | 0.85                            | 1.5  | 5                   | 10   | 1.5                            | 4    |

**Pin Configurations<sup>[3, 4]</sup>**

**48-ball VFBGA  
Top View**



**TSOP II (Forward)  
Top View**



**Notes:**

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.
- NC pins are not connected to the die.
- E3 (DNU) can be left as NC or V<sub>SS</sub> to ensure proper operation. (Expansion Pins on FBGA Package: E4 - 2M, D3 - 4M, H1 - 8M, G2 - 16M, H6 - 32M).

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

|  |                                 |
|--|---------------------------------|
| Storage Temperature .....  | -65°C to +150°C                 |
| Ambient Temperature with Power Applied.....                        | -55°C to +125°C                 |
| Supply Voltage to Ground Potential .....                           | -0.3 to 3.9V                    |
| DC Voltage Applied to Outputs in High-Z State <sup>[6]</sup> ..... | -0.3V to V <sub>CC</sub> + 0.3V |

|  |  |
|--|--|
| DC Input Voltage <sup>[6]</sup> .....  | -0.3V to V <sub>CC</sub> + 0.3V        |
| Output Current into Outputs (LOW)..... | 20 mA                                  |
| Static Discharge Voltage.....          | > 2001V (per MIL-STD-883, Method 3015) |
| Latch-up Current .....                 | > 200 mA                               |

**Operating Range**

| Range      | Ambient Temperature (T <sub>A</sub> ) | V <sub>CC</sub> <sup>[7]</sup> |
|------------|---------------------------------------|--------------------------------|
| Industrial | -40°C to +85°C                        | 2.2V to 3.6V                   |
| Automotive | -40°C to +125°C                       | 2.2V to 3.6V                   |

**DC Electrical Characteristics (Over the Operating Range)**

| Parameter        | Description                                 | Test Conditions   |   | CY62126DV30-55 |                     |                       | Unit |    |
|------------------|---|---|---|----------------|---------------------|-----------------------|------|----|
|                  |   |   |   | Min.           | Typ. <sup>[5]</sup> | Max.                  |      |    |
| V <sub>OH</sub>  | Output HIGH Voltage                         | 2.2V ≤ V <sub>CC</sub> ≤ 2.7V   | I <sub>OH</sub> = -0.1 mA                                   | 2.0            |                     |                       | V    |    |
|                  |   | 2.7V ≤ V <sub>CC</sub> ≤ 3.6V   | I <sub>OH</sub> = -1.0 mA                                   | 2.4            |                     |                       |      |    |
| V <sub>OL</sub>  | Output LOW Voltage                          | 2.2V ≤ V <sub>CC</sub> ≤ 2.7V   | I <sub>OL</sub> = 0.1 mA                                    |                |                     | 0.4                   | V    |    |
|                  |   | 2.7V ≤ V <sub>CC</sub> ≤ 3.6V   | I <sub>OL</sub> = 2.1 mA                                    |                |                     | 0.4                   |      |    |
| V <sub>IH</sub>  | Input HIGH Voltage                          | 2.2V ≤ V <sub>CC</sub> ≤ 2.7V   |   | 1.8            |                     | V <sub>CC</sub> + 0.3 | V    |    |
|                  |   | 2.7V ≤ V <sub>CC</sub> ≤ 3.6V   |   | 2.2            |                     | V <sub>CC</sub> + 0.3 |      |    |
| V <sub>IL</sub>  | Input LOW Voltage                           | 2.2V ≤ V <sub>CC</sub> ≤ 2.7V   |   | -0.3           |                     | 0.6                   | V    |    |
|                  |   | 2.7V ≤ V <sub>CC</sub> ≤ 3.6V   |   | -0.3           |                     | 0.8                   |      |    |
| I <sub>IX</sub>  | Input Leakage Current                       | GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>  |   | Ind'l          | -1                  | +1                    | μA   |    |
|                  |   |   |   | Auto           | -4                  | +4                    |      |    |
| I <sub>OZ</sub>  | Output Leakage Current                      | GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled  |   | Ind'l          | -1                  | +1                    | μA   |    |
|                  |   |   |   | Auto           | -4                  | +4                    |      |    |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current    | f = f <sub>Max</sub> = 1/t <sub>RC</sub>  | V <sub>CC</sub> = 3.6V, I <sub>OUT</sub> = 0 mA, CMOS level |                | 5                   | 10                    | mA   |    |
|                  |   | f = 1 MHz   |   |                | 0.85                | 1.5                   |      |    |
| I <sub>SB1</sub> | Automatic CE Power-down Current—CMOS Inputs | $\overline{CE} \geq V_{CC} - 0.2V,$<br>$V_{IN} \geq V_{CC} - 0.2V,$<br>$V_{IN} \leq 0.2V,$<br>$f = f_{Max}$ (Address and Data Only),<br>$f = 0$ ( $\overline{OE}$ , $\overline{WE}$ , $\overline{BHE}$ and $\overline{BLE}$ ) | L   | Ind'l          |                     | 1.5                   | 5    | μA |
|                  |   |   |   | Auto           |                     | 1.5                   | 15   |    |
|                  |   |   | LL  |                |                     | 1.5                   | 4    |    |
| I <sub>SB2</sub> | Automatic CE Power-down Current—CMOS Inputs | $\overline{CE} \geq V_{CC} - 0.2V,$<br>$V_{IN} \geq V_{CC} - 0.2V$ or<br>$V_{IN} \leq 0.2V, f = 0, V_{CC} = 3.6V$   | L   | Ind'l          |                     | 1.5                   | 5    | μA |
|                  |   |   |   | Auto           |                     | 1.5                   | 15   |    |
|                  |   |   | LL  |                |                     | 1.5                   | 4    |    |

**Notes:**

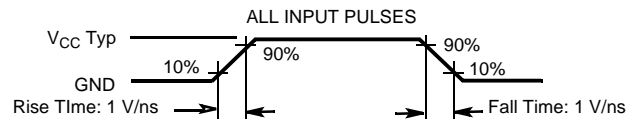
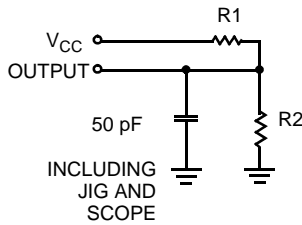
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.
- V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns., V<sub>IH(max.)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
- Full device operation requires linear ramp of V<sub>CC</sub> from 0V to V<sub>CC(min)</sub> & V<sub>CC</sub> must be stable at V<sub>CC(min)</sub> for 500 μs.

**Capacitance<sup>[8]</sup>**

| Parameter        | Description        | Test Conditions  | Max. | Unit |
|------------------|--------------------|--|------|------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub> | 8    | pF   |
| C <sub>OUT</sub> | Output Capacitance |  | 8    | pF   |

**Thermal Resistance<sup>[8]</sup>**

| Parameter       | Description                              | Test Conditions  | TSOP | VFBGA | Unit |
|-----------------|--|--|------|-------|------|
| Θ <sub>JA</sub> | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 x 4.5 inch, 2-layer printed circuit board | 55   | 76    | °C/W |
| Θ <sub>JC</sub> | Thermal Resistance (Junction to Case)    |  | 12   | 11    | °C/W |

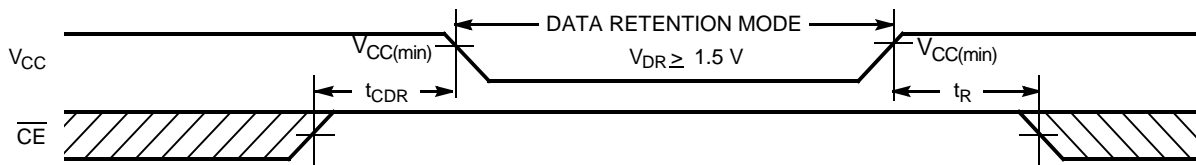
**AC Test Loads and Waveforms**


Equivalent to: THEVENIN EQUIVALENT

| Parameters      | 2.5V  | 3.0V | Unit  |
|-----------------|-------|------|-------|
| R <sub>1</sub>  | 16600 | 1103 | Ohms  |
| R <sub>2</sub>  | 15400 | 1554 | Ohms  |
| R <sub>TH</sub> | 8000  | 645  | Ohms  |
| V <sub>TH</sub> | 1.2   | 1.75 | Volts |

**Data Retention Characteristics**

| Parameter                       | Description                          | Conditions  | Min. | Typ <sup>[2]</sup> | Max. | Unit |
|---------------------------------|--------------------------------------|---|------|--------------------|------|------|
| V <sub>DR</sub>                 | V <sub>CC</sub> for Data Retention   |   | 1.5  |                    |      | V    |
| I <sub>CCDR</sub>               | Data Retention Current               | V <sub>CC</sub> =1.5V, $\overline{CE} \geq V_{CC} - 0.2V$ ,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V | L    | Ind'l              | 4    | μA   |
|                                 |                                      |   | L    | Auto               | 10   |      |
|                                 |                                      |   | LL   | Ind'l              | 3    |      |
| t <sub>CDR</sub> <sup>[8]</sup> | Chip Deselect to Data Retention Time |   | 0    |                    |      | ns   |
| t <sub>R</sub> <sup>[9]</sup>   | Operation Recovery Time              |   | 100  |                    |      | μs   |

**Data Retention Waveform**

**Notes:**

8. Tested initially and after any design or process changes that may affect these parameters.
9. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> >100 μs.

**Switching Characteristics (Over the Operating Range)<sup>[10]</sup>**

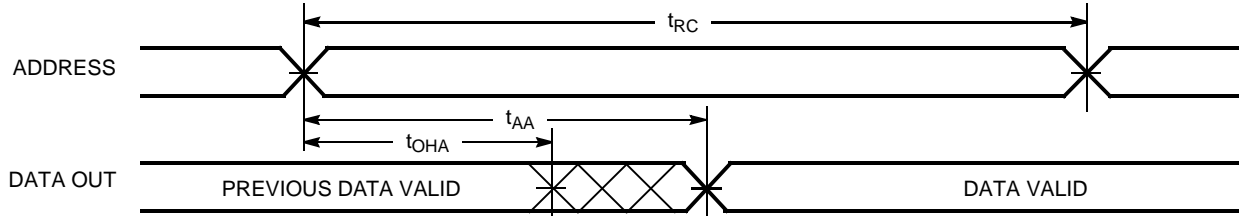
| Parameter                         | Description  | CY62126DV30-55 |      | Unit |
|-----------------------------------|--|----------------|------|------|
|                                   |  | Min.           | Max. |      |
| <b>Read Cycle</b>                 |  |                |      |      |
| $t_{RC}$                          | Read Cycle Time  | 55             |      | ns   |
| $t_{AA}$                          | Address to Data Valid  |                | 55   | ns   |
| $t_{OHA}$                         | Data Hold from Address Change                                      | 10             |      | ns   |
| $t_{ACE}$                         | $\overline{CE}$ LOW to Data Valid                                  |                | 55   | ns   |
| $t_{DOE}$                         | $\overline{OE}$ LOW to Data Valid                                  |                | 25   | ns   |
| $t_{LZOE}$                        | $\overline{OE}$ LOW to Low Z <sup>[11]</sup>                       | 5              |      | ns   |
| $t_{HZOE}$                        | $\overline{OE}$ HIGH to High Z <sup>[11, 12]</sup>                 |                | 20   | ns   |
| $t_{LZCE}$                        | $\overline{CE}$ LOW to Low Z <sup>[11]</sup>                       | 10             |      | ns   |
| $t_{HZCE}$                        | $\overline{CE}$ HIGH to High Z <sup>[11, 12]</sup>                 |                | 20   | ns   |
| $t_{PU}$                          | $\overline{CE}$ LOW to Power-up                                    | 0              |      | ns   |
| $t_{PD}$                          | $\overline{CE}$ HIGH to Power-down                                 |                | 55   | ns   |
| $t_{DBE}$                         | $\overline{BLE}/\overline{BHE}$ LOW to Data Valid                  |                | 25   | ns   |
| $t_{LZBE}$                        | $\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[11]</sup>       | 5              |      | ns   |
| $t_{HZBE}$                        | $\overline{BLE}/\overline{BHE}$ HIGH to High-Z <sup>[11, 12]</sup> |                | 20   | ns   |
| <b>Write Cycle<sup>[13]</sup></b> |  |                |      |      |
| $t_{WC}$                          | Write Cycle Time   | 55             |      | ns   |
| $t_{SCE}$                         | $\overline{CE}$ LOW to Write End                                   | 40             |      | ns   |
| $t_{AW}$                          | Address Set-up to Write End  | 40             |      | ns   |
| $t_{HA}$                          | Address Hold from Write End  | 0              |      | ns   |
| $t_{SA}$                          | Address Set-up to Write Start                                      | 0              |      | ns   |
| $t_{PWE}$                         | $\overline{WE}$ Pulse Width  | 40             |      | ns   |
| $t_{BW}$                          | $\overline{BLE}/\overline{BHE}$ LOW to Write End                   | 40             |      | ns   |
| $t_{SD}$                          | Data Set-up to Write End   | 25             |      | ns   |
| $t_{HD}$                          | Data Hold from Write End   | 0              |      | ns   |
| $t_{HZWE}$                        | $\overline{WE}$ LOW to High Z <sup>[11, 12]</sup>                  |                | 20   | ns   |
| $t_{LZWE}$                        | $\overline{WE}$ HIGH to Low Z <sup>[11]</sup>                      | 10             |      | ns   |

**Notes:**

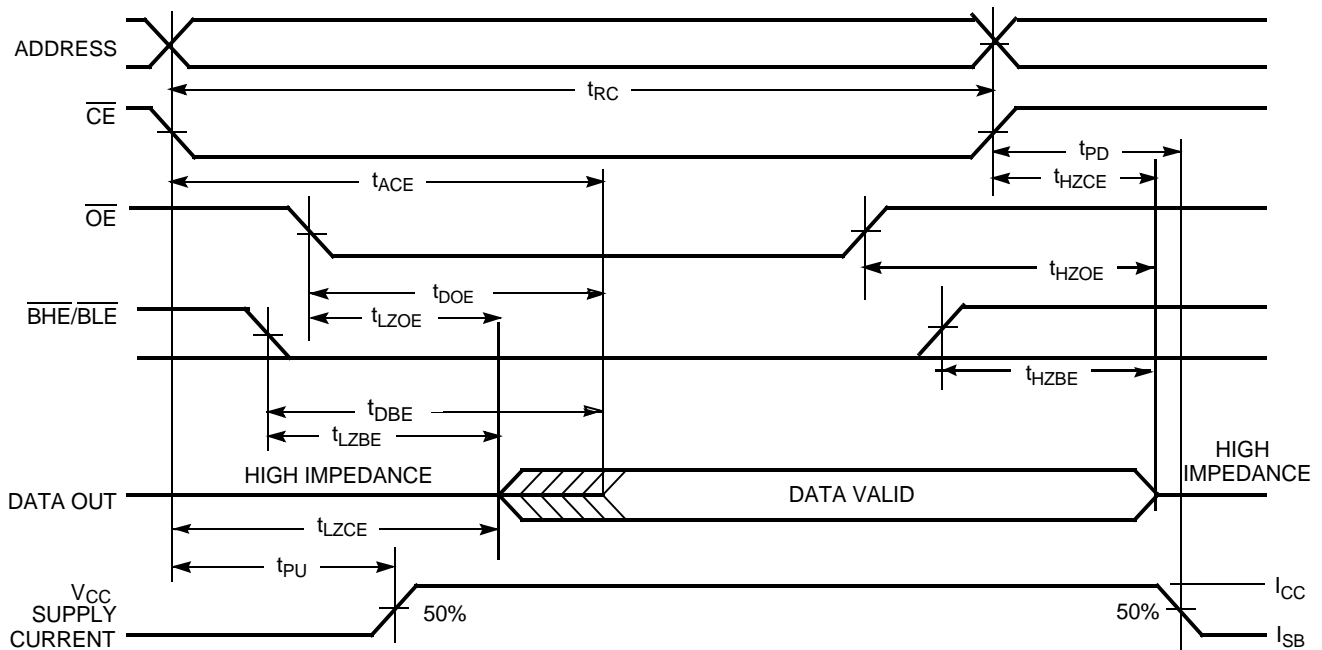
10. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}$ .
11. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ .
12.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
13. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

#### Read Cycle No. 1 (Address Transition Controlled)<sup>[14, 15]</sup>



#### Read Cycle No. 2 ( $\overline{OE}$ Controlled)<sup>[15, 16]</sup>

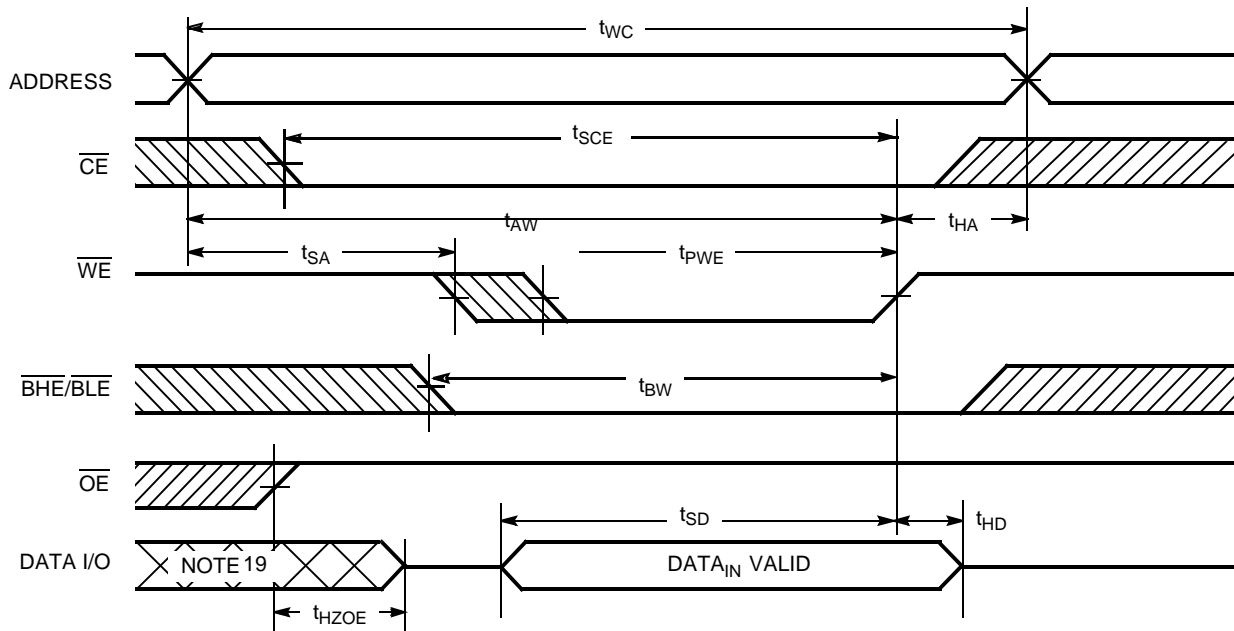


**Notes:**

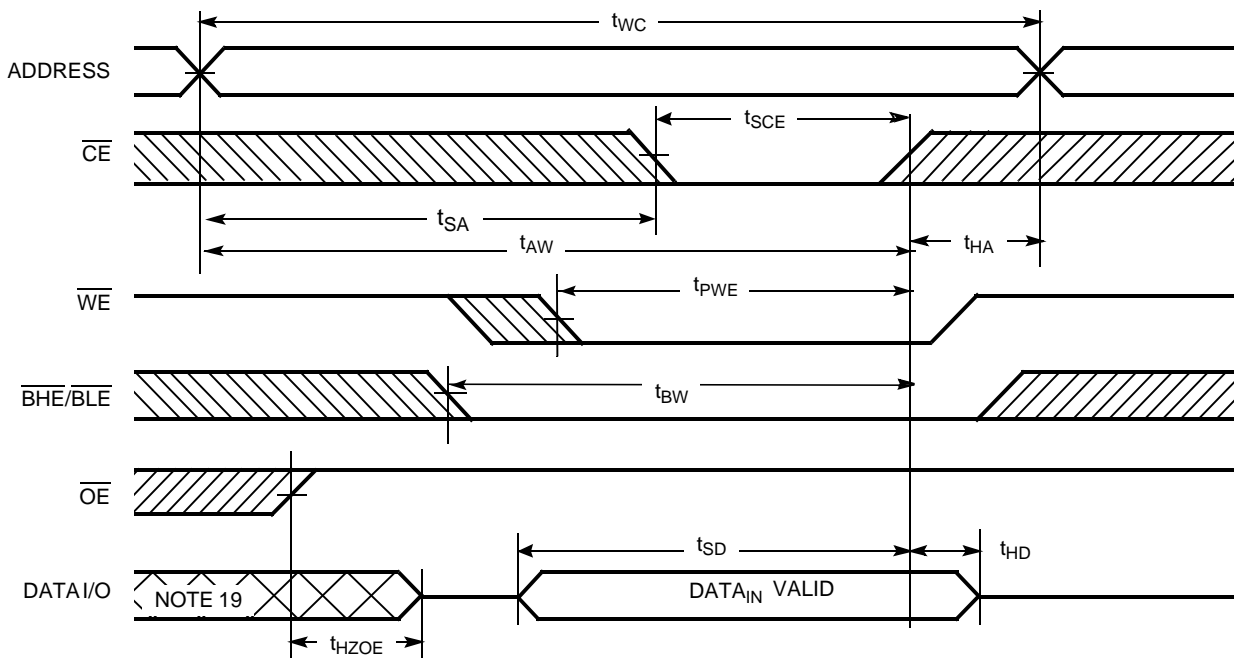
- 14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE} = V_{IL}$ .
- 15. WE is HIGH for Read cycle.
- 16. Address valid prior to or coincident with  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

Switching Waveforms(continued)

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[12, 13, 16, 17, 18]</sup>



Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[12, 13, 16, 17, 18]</sup>

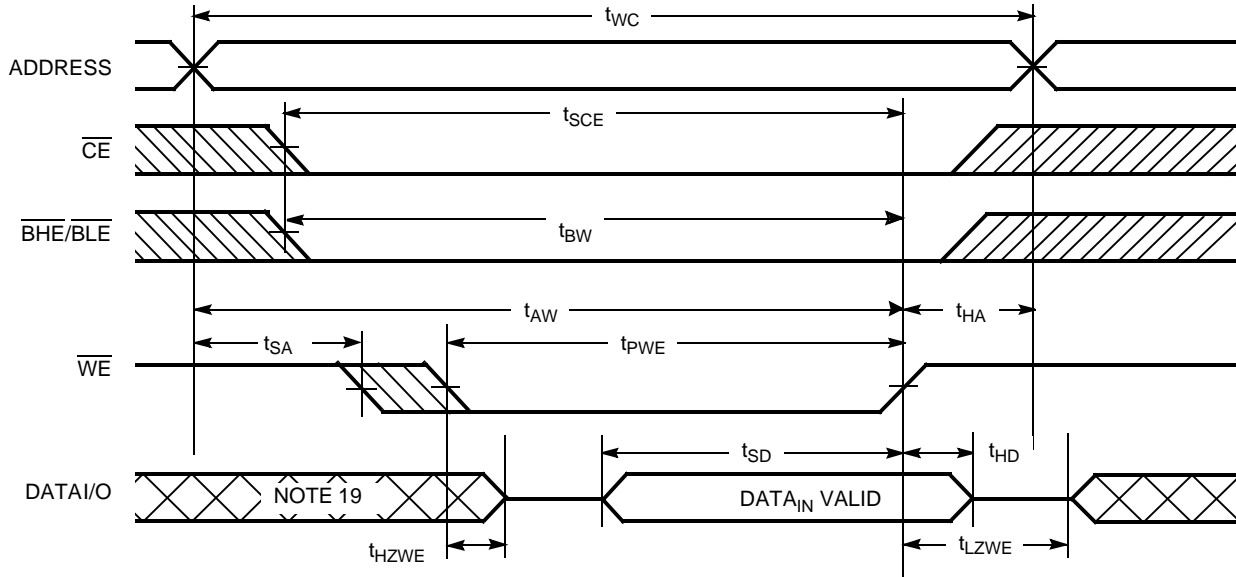


Notes:

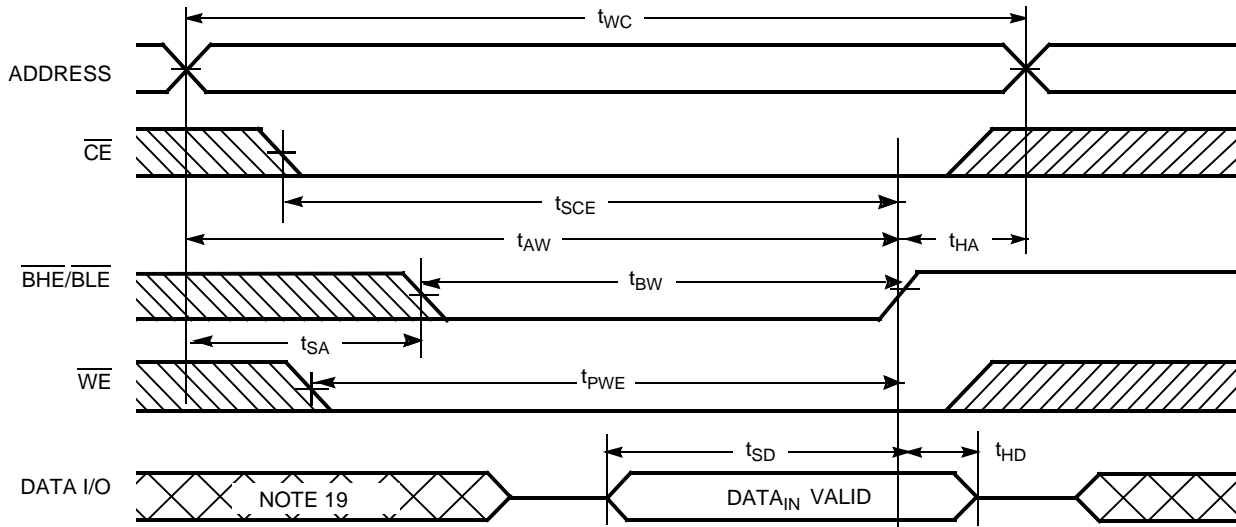
- 17. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
- 18. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
- 19. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms(continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[17, 18]</sup>



Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$ -controlled,  $\overline{OE}$  LOW)<sup>[17, 18]</sup>





**Truth Table**

| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | $\overline{\text{BHE}}$ | $\overline{\text{BLE}}$ | Inputs/Outputs   | Mode                | Power                       |
|------------------------|------------------------|------------------------|-------------------------|-------------------------|--|---------------------|-----------------------------|
| H                      | X                      | X                      | X                       | X                       | High Z   | Deselect/Power-Down | Standby ( $I_{\text{SB}}$ ) |
| L                      | X                      | X                      | H                       | H                       | High Z   | Output Disabled     | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | L                      | L                       | L                       | Data Out ( $I/O_0$ – $I/O_{15}$ )                                  | Read                | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | L                      | H                       | L                       | High Z ( $I/O_8$ – $I/O_{15}$ );<br>Data Out ( $I/O_0$ – $I/O_7$ ) | Read                | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | L                      | L                       | H                       | Data Out ( $I/O_8$ – $I/O_{15}$ );<br>High Z ( $I/O_0$ – $I/O_7$ ) | Read                | Active ( $I_{\text{CC}}$ )  |
| L                      | L                      | X                      | L                       | L                       | Data In ( $I/O_0$ – $I/O_{15}$ )                                   | Write               | Active ( $I_{\text{CC}}$ )  |
| L                      | L                      | X                      | H                       | L                       | High Z ( $I/O_8$ – $I/O_{15}$ );<br>Data In ( $I/O_0$ – $I/O_7$ )  | Write               | Active ( $I_{\text{CC}}$ )  |
| L                      | L                      | X                      | L                       | H                       | Data in ( $I/O_8$ – $I/O_{15}$ );<br>High Z ( $I/O_0$ – $I/O_7$ )  | Write               | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | H                      | L                       | L                       | High Z   | Output Disabled     | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | H                      | H                       | L                       | High Z   | Output Disabled     | Active ( $I_{\text{CC}}$ )  |
| L                      | H                      | H                      | L                       | H                       | High Z   | Output Disabled     | Active ( $I_{\text{CC}}$ )  |

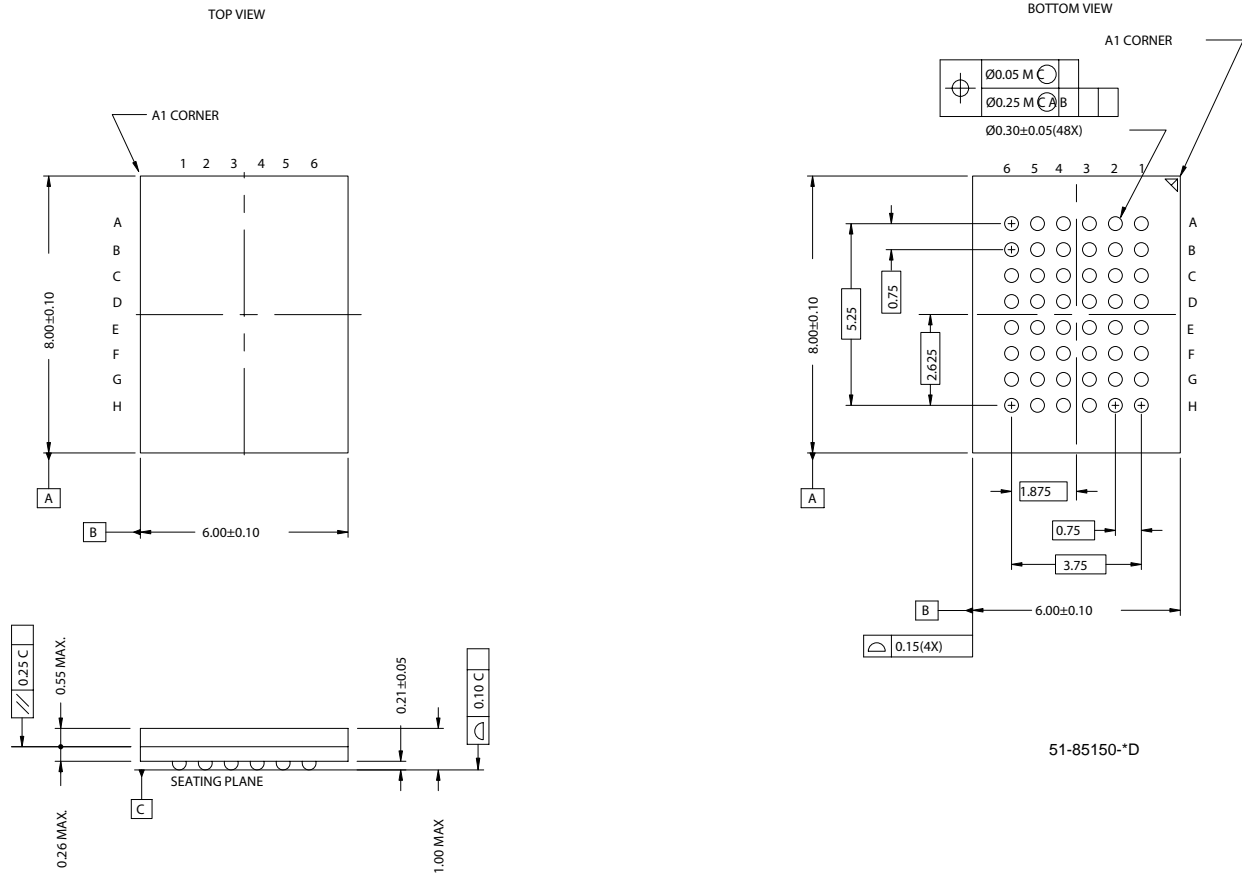
**Ordering Information**

| Speed (ns) | Ordering Code        | Package Diagram | Package Type  | Operating Range |
|------------|----------------------|-----------------|---|-----------------|
| 55         | CY62126DV30LL-55BVI  | 51-85150        | 48-ball Fine-Pitch Ball Grid Array (6 x 8 x 1 mm)           | Industrial      |
|            | CY62126DV30LL-55BVXI |                 | 48-ball Fine-Pitch Ball Grid Array (6 x 8 x 1 mm) (Pb-free) |                 |
|            | CY62126DV30LL-55ZI   | 51-85087        | 44-pin TSOP II  | Automotive      |
|            | CY62126DV30LL-55ZXI  |                 | 44-pin TSOP II (Pb-free)                                    |                 |
|            | CY62126DV30L-55BVXE  | 51-85150        | 48-ball Fine-Pitch Ball Grid Array (6 x 8 x 1 mm) (Pb-free) |                 |
|            | CY62126DV30L-55ZSXE  | 51-85087        | 44-pin TSOP II (Pb-free)                                    |                 |

Please contact your local Cypress sales representative for availability of these parts

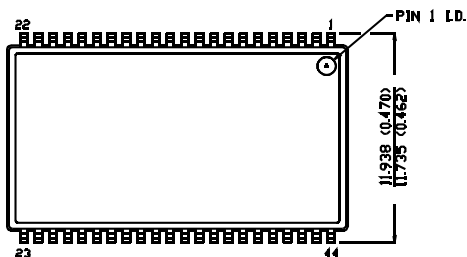
Package Diagrams

48-ball VFBGA (6 x 8 x 1 mm) (51-85150)

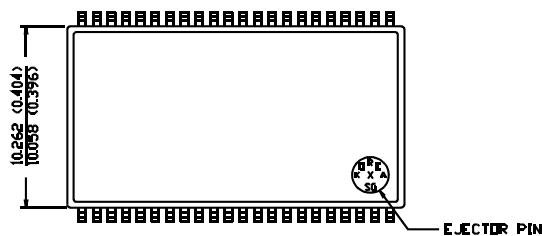


Package Diagrams(continued)

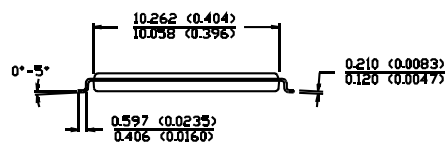
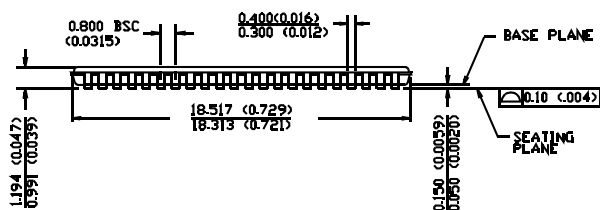
44-pin TSOP II (51-85087)



TOP VIEW



BOTTOM VIEW



51-85087-A

MoBL is a registered trademark, and MoBL2 and More Battery Life are trademarks of Cypress Semiconductor. All product and company names mentioned in this document are the trademarks of their respective holders.

**Document History Page**

| Document Title: CY62126DV30 MoBL® 1-Mbit (64K x 16) Static RAM |         |            |                 |  |
|--|---------|------------|-----------------|--|
| Document Number: 38-05230                                      |         |            |                 |  |
| REV.   | ECN NO. | Issue Date | Orig. of Change | Description of Change  |
| **   | 117689  | 08/27/02   | JUI             | New Data Sheet   |
| *A   | 127313  | 06/13/03   | MPR             | Changed From Advanced Status to Preliminary.<br>Changed I <sub>SB2</sub> to 5 $\mu$ A (L), 4 $\mu$ A (LL)<br>Changed I <sub>CCDR</sub> to 4 $\mu$ A (L), 3 $\mu$ A (LL)<br>Changed C <sub>IN</sub> from 6 pF to 8 pF   |
| *B   | 128340  | 07/22/03   | JUI             | Changed from Preliminary to Final<br>Add 70-ns speed, updated ordering information   |
| *C   | 129002  | 08/29/03   | CDY             | Changed I <sub>CC</sub> 1 MHz typ from 0.5 mA to 0.85 mA   |
| *D   | 238050  | See ECN    | AJU             | Fixed typo: Changed t <sub>DBE</sub> from 70 ns to 35 ns   |
| *E   | 316039  | See ECN    | PCI             | Added 45-ns Speed Bin in AC, DC and Ordering Information tables<br>Added Footnote #8 on page #4<br>Added Pb-free package ordering information on page # 9<br>Changed 44-pin TSOP-II package name from Z44 to ZS44  |
| *F   | 335861  | See ECN    | SYT             | Added Temperature Ranges in the Features Section on Page # 1<br>Added Automotive Product Information for CY62126DV30-L for 55 ns<br>Added I <sub>SB1</sub> and I <sub>SB2</sub> values for Automotive range of CY62126DV30-L for 55 ns<br>Added Automotive Information for I <sub>CCDR</sub> in the Data Retention Characteristics table<br>Added Pb-free packages in the ordering information<br>Changed 44-pin TSOP-II package name from ZS44 to Z44 |
| *G   | 357256  | See ECN    | PCI             | Added Pin Configuration and Package Diagram for 56-Lead QFN Package<br>Updated Thermal Characteristics and Ordering Information Table<br>Added Automotive Specs for I <sub>Ix</sub> and I <sub>Oz</sub> in the DC Electrical Characteristics table on Page# 4  |
| *H   | 486789  | See ECN    | VKN             | Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court"<br>Removed 45 ns and 70ns Speed bin from Product offering<br>Removed 56-pin QFN package<br>Updated Ordering Information Table   |