

# MoBL® 1 Mbit (128K x 8) Static RAM

### **Features**

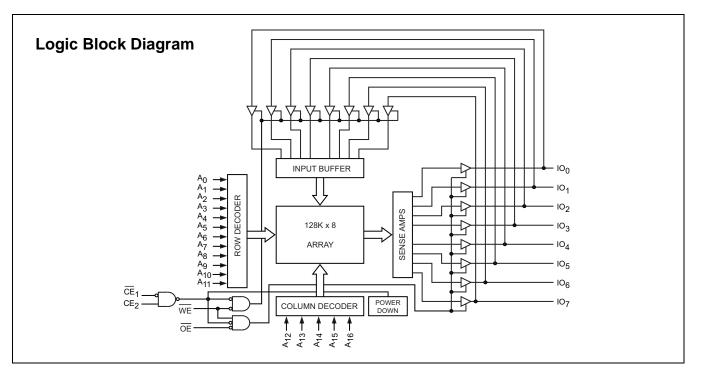
- Very high speed: 45 ns
  - Temperature ranges:
    - Industrial: –40°C to +85°C
    - Automotive-A: -40°C to +85°C
    - Automotive-E: –40°C to +125°C
- Wide voltage range: 2.20V 3.60V
- Pin compatible with CY62128DV30
- Ultra low standby power
   Typical standby current: 1 μA
   Maximum standby current: 4 μA
- Ultra low active power
   Typical active current: 1.3 mA @ f = 1 MHz
- Easy memory expansion with CE<sub>1</sub>, CE<sub>2</sub> and OE features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 32-pin SOIC, 32-pin TSOP I, and 32-pin STSOP packages

### **Functional Description**

The CY62128EV30<sup>[1]</sup> is a high performance CMOS static RAM module organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life<sup>TM</sup> (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (CE<sub>1</sub> HIGH or CE<sub>2</sub> LOW). The eight input and output pins (IO<sub>0</sub> through IO<sub>7</sub>) are placed in a high impedance state when the device is deselected (CE<sub>1</sub> HIGH or CE<sub>2</sub> LOW), the outputs are disabled (OE HIGH), or a write operation is in progress (CE<sub>1</sub> LOW and CE<sub>2</sub> HIGH and WE LOW).

To write to the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) and Write Enable (WE) inputs LOW. Data on the eight IO pins is then written into the location specified on the Address pin (A<sub>0</sub> through A<sub>16</sub>).

To read from the device, take Chip Enable ( $\overline{CE}_1$  LOW and  $CE_2$  <u>HIGH</u>) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the IO pins.



#### Note

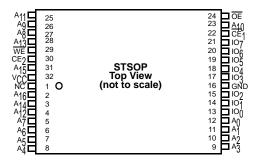
1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at http://www.cypress.com.

Cypress Semiconductor Corporation Document #: 38-05579 Rev. \*D 198 Champion Court

San Jose, CA 95134-1709 • 408-943-2600 Revised March 28, 2008



## Pin Configuration<sup>[2]</sup>



	Top View SOIC								
NC	10	32 🗌 V <sub>CC</sub>							
A <sub>16</sub>	2	31 🗌 A <sub>15</sub>							
A <sub>14</sub>	3	30 CE2							
A <sub>12</sub>	4	29 🗌 WE							
A7	5	<sup>28</sup> A <sub>13</sub>							
A <sub>6</sub>	6	27 🗖 A8							
A <sub>5</sub>	7	26 🛛 A <sub>9</sub>							
A <sub>4</sub>	8	25 🗖 A <sub>11</sub>							
A <sub>3</sub>	9	24 🗆 📊							
A <sub>2</sub>	10	23 🗖 A <sub>10</sub>							
A <sub>1</sub>	11	22 CE1							
A <sub>0</sub>	12	21 🗌 IO 7							
10 0	13	20 🗖 IO 6							
IO 1	14	19 🛛 IO 5							
IO 2	15	18 🛛 IO 4							
GND	16	17 🗆 IO <sub>3</sub>							

#### Table 1. Product Portfolio

								Power D	Dissipatio	on	
Product	Range			Speed (ns)	Speed Operating		g I <sub>CC</sub> (mA)		Standby Ι <sub>SB2</sub> (μΑ		
			, t		<b>x</b> - <b>y</b>	f = 1	MHz	f = f	max	Stanuby	ISB2 (µA)
		Min	<b>Typ</b> <sup>[3]</sup>	Max		<b>Typ</b> <sup>[3]</sup>	Max	<b>Typ</b> <sup>[3]</sup>	Max	<b>Typ</b> <sup>[3]</sup>	Max
CY62128EV30LL	Ind'l/Auto-A	2.2	3.0	3.6	45	1.3	2.0	11	16	1	4
CY62128EV30LL	Auto-E	2.2	3.0	3.6	55	1.3	4.0	11	35	1	30

A<sub>11</sub> A<sub>9</sub> A<sub>8</sub> A<sub>13</sub> WE CE<sub>2</sub> V<sub>CC</sub> CC A<sub>16</sub> A<sub>14</sub> A<sub>7</sub> A<sub>6</sub> A<sub>5</sub> A<sub>4</sub>

TSOP I Top View (not to scale)

#### Notes

2. NC pins are not connected on the die.

3. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25^{\circ}C$ .



### **Maximum Ratings**

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage to Ground Potential0	.3V to V <sub>CC(max)</sub> + 0.3V
DC Voltage Applied to Outputs in High-Z State <sup>[4, 5]</sup> 0	.3V to V <sub>CC(max)</sub> + 0.3V
DC Input Voltage <sup>[4,5]</sup> 0	

Output Current into Outputs (LOW)	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	> 2001V
Latch up Current	> 200 mA

## **Operating Range**

Device	Range	Ambient Temperature	<b>V<sub>CC</sub></b> <sup>[6]</sup>
CY62128EV30LL	Ind'l/Auto-A	-40°C to +85°C	2.2V to
	Auto-E	-40°C to +125°C	3.6V

## **Electrical Characteristics**

(Over the Operating Range)

Deremeter	Description	Test Conditions	45 ns	(Ind'l/A	uto-A)	55 ns (Auto-E)			Unit
Parameter	Description	Test Conditions	Min	<b>Typ</b> <sup>[3]</sup>	Max	Min	<b>Typ</b> <sup>[3]</sup>	Max	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	2.0			2.0			V
		$I_{OH} = -1.0 \text{ mA}, V_{CC} \ge 2.70 \text{ V}$	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA			0.4			0.4	V
		$I_{OL} = 2.1 \text{ mA}, V_{CC} \ge 2.70 \text{ V}$			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.2V to 2.7V	1.8		V <sub>CC</sub> + 0.3V	1.8		V <sub>CC</sub> + 0.3V	V
		V <sub>CC</sub> = 2.7V to 3.6V	2.2		V <sub>CC</sub> + 0.3V	2.2		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage	$V_{CC} = 2.2V$ to 2.7V	-0.3		0.6	-0.3		0.6	V
		V <sub>CC</sub> = 2.7V to 3.6V	-0.3		0.8	-0.3		0.8	V
I <sub>IX</sub>	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-4		+4	μΑ
I <sub>OZ</sub>	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	-4		+4	μΑ
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply	$f = f_{max} = 1/t_{RC}$ $V_{CC} = V_{CCmax}$		11	16		11	35	mA
	Current	f = 1 MHz I <sub>OUT</sub> = 0 mA CMOS levels		1.3	2.0		1.3	4.0	mA
I <sub>SB1</sub>	Automatic CE Power down Current — CMOS Inputs	$\label{eq:central_states} \begin{split} \overline{CE}_1 &\geq V_{CC} - 0.2V, \ CE_2 < 0.2V \\ V_{IN} &\geq V_{CC} - 0.2V, \ V_{IN} \leq 0.2V) \\ f &= f_{max} (Address and Data Only), \\ f &= 0 (OE and WE), \ V_{CC} = 3.60V \end{split}$		1	4		1	35	μΑ
I <sub>SB2</sub> <sup>[7]</sup>	Automatic CE Power down Current — CMOS Inputs	$\label{eq:cell} \begin{array}{l} \overline{CE}_1 \geq V_{CC} - 0.2V, \ CE_2 < 0.2V \\ V_{IN} \geq V_{CC} - 0.2V \ or \ V_{IN} < 0.2V, \\ f = 0, \ V_{CC} = 3.60V \end{array}$		1	4		1	30	μΑ

Notes

- 4.  $V_{IL(min)} = -2.0V$  for pulse durations less than 20 ns.

- 1.  $V_{IL(mn)} = V_{CC}+0.75V$  for pulse durations less than 20 ns. 5.  $V_{IL(max)} = V_{CC}+0.75V$  for pulse durations less than 20 ns. 6. Full device AC operation assumes a 100 µs ramp time from 0 to  $V_{CC}(min)$  and 200 µs wait time after  $V_{CC}$  stabilization. 7. Only chip enables ( $\overline{CE}_1$  and  $\overline{CE}_2$ ) must be at CMOS level to meet the  $I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.

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## Capacitance

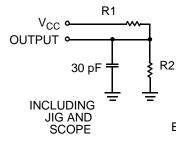
#### (For all packages)<sup>[8]</sup>

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	$T_A = 25^{\circ}C, f = 1 MHz,$	10	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC} = V_{CC(typ)}$	10	pF

### **Thermal Resistance**

Parameter	Description	Test Conditions	TSOP I	SOIC	STSOP	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	33.01	48.67	32.56	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		3.42	25.86	3.59	°C/W





ALL INPUT PULSES  $V_{CC}$ 90% 90% 10% .10% GND Rise Time = 1 V/ns-- Fall Time = 1 V/ns

1.75

THEVENIN EQUIVALENT Equivalent to:

 $\mathsf{R}_{\mathsf{TH}}$ 

۰V

**Parameters** 2.50V 3.0V Unit R1 16667 1103 Ω R2 15385 1554 Ω R<sub>TH</sub> 8000 645 Ω

1.20

OUTPUT-

## **Data Retention Characteristics**

 $V_{TH}$ 

(Over the Operating Range)

Parameter	Description	Conditions		Min	<b>Typ</b> <sup>[3]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5			V	
I <sub>CCDR</sub> <sup>[7]</sup>	Data Retention Current	$\frac{V_{CC}}{V_{CC}} = 1.5V,$	Ind'l/Auto-A			3	μΑ
	$ \begin{array}{l} \text{Data Retention Current} \\ \hline V_{CC} = 1.5 \text{V}, \\ CE_1 \geq \text{V}_{CC} - 0.2 \text{V or } CE_2 \leq 0.2 \text{V}, \\ \text{V}_{\text{IN}} \geq \text{V}_{CC} - 0.2 \text{V or } \text{V}_{\text{IN}} \leq 0.2 \text{V} \end{array} $		Auto-E			30	μΑ
t <sub>CDR</sub> <sup>[8]</sup>	Chip Deselect to Data Retention Time			0			ns
t <sub>R</sub> <sup>[9]</sup>	Operation Recovery Time			t <sub>RC</sub>			ns

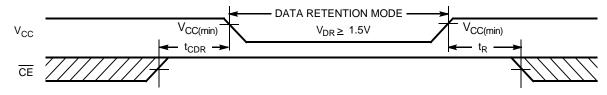
Note

Note
 Tested initially and after any design or process changes that may affect these parameters.
 Full device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

V



### Data Retention Waveform [10]



## Switching Characteristics

(Over the Operating Range)<sup>[10, 11]</sup>

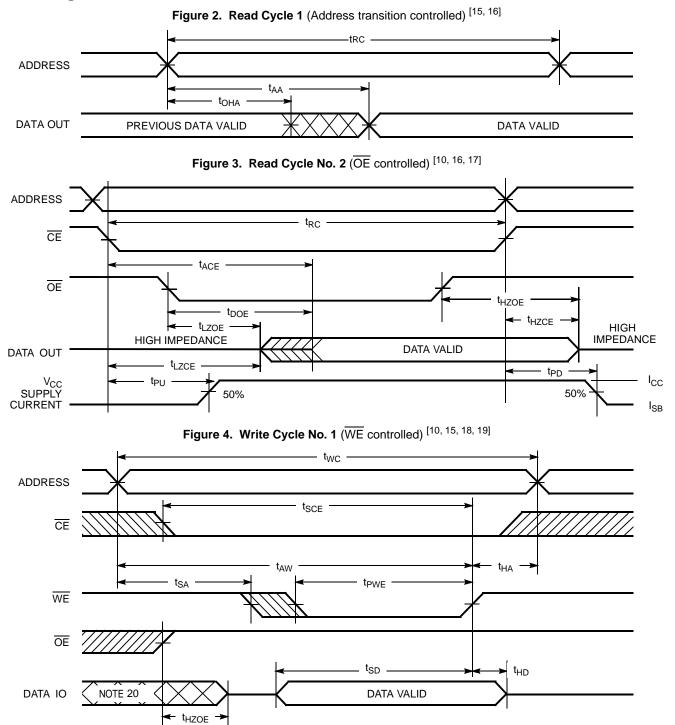
Demonster	Description	45 ns (Inc	d'l/Auto-A)	55 ns (	11	
Parameter	Description	Min	Max	Min	Max	Unit
Read Cycle	·					
t <sub>RC</sub>	Read Cycle Time	45		55		ns
t <sub>AA</sub>	Address to Data Valid		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	CE LOW to Data Valid		45		55	ns
t <sub>DOE</sub>	OE LOW to Data Valid		22		25	ns
t <sub>LZOE</sub>	OE LOW to Low Z <sup>[12]</sup>	5		5		ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[12,13]</sup>		18		20	ns
t <sub>LZCE</sub>	CE LOW to Low Z <sup>[12]</sup>	10		10		ns
t <sub>HZCE</sub>	CE HIGH to High Z <sup>[12, 13]</sup>		18		20	ns
t <sub>PU</sub>	CE LOW to Power Up	0		0		ns
t <sub>PD</sub>	CE HIGH to Power Up		45		55	ns
Write Cycle <sup>[14]</sup>	-		1			
t <sub>WC</sub>	Write Cycle Time	45		55		ns
t <sub>SCE</sub>	CE LOW to Write End	35		40		ns
t <sub>AW</sub>	Address Setup to Write End	35		40		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		ns
t <sub>PWE</sub>	WE Pulse Width	35		40		ns
t <sub>SD</sub>	Data Setup to Write End	25		25		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	WE LOW to High Z <sup>[12, 13]</sup>		18		20	ns
t <sub>LZWE</sub>	WE HIGH to Low Z <sup>[12]</sup>	10		10		ns

#### Notes

Notes
10. CE is the logical combination of CE<sub>1</sub> and CE<sub>2</sub>. When CE<sub>1</sub> is LOW and CE<sub>2</sub> is HIGH, CE is LOW; when CE<sub>1</sub> is HIGH or CE<sub>2</sub> is LOW, CE is HIGH.
11. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of V<sub>CC(typ)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> as shown in the "AC Test Loads and Waveforms" on page 4.
12. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZWE</sub> is less than t<sub>LZWE</sub> for any given device.
13. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> transitions are measured when the output enter a high impedance state.
14. The internal write time of the memory is defined by the overlap of WE, CE = V<sub>IL</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.



### Switching Waveforms



#### Notes

15. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ . 16. WE is HIGH for read cycle.

17. Address valid before or similar to CE1 transition LOW and CE2 transition HIGH.

18. Data IO is high impedance if  $\overline{OE} = V_{1H}$ . 19. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.

20. During this period, the IOs are in output state. Do not apply input signals.



### Switching Waveforms (continued)

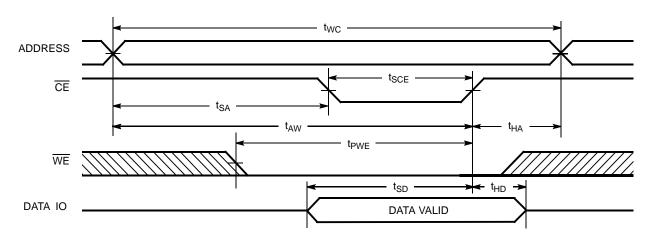
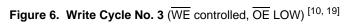
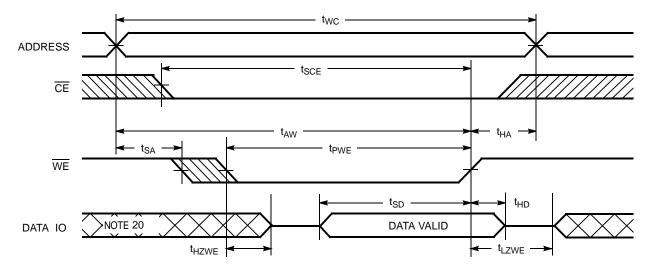


Figure 5. Write Cycle No. 2 (CE1 or CE2 controlled) [10, 14, 18, 19]





#### Table 2. Truth Table for CY62128EV30

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	Inputs/Outputs	Mode	Power
Н	Х	Х	Х	High Z	Deselect/Power Down	Standby (I <sub>SB</sub> )
Х	L	Х	Х	High Z	Deselect/Power Down	Standby (I <sub>SB</sub> )
L	Н	Н	L	Data Out	Read	Active (I <sub>CC</sub> )
L	Н	Н	Н	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	Н	L	Х	Data in	Write	Active (I <sub>CC</sub> )

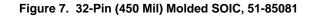


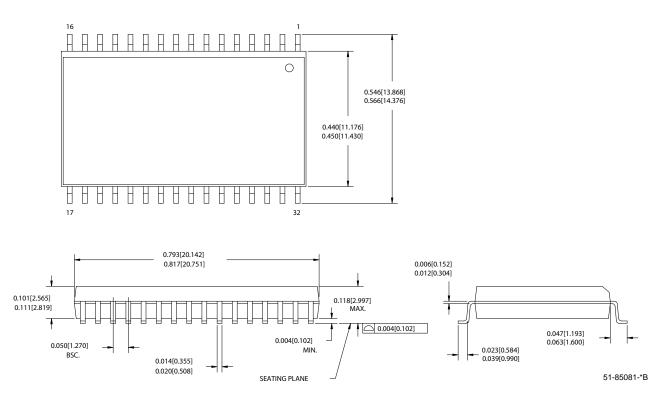
### **Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62128EV30LL-45SXI	51-85081	32-pin 450-Mil SOIC (Pb-free)	Industrial
	CY62128EV30LL-45ZXI	51-85056	32-pin TSOP Type I (Pb-free)	
	CY62128EV30LL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	
45	CY62128EV30LL-45ZXA	51-85056	32-pin TSOP Type I (Pb-free)	Automotive-A
55	CY62128EV30LL-55ZXE	51-85056	32-pin TSOP Type I (Pb-free)	Automotive-E

Contact your local Cypress sales representative for availability of these parts.

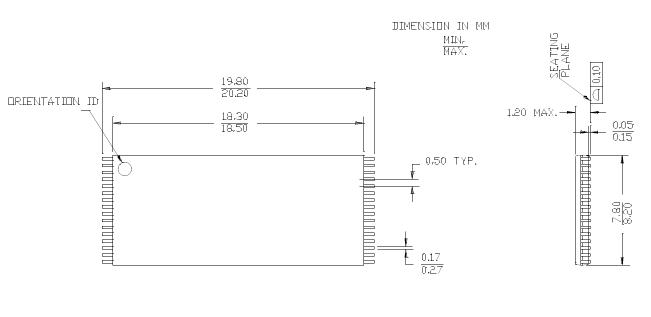
### **Package Diagrams**



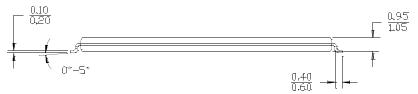




## Package Diagrams (continued)



#### Figure 8. 32-Pin Thin Small Outline Package Type I (8 x 20 mm), 51-85056

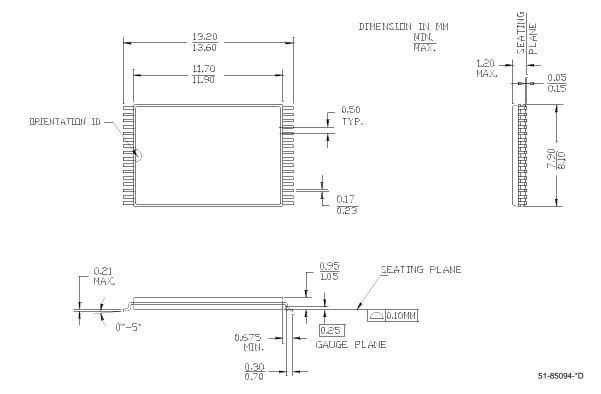


51-85056-\*D



## Package Diagrams (continued)







### **Document History Page**

Document Title: CY62128EV30 MoBL® 1 Mbit (128K x 8) Static RAM Document Number: 38-05579				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	285473	See ECN	PCI	New Data Sheet
*A	461631	See ECN	NXR	Converted from Preliminary to Final Removed 35 ns Speed Bin Removed "L" version of CY62128EV30 Removed Reverse TSOP I package from Product offering. Changed I <sub>CC (Typ)</sub> from 8 mA to 11 mA and I <sub>CC (Max)</sub> from 12 mA to 16 mA for f = f <sub>max</sub> Changed I <sub>CC (max)</sub> from 1.5 mA to 2.0 mA for f = 1 MHz Changed I <sub>SB2 (max)</sub> from 1 $\mu$ A to 4 $\mu$ A Changed I <sub>SB2 (max)</sub> from 0.5 $\mu$ A to 1 $\mu$ A Changed I <sub>CDR (max)</sub> from 1 $\mu$ A to 3 $\mu$ A Changed the AC Test load Capacitance value from 50 pF to 30 pF Changed t <sub>LZCE</sub> from 3 to 5 ns Changed t <sub>LZCE</sub> from 6 to 10 ns Changed t <sub>PWE</sub> from 30 to 35 ns Changed t <sub>LZWE</sub> from 6 to 10 ns Changed t <sub>LZWE</sub> from 6 to 10 ns Updated the Ordering Information table.
*В	464721	See ECN	NXR	Updated the Block Diagram on page # 1
*C	1024520	See ECN	VKN	Added final Automotive-A and Automotive-E information Added footnote #9 related to I <sub>SB2</sub> and I <sub>CCDR</sub> Updated Ordering Information table
*D	2257446	See ECN	NXR	Changed the Maximum rating of Ambient Temperature with Power Applied from $55^{\circ}$ C to $+125^{\circ}$ C to $-55^{\circ}$ C to $+125^{\circ}$ C.

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