IS42G32256

256K x 32 x 2 (16-Mbit) SYNCHRONOUS GRAPHICS RAM

ADVANCE INFORMATION
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FEATURES

- 256,144 words x 32 bits x 2-bank organization
- All inputs are sampled at the positive going edge of the system clock
- Dual internal bank control
- Single 3.3V ± 3V power supply
- Programmable mode register
  – Burst length (1, 2, 4, 8, and full page)
  – CAS latency (2 and 3)
  – Burst type: Sequential and Interleave
- Burst Read single-bit Write Operation
- Refresh capability
  – Auto, self-refresh
- 2,048 refresh cycles/32 ms
- LVTTL compatible inputs and outputs
- 100-pin PQFP
  (14mm x 20mm)

GRAPHIC FEATURES

- SMRS cycle
  – Load mask register
  – Load color register
- Write per bit (old mask)
- Block write (eight columns)

DESCRIPTION

The ISSI IS42G32256 is a high-speed 16-Mbit CMOS Synchronous Graphics RAM organized as 256K words x 32 bits x 2 banks. With SGRAM, all input and output signals are synchronized with the rising edge of the system clock. Programmable Mode Register and Special Registers provide a choice of Read or Write burst lengths of 1, 2, 4, or 8 locations or a Full Page with burst termination options. The SGRAM performance is enhanced with the Write-per-bit (WPB) and eight columns of Block Write functions.

The IS42G32256 is ideal for high-performance, high-bandwidth applications including workstation graphics, set top box, games, and PC-2D/3D graphic applications.

Table 1. Key Timing Parameters

Symbol	Parameter	-7	-8	-10	Units
t_{CK}	Clock Cycle Time	7	8	10	ns
	Access Time @ CL = 3	6	6.5	7	ns
	Operating Frequency	143	125	100	MHz

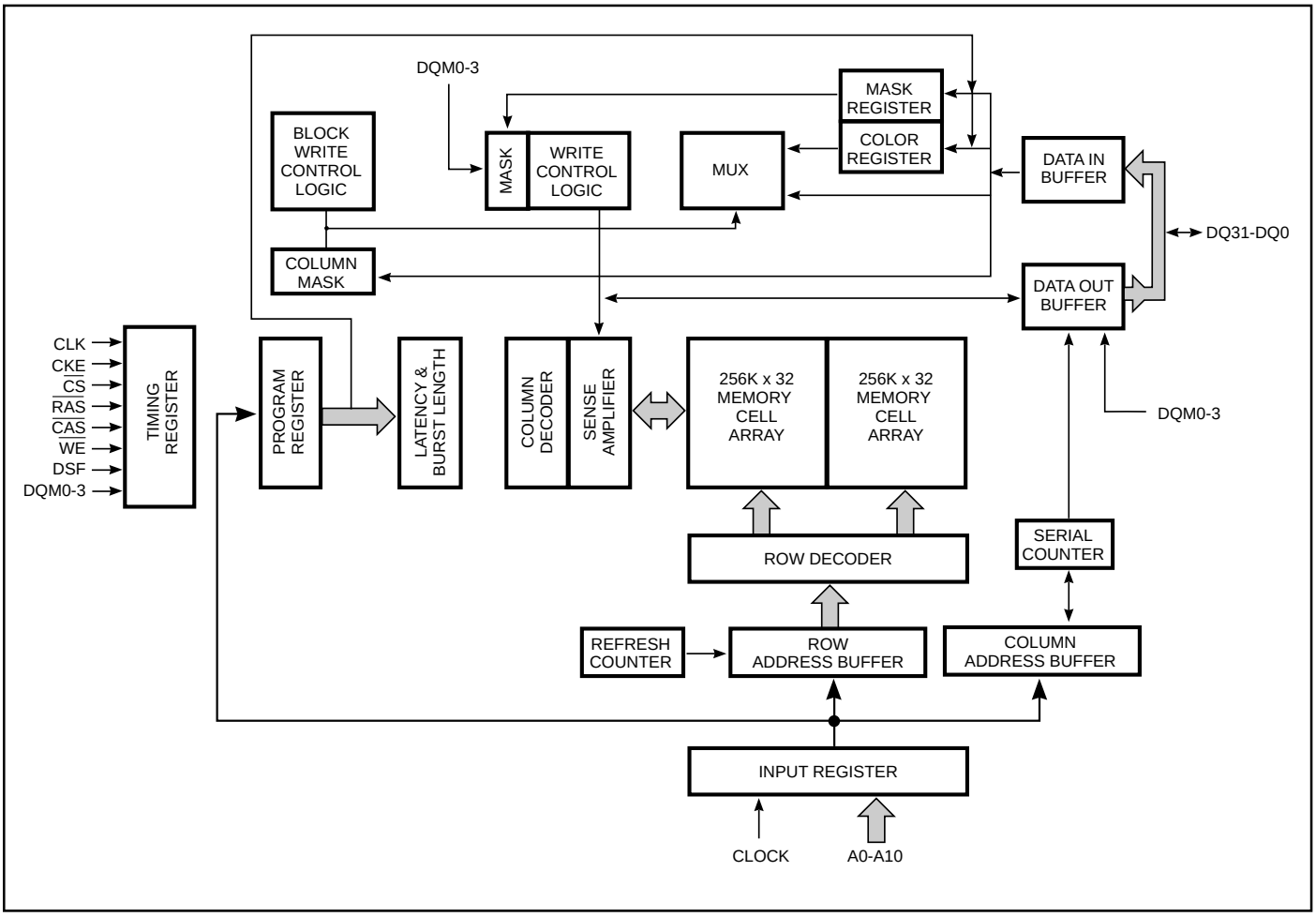


Figure 1. IS42G32256 Functional Block Diagram

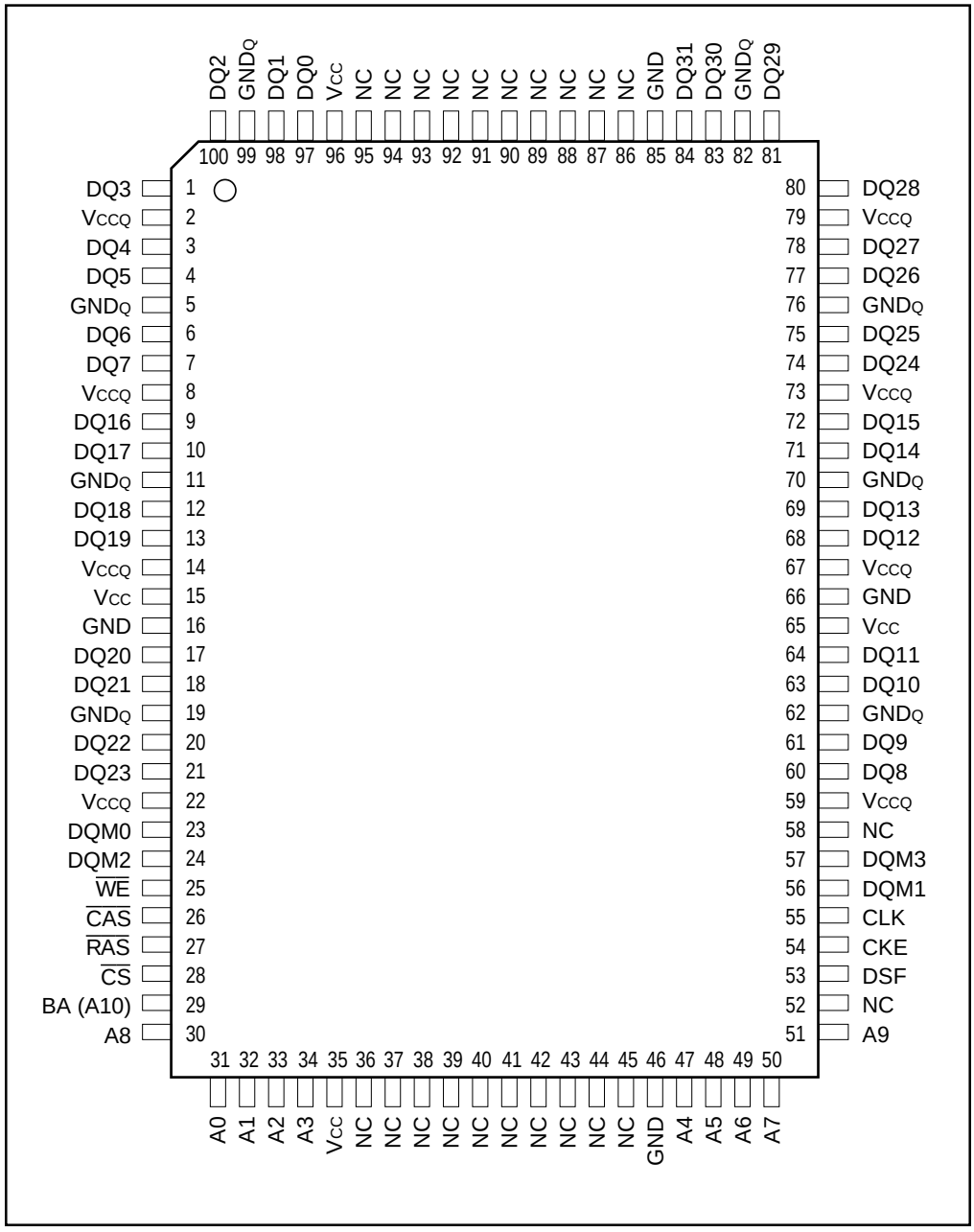


Figure 2. IS42G32256 Pin Configuration, 100-pin PQFP

Table 2. Pin Descriptions

Symbol	Pin Number	I/O	Name and Function
A0-A9	30-34, 47-51	I	**Address:** Row/Column addresses are multiplexed on the same pins. Row address: RA0-RA9 Column address: CA0-CA7
A10/BP	29	I	**Bank Select Address:** Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{CAS}$	26	I	**Column Address Strobe:** Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
CKE	54	I	**Clock Enable:** Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock + t_{CKS} prior to new command. Disable input buffers for power down in standby.
CLK	55	I	**System Clock:** Active on the positive going edge to sample all inputs.
$\overline{CS}$	28	I	**Chip Select:** Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM_X.
DQ0-DQ31	1, 3-4, 6-7, 9-10, 12-13, 17-18, 20-21, 60-61, 63-64, 68-69, 71-72, 74-75, 77-78, 81-81, 83-84, 97-98, 100	I/O	**Data Input/Output:** Data Inputs/Outputs are multiplexed on the same pins.
DQM0-DQM3	23-24, 56-57	I/O	**Data Input/Output Mask:** Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte Masking)
DSF	53		**Define Special Function:** Enables write per bit, block write and special mode register set.
$\overline{RAS}$	27	I	**Row Address Strobe:** Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access and precharge.
$\overline{WE}$	25	I	**Write Enable:** Enables write operation and row precharge.
V_{CCQ}	2, 8, 14, 22, 59, 67, 73, 76, 79		Supplies voltage for data output
Vcc	15, 35, 65, 96		Power Supply Voltage
GND_Q	5, 11, 19, 62, 70, 82, 99		Ground for D_Q
GND	16, 46, 66, 85		Ground
NC	36-45, 52, 58, 86-95		No connect

Table 3. Frequency vs. AC Parameter Relationships

IS42G32256: 7 ns (Unit: number of clocks)

Frequency	$\overline{CAS}$ Latency	t_{RC} 63 ns	t_{RAS} 42 ns	t_{RP} 21 ns	t_{RRD} 14 ns	t_{RCD} 20 ns	t_{CCD} 7 ns	t_{CDL} 7 ns	t_{RDL} 7 ns
143 MHz (7 ns)	3	9	6	3	2	3	1	1	1
125 MHz (8 ns)	3	8	6	3	2	3	1	1	1
100 MHz (10 ns)	2	7	5	3	2	2	1	1	1
83 MHz (12 ns)	2	6	4	2	2	2	1	1	1
75 MHz (13.4 ns)	2	5	4	2	2	2	1	1	1
66 MHz (15 ns)	2	5	3	2	1	2	1	1	1

IS42G32256: 8 ns (Unit: number of clocks)

Frequency	$\overline{CAS}$ Latency	t_{RC} 70 ns	t_{RAS} 48 ns	t_{RP} 24 ns	t_{RRD} 16 ns	t_{RCD} 20 ns	t_{CCD} 8 ns	t_{CDL} 8 ns	t_{RDL} 8 ns
125 MHz (8 ns)	3	9	6	3	2	3	1	1	1
100 MHz (10 ns)	3	8	5	3	2	2	1	1	1
83 MHz (12 ns)	2	6	4	2	2	2	1	1	1
75 MHz (13.4 ns)	2	6	4	2	2	2	1	1	1
66 MHz (15 ns)	2	5	4	2	2	2	1	1	1
50 MHz (20 ns)	2	4	3	2	1	1	1	1	1

IS42G32256: 10 ns (Unit: number of clocks)

Frequency	$\overline{CAS}$ Latency	t_{RC} 80 ns	t_{RAS} 50 ns	t_{RP} 26 ns	t_{RRD} 20 ns	t_{RCD} 20 ns	t_{CCD} 10 ns	t_{CDL} 10 ns	t_{RDL} 10 ns
100 MHz (10 ns)	3	8	5	3	2	2	2	1	1
83 MHz (12 ns)	3	7	5	3	2	2	2	1	1
71 MHz (14 ns)	2	6	4	2	2	2	2	1	1
66 MHz (15 ns)	2	6	4	2	2	2	2	1	1
50 MHz (20 ns)	2	4	3	2	1	1	1	1	1
40 MHz (25 ns)	2	4	2	2	1	1	1	1	1

Table 4. Truth Table

Function	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	DQM	A10	A9	A8-A0
Mode Register Set[2,3]	H	X	L	L	L	L	L	X	OP CODE		
Special Mode Register Set[2,3,8]	H	X	L	L	L	L	H	X	OP CODE		
Auto Refresh[4]	H	H	L	L	L	H	L	X	X	X	X
Self Refresh, Entry[4]	H	L	L	L	L	H	L	X	X	X	X
Self Refresh, Exit[4]	L	H	L	H	H	H	X	X	X	X	X
	L	H	H	X	X	X	X	X	X	X	X
Bank Active/Row Address Write Per Bit Disable[5,6]	H	X	L	L	H	H	L	X	V		Row Address
Bank Active/Row Address Write Per Bit Enable[5,6,10]	H	X	L	L	H	H	H	X	V		Row Address
Read and Column Address Auto Precharge Disable[5]	H	X	L	H	L	H	L	X	V	L	Column Address
Read and Column Address Auto Precharge Enable[5,6]	H	X	L	H	L	H	L	X	V	H	Column Address
Write and Column Address Auto Precharge Disable[5,6]	H	X	L	H	L	L	L	X	V	L	Column Address
Write and Column Address Auto Precharge Enable[5,6,7,10]	H	X	L	H	L	L	L	X	V	H	Column Address
Block Write and Column Address Auto Precharge Disable[5,6]	H	X	L	H	L	L	H	X	V	L	Column Address
Block Write and Column Address Auto Precharge Enable[5,6,7,10]	H	X	L	H	L	L	H	X	V	H	Column Address
Burst Stop[8]	H	X	L	H	H	L	L	X	X	X	X
Precharge Bank Selection	H	X	L	L	H	L	L	X	V	L	X
Precharge Both Banks	H	X	L	L	H	L	L	X	X	H	X
Clock Suspend or	H	L	L	H	H	H	X	X	X	X	X
Active Power Down Entry	H	L	H	X	X	X	X	X	X	X	X
Clock Suspend or Active Power Down Exit	L	H	X	X	X	X	X	X	X	X	X
Precharge Pover Down Mode Entry	H	L	L	H	H	H	X	X	X	X	X
	H	L	H	X	X	X	X	X	X	X	X
Precharge Pover Down Mode Exit	L	H	L	V	V	V	V	X	X	X	X
	L	H	H	X	X	X	X	X	X	X	X
DQM[9]	H	X	X	X	X	X	X	V	X	X	X
No Operation Command	H	X	L	H	H	H	X	X	X	X	X
	H	X	H	X	X	X	X	X	X	X	X

Notes:

1. V = Valid, X = Don't Care, H = Logic High, L = Logic Low
2. OP Code: Operand Code; A0-A10: Program keys (@MRS); A5, A6: LMR or LCR select. (@SMRS) Color register exists only one per DQi which both banks share. So does Mask Register. Color or mask is loaded into chip through DQ pin.
3. MRS can be issued only at both banks precharge state. SMRS can be issued only if DQs are idle. A new command can be issued at the next clock of MRS/SMRS.
4. Auto refresh functions as same as CBR refresh of DRAM. The automatical precharge without row precharge command is meant by "Auto". Auto/Self refresh can be issued only at both precharge state.
5. A10: bank select address. If "Low" at read, (block) write, row active and precharge, bank A is selected. If "High" at read, (block) write, row active and precharge, bank B is selected. If A9 is "High" at row precharge, A10 is ignored and both banks are precharged.
6. It is determined at row active cycle whether normal/block write operates in write per bit mode or not. For A bank write, at A bank row active, for B bank write, at B bank row active. Terminology: Write per bit = I/O mask. (Block) Write with write per bit mode = masked (block) write.
7. During burst read or write with auto precharge, new read/(block) write command cannot be issued. Another bank read/(block) write command can be issued at t_{RP} after the end of burst.
8. Burst stop command is valid only at full page burst length.
9. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (write DQM latency is 0) but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2.)
10. Graphic features added to SDRAMs original features. If SDF is tied to low, graphic functions are disabled and chip operates as a 16M SDRAM with 32 DQs.

Table 5. SGRAM vs SDRAM

SDRAM Function	MRS		Bank Active		Write	
DSF	L	H	L	H	L	H
SGRAM Function	MRS	SMRS	Bank Active with Write per bit Disable	Bank Active with Write per bit Enable	Normal Write	Block Write

Notes:
1. If DSF is low, SGRAM functionality is identical to SDRAM functionality.
2. SGRAM can be used as a unified memory by the appropriate DSF control; SGRAM = Graphic Memory + Main Memory.

Table 6. Mode Register Field Table to Program Modes

Register Programmed with MRS

Address	A10	A9	A8, A7	A6, A5, A4	A3	A2, A1, A0
Function	RFU(1)	W.B.L.(2)	TM	CAS Latency	BT	Burst Length

Test Mode			CAS Latency				Burst Type					Burst Length	
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	Reserved
0	1	Vendor	0	0	1	—	1	Interleave	0	0	1	2	Reserved
1	0	Use	0	1	0	2			0	1	0	4	4
1	1	Only	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	256(Full)(3)	Reserved

Special mode Register Programmed with SMRS

Address	A10, A9, A8, A7	A6	A5	A4, A3, A2, A1, A0
Function	X	LC(4)	LM(4)	X

Load Color		Load Mask	
A6	Function	A5	Function
0	Disable	0	Disable
1	Enable	1	Enable

Notes:
1. RFU (Reserved for Future Use) should stay “0” during MRS cycle.
2. If A9 is high during MRS cycle, “Burst Read Single Bit Write” function will be enabled.
3. The full column burst (256-bit) is available only at Sequential mode of burst type.
4. If LC and LM both high (1), data of mask and color register will be unknown.

POWER UP SEQUENCE

1. Apply power and start clock, attempt to maintain DKE = “H” and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200 µs.
3. Issue precharge commands for all banks of the devices.
4. Issue two or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Sequence of 4 and 5 may be changed.

The device is now ready for normal operation.

Table 7. Burst Sequence (Burst Length = 4)

Initial Address A1	A0	Sequential				Interleave			
0	0	0	1	2	3	0	1	2	3
0	I	1	2	3	0	1	0	3	2
I	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

Table 8. Burst Sequence (Burst Length = 8)

Initial Address A2	A1	A0	Sequential								Interleave							
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

Table 10. Pixel to DQ Mapping (at Block Write)

Column Address			3 Byte	2 Byte	1 Byte	0 Byte
A2	A1	A0	I/O31-I/O24	I/O23-I/O16	I/O15-I/O8	I/O7-I/O0
0	0	0	DQ24	DQ 16	DQ8	DQ0
0	0	1	DQ25	DQ 17	DQ9	DQ1
0	1	0	DQ26	DQ18	DQ10	DQ2
0	1	1	DQ27	DQ19	DQ11	DQ3
1	0	0	DQ28	DQ20	DQ12	DQ4
1	0	1	DQ29	DQ21	DQ13	DQ5
1	1	0	DQ30	DQ22	DQ14	DQ6
1	1	1	DQ31	DQ23	DQ 15	DQ7

DEVICE OPERATIONS

Clock (CLK)

The clock input is used as the reference for all SGRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of setup and hold time around positive edge of the clock for proper functionality and Icc specifications.

Clock Enable (CKE)

The clock enable (CKE) gates the clock onto SGRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When both banks are in the idle state and CKE goes low synchronously with clock, the SGRAM enters the power down mode from the next clock cycle. The SGRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "t_{SS}+ICLOCK" before the high going edge of the clock, then the SGRAM becomes active from the same clock edge accepting all the input commands.

Bank Select (A10)

This SGRAM is organized as two independent banks of 262,144 words x 32 bits memory arrays. The A10 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. When A10 is asserted low, bank A is selected. When A10 is latched high, bank B is selected. The banks select Al0 is latched at bank activate, read, write, mode register set and precharge operations.

Address Inputs (A0-A9)

The 18 address bits are required to decode the 262,144 word locations are multiplexed into ten address input pins (A0-A9). The 10-bit row address is latched along with $\overline{RAS}$ and A10 during bank activate command. The 8-bit column address is latched along with $\overline{CAS}$, $\overline{WE}$ and A10 during read or with command.

NOP and Device Deselect

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, The SGRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF and all the address inputs are ignored.

Power-up

The following sequence is recommended for Power-up:

1. Power must be applied to either CKE and DQM inputs to pull them high and other pins are NOP condition at the condition at the inputs before or along with V_{DD} (and V_{DDQ}) supply.

   The clock signal must also be asserted at the same time.

2. After V_{DD} reaches the desired voltage, a minimum pause of 200 microseconds is required with inputs in NOP condition.
3. Both banks must be precharged now.
4. Perform a minimum of two auto refresh cycles to stabilize the internal circuitry.
5. Perform a Mode Register Set cycle to program the $\overline{CAS}$ latency, burst length and burst type as the default value of mode register is undefined.

At the end of one clock cycle from the mode register set cycle, the device is ready for operation.

When the above sequence is used for Power-up, all the outputs will be in high-impedance state. The high-impedance of outputs is not guaranteed in any other power-up sequence.

Note: Sequence of 4 and 5 may be changed.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of SGRAM. It programs the $\overline{CAS}$ latency, burst type, addressing, burst length, test mode and various vendor specific options to make SGRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SGRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and DSF (The SGRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0-A9 and A10 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and DSF going low is the data written in the mode register. One clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as both banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length field uses A0-A2, burst type

uses A3, CAS latency (read latency from column address) A4-A6, A7-A8 and A10 are uses for vendor specific options or test mode use. And the write burst length is programmed using A9. A7-A8 and A10 must be set to low for normal SGRAM operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.

Bank Activate

The bank activate command is used to select a random row in an idle bank. By asserting low on RAS and CS with desired row and bank addresses, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD} (min) from the time of bank activation. t_{RCD} (min) is the internal timing parameter of SGRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD} (min) with cycle time of the clock and then rounding of the result to the next higher integer. The SGRAM has two internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of both banks immediately. Also the noise generated during sensing of each bank of SGRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. t_{RRD} (min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS} (min). Every SGRAM bank activate command must satisfy t_{RAS} (min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS} (max). The number of cycles for both t_{RAS} (min) and t_{RAS} (max) can be calculated similar to t_{RCD} specification.

Burst Read

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on CS and RAS with WE being high on the positive edge of the clock. The bank must be active for at least t_{RCD} (min) before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid for all burst length.

Burst Write

The burst write command is similar to burst read command, and is used to write data into the SGRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on CS, CAS and WE with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing may not have been completed yet. The writing can not complete burst length. The burst write can be terminated by issuing a burst read and DQM for blocking data inputs or burst write in the same or the other active bank.

The write burst can also be terminated by using DQM for blocking data and precharging the bank "t_{RDL}" after the last data input to be written into the active row. See DQM Operation also.

DQM Operation

The DQM is used mask input and output operations. It works similar to OE during operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SGRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is required. DQM is also used for device selection and bus control in a memory system. DQM0 controls DQ0 to DQ7, DQM1 controls DQ8 to DQ15, DQM2 controls DQ16 to DQ23, DQM3 controls DQ24 to DQ31. DQM masks the DQs by a byte regardless that the corresponding DQs are in a state of WPB masking or Pixel masking. Please refer to DQM timing diagram also.

Precharge

The precharge is performed on an active bank by asserting low on CS, RAS, WE and A9 with valid A10 of the bank to be precharged. The precharge command can be asserted anytime after t_{RAS} (min) is satisfy from the bank activate command in the desired bank. "t_{RP}" is defined as the minimum time required to precharge a bank.

The minimum number of clock cycles required to complete row precharge is calculated by dividing "tRP" with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by tRAS (max). Therefore, each bank has to be precharged within tRAS (max) from the bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again.

Entry to Power Down, Auto refresh, Self refresh and Mode register Set etc. is possible only when both banks are in idle state.

Auto Precharge

The precharge operation can also be performed by using auto precharge. The SGRAM internally generates the timing to satisfy tRAS (min) and "tRP" for the programmed burst length and $\overline{CAS}$ latency. The auto precharge command is issued at the same time as burst write by asserting high on A9. If burst read or burst write command is issued with low on A9, the bank is left active until a new command is asserted. Once auto precharge command is given, no new command are possible to that particular bank until the bank achieves idle state.

Both Banks Precharge

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ with high on A9 after all banks have satisfied tRAS (min) requirement, performs precharge on both banks. At the end of tRP after performing precharge all, all banks are in idle state.

Auto Refresh

The storage cells of SGRAM need to be refreshed every 32 ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by tRC (min). The minimum number of clock cycles required can be calculated by driving tRC with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOPs until the auto refresh operation is completed. Both banks will be in the idle state at the end of auto refresh operation. The auto refresh is the preferred refresh mode when the SGRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6 µs or the burst of 2048 auto refresh cycles in 32 ms.

Self Refresh

The self refresh is another refresh mode available in the SGRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SGRAM. In self refresh mode, the SGRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption.

The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the refresh.

The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of tRC before the SGRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 2048 auto refresh cycles immediately after exiting self refresh.

Define Special Function (DSF)

The DSF controls the graphic applications of SGRAM. If DSF is tied to low, SGRAM functions as 256K x 32 x 2 Bank SGRAM. SGRAM can be used as an unified memory by the appropriate DSF command. All the graphic function mode can be entered only by setting DSF high when issuing commands which otherwise would be normal SGRAM commands.

SGRAM functions such as $\overline{RAS}$ Active, Write and WCBR change to SGRAM functions such as $\overline{RAS}$ Active with WPB, Block Write and SWCBR respectively that DSF controls.

Special Mode Register Set (SMRS)

There are two kinds of special mode registers in SGRAM. One is color register and the other is mask register. Those usage will be explained at "Write Per Bit" and "Block Write" session. When A5 and DSF goes high in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low, load color register is filled with color data for associated DQ's through the DQ pins. If both A5 and A6 are high at SMRS, data of mask and color cycle is required to complete the write in the mask register and the color register at LMR and LCR respectively. The next color of LMR and LCR, a new commands can be

issued. SMRS, compared with MRS, can be issued at the active state under the condition that DQs are idle. As in write operation, SMRS accepts the data needed through DQ pins. Therefore it should be attended not to induce bus contention. The more detailed materials can be obtained by referring corresponding timing diagram.

Write Per Bit

Write per bit (i.e., I/O mask mode) for SGRAM is a function that selectively masks bits of data being written to the devices. The mask is stored in an internal register and applied to each bit of data written when enable. Bank active command with DSF=High enable write per bit for the associated bank. The mask used for write per bit operations is stored in the mask register accessed by SWCBR (Special Mode Register Set Command). When a mask bit=0, the associated data bit is unaltered when a write command is executed and the write per bit has been enable for the bank being written. No additional timing conditions. Write per bit writes can be either masking is the same for write per bit and non-WPB write.

Block Write

Block write is a feature allowing the simultaneous writing of consecutive eight columns of data within a RAM device during a single access cycle. During block write the data to be written comes from the internal “color” register and DQ I/O pins are used for independent column selection. The block of column to be written is aligned on 8-column boundaries and is defined by the column address with the three LSBs ignored. Write command with DSF=1 enable block write for the associated bank. The block width is eight columns where column =“n” bits for by “n” part. The color register is the same width as the data port of the chip. It is width via a SWCBR where data present on the DQ pins is to be coupled into the internal color register. The color register provides the data masked by the DQ column select, WPB mask (if enable), and DQM byte mask. Column data masking (Pixel masking) is provided on an individual column basis for each byte of data. The column mask is driven on the DQ pins during a block write command. The DQ column mask function is segmented on a per bit basis (i.e., DQ[0:7] provided the column mask for data bits [0:7], DQ[8:15] provided the column mask for data bits [8:15], DQ0 masks column [0] for data bits [0:7], DQ9 masks column [1] for data bits [8:15], etc.). Block writes are always non-burst independent of the burst length that has been programmed into to the mode register. If write per bit was enabled by the bank active command with DSF=1, then write per bit masking of the color register data is enabled.

If write per bit was disabled by a bank active command with DSF=0, the write per bit masking of the color register data is disabled. DQM masking provides independent data byte masking during normal write operations, except that the control is extended to the consecutive eight columns of the block write.

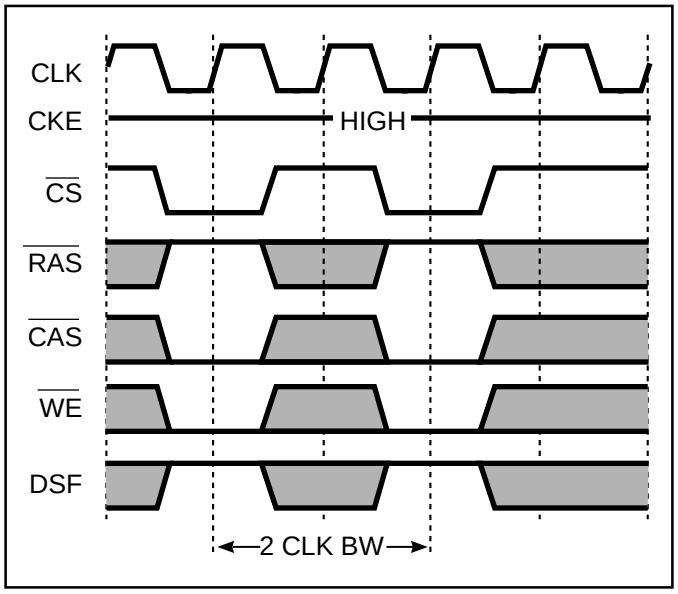
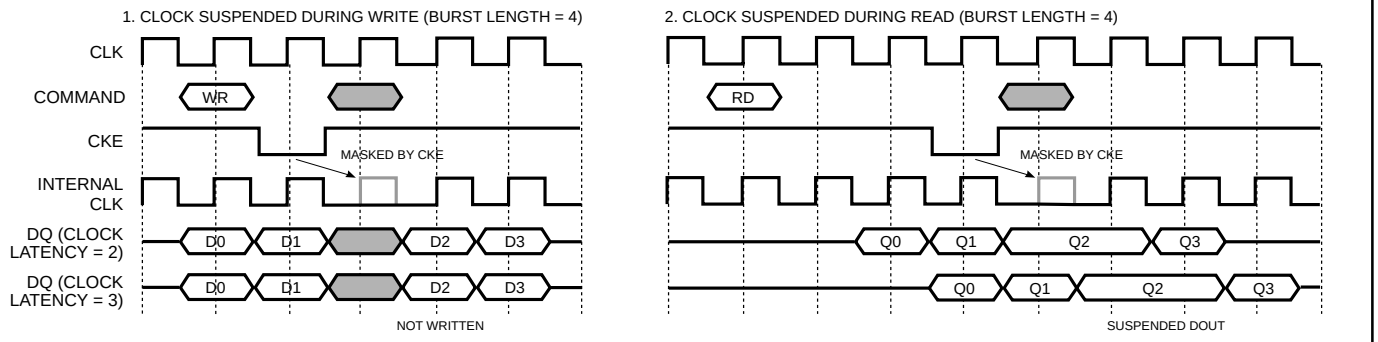


Figure 3. Timing Diagram to Illustrate t_{BWC}. (2CLK Clcle Block Write)

Table 11. Summary of SGRAM Basic Features and Benefits

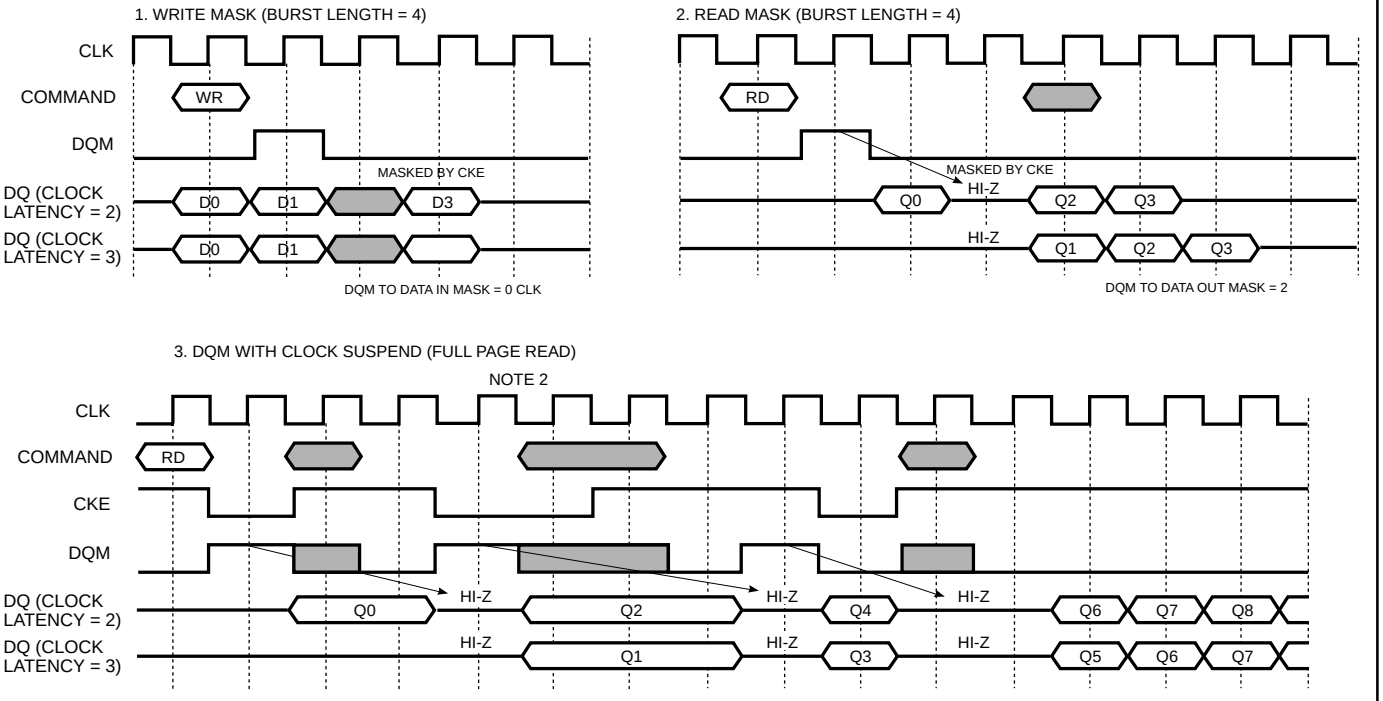
Features	256K x 32 x 2 SGRAM	Benefits
Interface	Synchronous	Better interaction between memory and system without wait-state of asynchronous DRAM. High speed vertical and horizontal drawing. High operation frequency allows performance gain for SCROLL, FILL, and BitBLT.
Bank	2 each	Pseudo-infinite row length by on-chip interleaving operation. Hidden row activation precharge.
Page Depth /1 Row	256 bit	High-speed vertical and horizontal drawing.
Total Page Depth	2048 bytes	High speed vertical and horizontal drawing.
Burst Length (Read)	1, 2, 4, 8 Full Page	Programmable burst of 1, 2, 4, 8 and full page transfer per column address.
Burst Length (Write)	1 2 4 8 Full Page	Programmable burst of 1, 2, 4, 8 and full page transfer per column address.
	BRSW	Switch to burst length of 1 at write without MRS.
Burst Type	Sequential & Interleave	Compatible with Intel and Motorola CPU based system.
CAS Latency	2, 3	Programmable CAS latency.
Block Write	8-Column	High speed FILL, CLEAR, Text with color registers. Maximum 32-byte data transfer (e.g., for 8bpp: 32 pixels) with plane and byte masking functions.
Color Register	1 each	A and B bank share.
Mask Register	1 each	Write-per-bit capability (bit plane masking). A and B bank share.
	DQM0-3	Byte masking (pixel masking for 8bpp system) for data-out/in.
Mask function	Write per bit	Each bit of the mask register directly controls a corresponding bit plane.
	Pixel Mask at Block Write	Byte masking (pixel masking for 8bpp system) for color DQi.

BASIC FEATURES AND FUNCTION DESCRIPTION



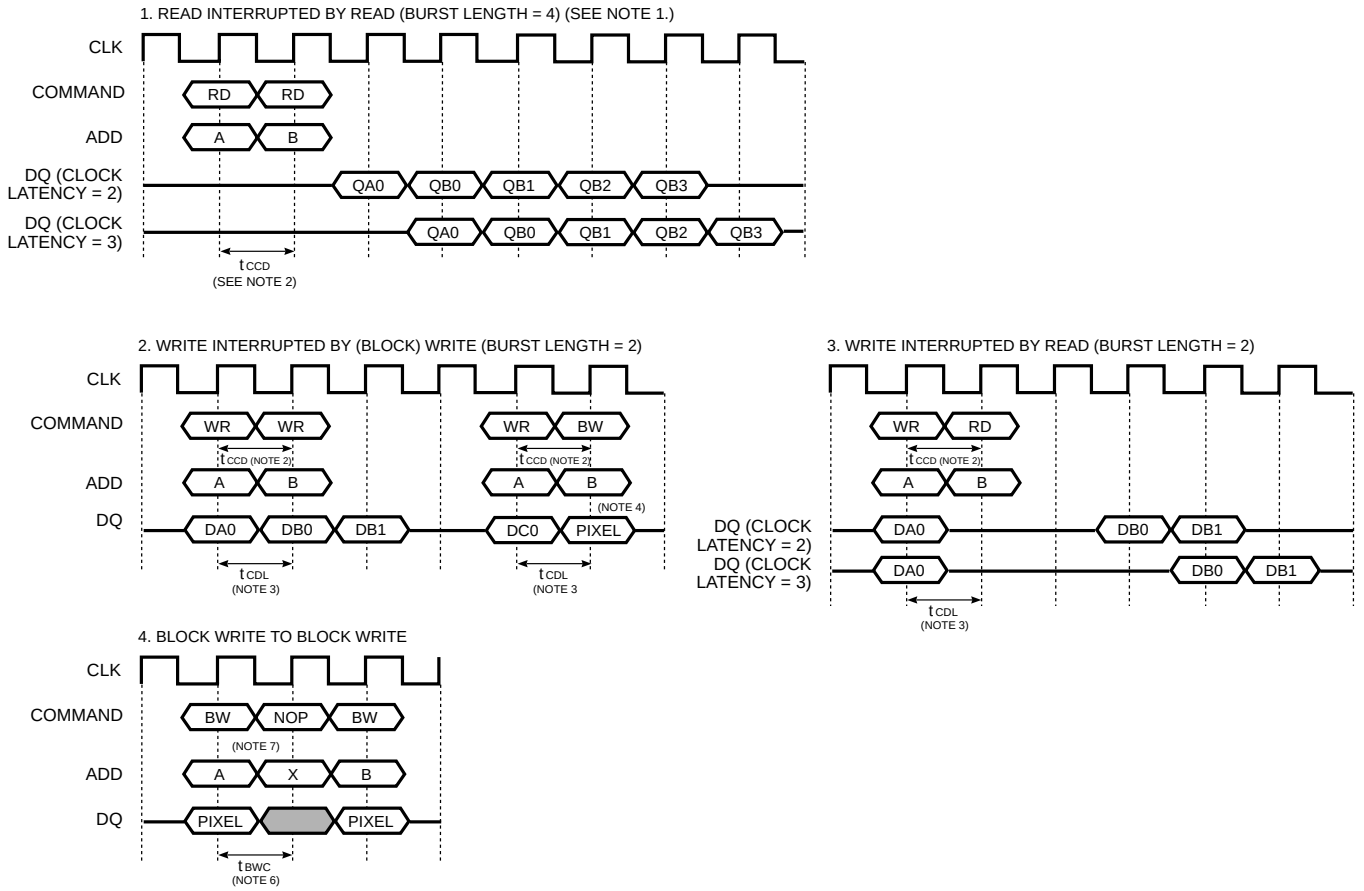
Note:
1. CKE to CLK disable/enable = 1 clock.

Figure 4. Clock Suspend



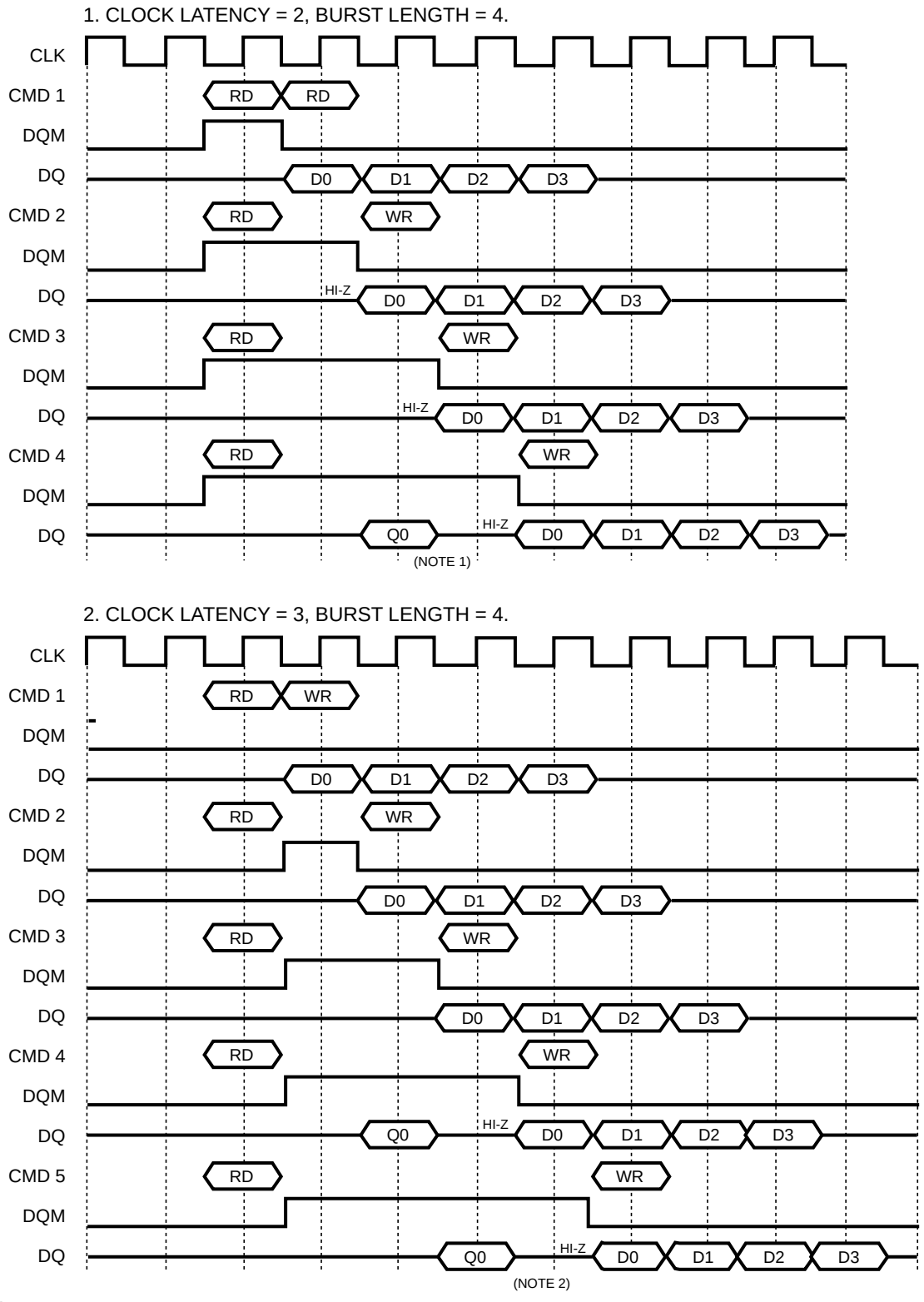
Notes:
1. There are four DQMi (i = 0-3).
   Each DQMi masks eight DQs. (One Byte, one Pixel for 8bpp.)
2. DQM masks data out Hi-Z after two clocks which should be masked by CKE "L".

Figure 5. DQM Operation



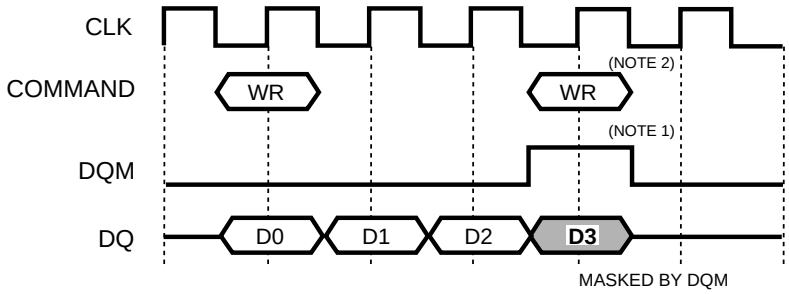
Notes:
1. By "Interrpt", it is possible to stop burst read/write by external before the end of burst.
   By "$\overline{\text{CAS}}$ Interrupt", to stop burst read/write by $\overline{\text{CAS}}$ access; read, write, and block write.
2. t_{CCD}: $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay (=1CLK).
3. t_{CDL}: Last data in to new column address delay (=1CLK).
4. Pixel: Pixel mask.
5. t_{CC}: Clock cycle time.
6. t_{BWC}: Block write minimum cycle time.
7. Other bank can be active or precharge.

Figure 6. $\overline{\text{CAS}}$ Interrupt (I)



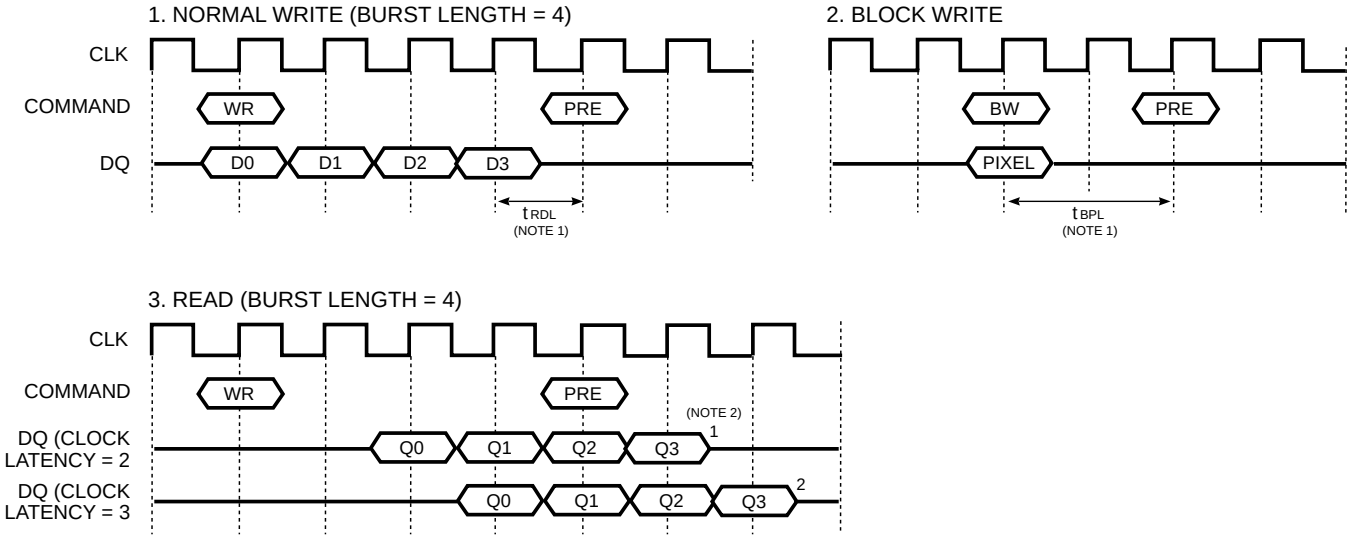
Notes:
1. To prevent bus contention, there should be at least one gap between data in and data out.
2. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.

Figure 7. $\overline{\text{CAS}}$ Interrupt (II): Read Interrupted by Write and DQM



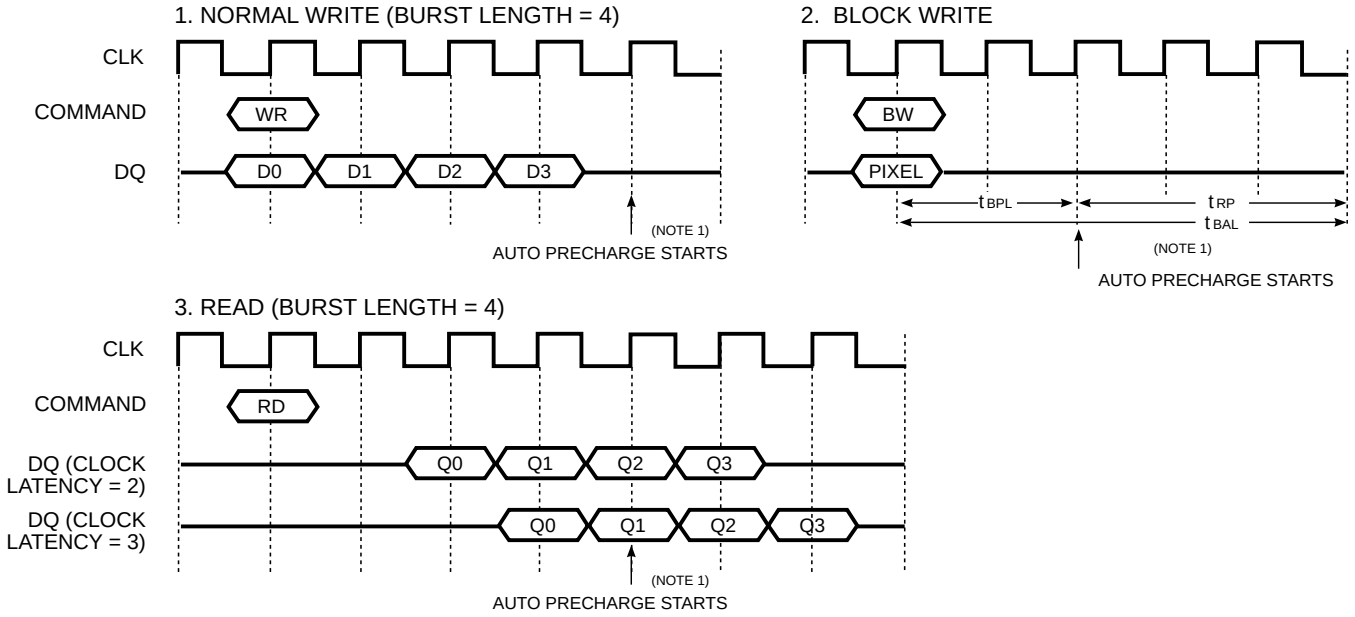
Notes:
1. To Inhibit invalid write, DQM should be issued.
2. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of dual banks operation.

Figure 8. Write Interrupted by Precharge and DQM



Notes:
1. t_{RDL}: Write data-in to PRE command delay, t_{BPL}: Block Write data-in to PRE command delay.
2. Number of valid output data after row precharge: 1, 2 for CAS, Latency = 2, 3 respectively.

Figure 9. Precharge



Note:
1. The row active command of the precharge bank can be issued after t_{RP} from this point.
   The new read/write command of other activated bank can be issued from this point.
   At burst read/write with auto precharge, $\overline{CAS}$ interrupt of the same bank is illegal.

Figure 10. Auto Precharge

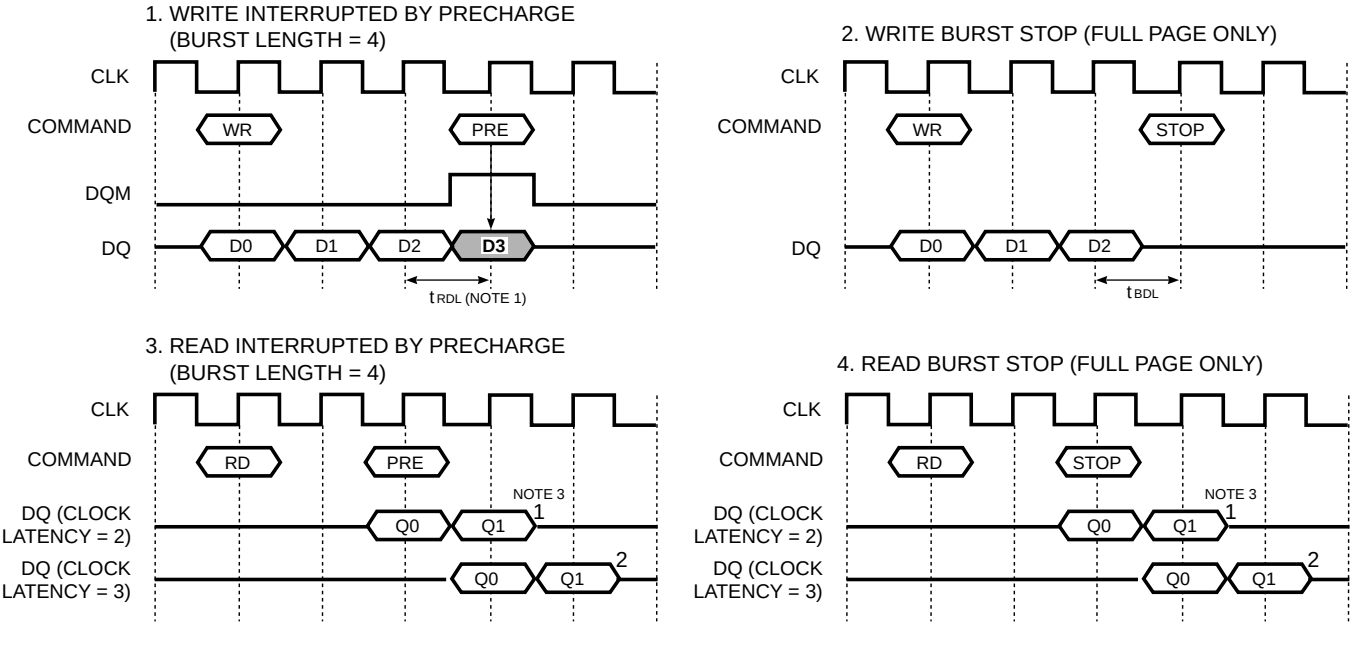
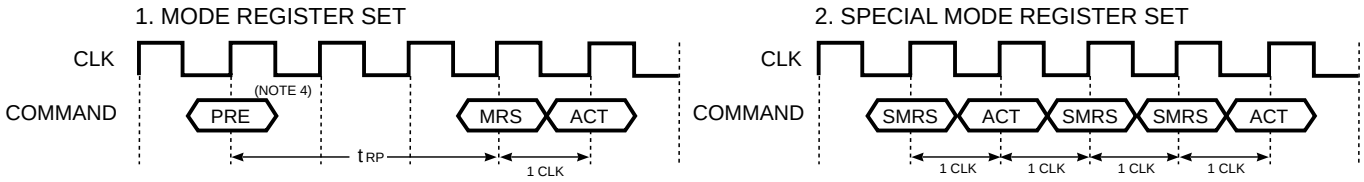


Figure 11. Burst Stop and Precharge Interrupted



Notes:
1. t_{RDL}: 1 CLK; last data in to Row Precharge.
2. t_{BDL}: 1 CLK; last data in to Burst Stop Delay.
3. Number of valid output data after Row Precharge or Burst Stop: 1, 2 for $\overline{CAS}$, Latency = 2, 3 respectively.
4. PRE: Both banks precharge, if necessary.
   MRS can be issued only at all banks precharge state.

Figure 12. MRS and SMRS

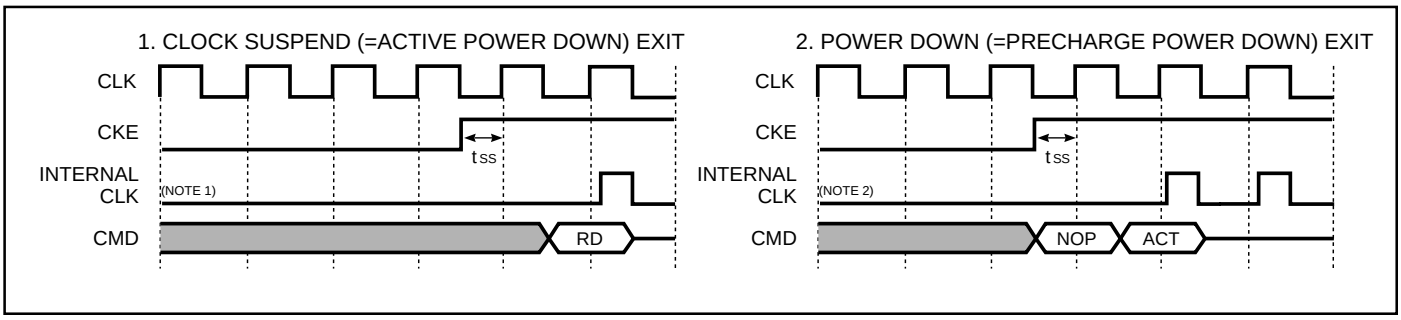
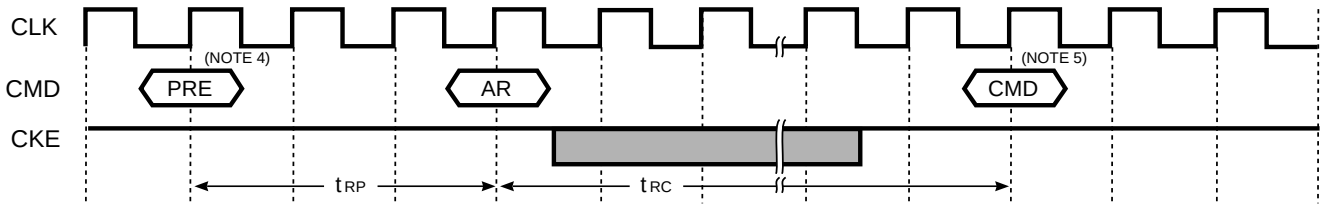
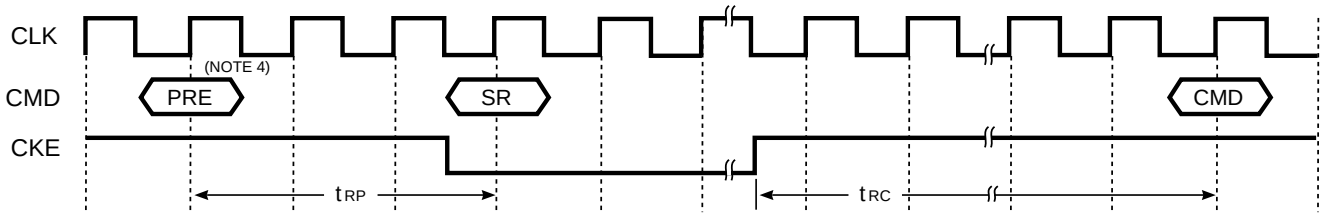


Figure 13. Clock Suspend Exit and Power Down Exit

1. AUTO REFRESH (NOTE 3)



2. SELF REFRESH (NOTE 6)



Notes:
1. Active power down: one or more banks active state.
2. Precharge power down: both banks precharge state.
3. The Auto Refresh is the same as CBR refresh of conventional DRAM. No precharge commands are required after Auto Refresh command. During t_{RC} from Auto Refresh command, any other command can not be accepted.
4. Before excuting auto/self refresh command, both banks must be idle state.
5. (S)MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refresh mode, refresh interval and refresh operation are performed internally. After self refresh entry, self refresh mode is kept while CKE is low.
   During self refresh mode, all inputs except CKE will be “Don’t Care”, and outputs will be in Hi-Z state.
   During t_{RC} from self refresh exit command, any other comman can not be accepted.
   Before/after self refresh mode, burst auto refresh (2K cycles) is recommended.

Figure 14. Auto Refresh and Self Refresh

Table 11. About Burst Type Control

Basic Mode	Sequential Counting	At MRS, A3="0". See the Burst Sequence Table. (BL=4, 8) BL=1, 2, 4, 8 and full page wrap around.
	Interleave Counting	At MRS A3="1". See the Burst Sequence Table. (BL=4, 8) BL=4, 8. At BL=1, 2 Interleave Counting = Sequential Counting
Pseudo-Mode	Pseudo-Document Sequential Counting	At MRS A3="1". (See to interleave Counting Mode) Staring Address LSB 3 bits A 0-2 should be "000" or "111". @BL=8 — if LSB ="000": Increment Counting. — if LSB ="111": Decrement Counting. For Example, (Assume Addresses except LSB 3 bits are all 0, BL=8) — @ write, LSB ="000", Accessed Column in order 0-1-2-3-4-5-6-7 — @ read, LSB ="111", Accessed Column in order 7-6-5-4-3-2-1-0 At BL=4, same applications are possible. As above example, at interleave Counting mode, by confining starting address to some value, Pseudo-Decrement Counting Mode can be realize. See the Burst Sequence Table carefully.
	Pseudo-Binary Counting	At MRS A3="0". (See to Sequential Counting Mode) A0-2 ="111". (See to Full Page Mode). Using Full Page Mode and Burst Stop Command, Binary Counting Mode can be realized. — @ Sequential Counting, Accessed Column in order 3-4-5-6-7-1-2-3 (BL=8) — @ Pseudo-Binary Counting Accessed Column in order 3-4-5-6-7-8-9-10 (Burst Stop command) **Note:** The next column address of 256 is 0.
Random Mode	Random Column Access, t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

Table 12. About Burst Length Control

Basic Mode	1	At MRS A2, 1, 0 = "000". At auto precharge, t_{RAS} should not be violated.
	2	At MRS A2, 1, 0 = "001". At auto precharge, t_{RAS} should not be violated.
	4	At MRS A2, 1, 0 ="010".
	8	At MRS A2, 1, 0 ="011".
	Full Page	At MRS A2, 1, 0 ="111". Wrap around mode (infinite burst length) should be stopped by burst stop. $\overline{RAS}$ interrupt or $\overline{CAS}$ interrupt.
Special Mode	BRSW	At MRS A9 ="1". Read Burst =1, 2, 4, 8, full page/write Burst =1. At auto precharge of write, t_{RAS} should not be violated.
	Block Write	8-Column Block Write. LSB A0-2 are ignored. Burst length =1. t_{RAS} should not be violated. At auto precharge, t_{RAS} should not be violated.
Random Mode	Burst Stop	t_{BDL} =1, Valid DQ after burst stop is 1, 2 for CL=2, 3 respectively. Using burst stop command, random mode it is possible only at full page burst length.
Interrupt Mode	$\overline{RAS}$ Interrupt	Before the end of burst, Row precharge command of the same bank stops read/write burst with Row precharge. t_{RDL} =1 with DQM, valid DQ after burst stop is 1, 2 for CL=2, 3 respectively. During read/write burst with auto precharge, $\overline{RAS}$ interrupt can not be issued.
	$\overline{CAS}$ Interrupts	Before the end of burst, new read/write stops read/write burst and starts new read/write burst or block write. During read write burst with auto precharge, $\overline{CAS}$ interrupt can not be issued.

Table 13. Mask Function Procedure

1. Normal Write
   I/O masking: By Mask at Write Per Bit Mode, the selected bit planes keep the original data.
   If bit plane 0, 3, 7, 9, 19, 22, 24, and 31 keep the original value.
   a. STEP
      I. SMRS(LMR): Load mask [31-0]="0111, 1110, 1011, 0111, 1111, 1101, 0111, 0110"
      II. Row Active with DSF "H": Write Per Bit Mode Enable
      III. Perform Normal Write
   b. Illustration

I/O (=DQ)	31 24	23 16	15 8	7 0
External Data-in	11111111	11111111	00000000	00000000
DQMi	DQM3=0	DQM2=0	DQM1=0	DQM0=1
Mask Register	01111110	10110111	11111101	01110110
Before Write	00000000	00000000	11111111	11111111
After Write	01111110	10110111	00000010	11111111

DQM byte masking

2. Block Write
   Pixel masking: By Pixel Data issued through DQ pin, the selected pixels keep the original data.
   See Pixel To DQ Mapping Table.
   If Pixel 0, 4, 9, 13, 18, 22, 27, and 31 keep the original white color.

   Assume 8bpp
   White = "0000, 0000", Red = "1010, 0011", Green = "1110, 0001", Yellow = "0000, 1111", Blue = "1100, 0011"
   a. STEP
      I. SMRS(LCR): Load color (for 8bpp, through x32 DQ color0-3 are loaded into color registers). Load (color3, color2, color1, color0) = (Blue, Green, Yellow, Red)
      "1100,0011,1110,0001,0000,1111,1010,0011"
      II. Row Active with DSF "L": I/O Mask by Write Per Bit Mode Disable
      III. Block write with DQ[31-0] = "0111, 0111, 1011, 1011, 1101, 1101, 1110, 1110"

Table 13. Mask Function Procedure *(continued)*

b. Illustration

I/O (=DQ)(1)	31 24	23 16	15 8	7 0
DQMi	DQM3=0	DQM2=0	DQM1=0	DQM0= 1
Color Register	Color3=Blue	Color2=Green	Color1=Yellow	Color0=Red
Before Block Write & DQ (Pixel data)				
000	White DQ24=H	White DQ16=H	White DQ8=H	White DQ0=L
001	White DQ25=H	White DQ17=H	White DQ9=L	White DQ1=H
010	White DQ26=H	White DQ18=L	White DQ10=H	White DQ2=H
011	White DQ27=L	White DQ19=H	White DQ11=H	White DQ3=H
100	White DQ28=H	White DQ20=H	White DQ12=H	White DQ4=L
101	White DQ29=H	White DQ21=H	White DQ13=L	White DQ5=H
110	White DQ30=H	White DQ22=L	White DQ14=H	White DQ6=H
111	White DQ31=L	White DQ23=H	White DQ15=H	White DQ7=H
After Block Write				
000	Blue	Green	Yellow	White
001	Blue	Green	White	White
010	Blue	White	Yellow	White
011	White	Green	Yellow	White
100	Blue	Green	Yellow	White
101	Blue	Green	White	White
110	Blue	White	Yellow	White
111	White	Green	Yellow	White

Note:
1. At normal write, ONE column is selected among columns decoded by A2-0 (000-111).
   At block write, instead of ignored address A2-0, DQ0-31 control each pixel.

3. Pixel and I/O masking: By Mask at Write Per Bit Mode, the selected bit planes keep the original data.
   By Pixel Data issued through DQ pin, the selected pixels keep the original data.
   See Pixel To DQ Mapping Table.

Assume 8bpp,
White = “0000, 0000”, Red = “1010, 0011”, Green = “1110, 0001”, Yellow = “0000, 1111”, Blue = ‘ 1100, 0011"

a. STEP
   I. SMRS(LCR): Load color (for 8bpp, through x 32 DQ color0-3 are loaded into color registers)
      Load (color3, color2, color1, color0,) = (Blue, Green, Yellow, Red)
      =“1100, 0011, 1110, 0001, 0000, 1111, 1010, 0011"
   II. SMRS(LMR) Load mask. Mask[31-0] = “1111, 1111, 1101, 1101, 0100, 0010, 0111, 0110”
      Byte 3 : No I/O Masking ; Byte 2: I/O Masking ; Byte 1: I/O and Pixel Masking ; Byte 0: DQM Byte Masking
   III. Row Active with DSF “H” : I/O mask by Write Per Bit Mode Enable
   IV. Block Write with DQ [31-0] = “0111, 0111,1111, 1111, 0101, 0101, 1110, 1110” (Pixel Mask)

Table 13. Mask Function Procedure *(continued)*

b. Illustration

I/O (=DQ)[1]	31 24	23 16	15 8	7 0
Color Register	Blue 11000011	Green 11100001	Yellow 00001111	Red 10100011
DQMi	DQM3=0	DQM2=0	DQM1=0	DQM0=1
Mask Register	11111111	11011101	01000010	01110110
Before Write	Yellow 00001111	Yellow 00001111	Green 11100001	White 00000000
After Write	Blue 11000011	Blue 11000011	Red 10100011	White 00000000

I/O (=DQ)[1]	31 24	23 16	15 8	7 0
DQMi	DQM3=0	DQM2=0	DQM1=0	DQM0=1
Color Register	Color3=Blue	Color2=Green	Color1=Yellow	Color0=Red
Before Block Write & DQ (Pixel data)				
000	Yellow DQ24=H	Yellow DQ16=H	Green DQ8=H	White DQ0=L
001	Yellow DQ25=H	Yellow DQ17=H	Green DQ9=L	White DQ1=H
010	Yellow DQ26=H	Yellow DQ18=H	Green DQ10=H	White DQ2=H
011	Yellow DQ27=L	Yellow DQ19=H	Green DQ11=L	White DQ3=H
100	Yellow DQ28=H	Yellow DQ20=H	Green DQ12=H	White DQ4=L
101	Yellow DQ29=H	Yellow DQ21=H	Green DQ13=L	White DQ5=H
110	Yellow DQ30=H	Yellow DQ22=H	Green DQ14=H	White DQ6=H
111	Yellow DQ31=L	Yellow DQ23=H	Green DQ15=L	White DQ7=H
After Block Write				
000	Blue	Blue	Red	White
001	Blue	Blue	Green	White
010	Blue	Blue	Red	White
011	Yellow	Blue	Green	White
100	Blue	Blue	Red	White
101	Blue	Blue	Green	White
110	Blue	Blue	Red	White
111	Yellow	Blue	Green	White
	PIXEL MASK	**I/O MASK**	**PIXEL & I/O MASK**	**BYTE MASK**

Note:
1. DQM byte masking.
2. At normal write, ONE column is selected among columns decoded by A2-0 (000-111). At block write, instead of ignored address A2-0, DQ0-31 control each pixel.

Table 14. Function Truth Table

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BA (A10)	ADDR	Action
IDLE	H	X	X	X _	X	X	X	NOP
	L	H	H	H	X	X	X	NOP
	L	H	H	L	X	X	X	ILLEGAL(2)
	L	H	L	X	X	BA	CA	ILLEGAL(2)
	L	L	H	H	L	BA	RA	Row Active; Latch Row Address; Non-I/O Mask
	L	L	H	H	H	BA	RA	Row Active; Latch Row Address; I/O Mask
	L	L	H	L	L	X	PA	Auto Refresh or Self Refresh(4)
	L	L	H	L	H	BA	X	NOP
	L	L	L	H	L	X	X	Auto Refresh or Self Refresh(5)
	L	L	L	H	H	BA	X	ILLEGAL
	L	L	L	L	L	OP Code		Mode Register Access(5)
	L	L	L	L	H	OP Code		Special Mode Register Access(6)
Row Active	H	X	X	X	X	X	X	NOP
	L	H	H	H	X	X	X	NOP
	L	H	H	L	X	X	X	ILLEGAL(2)
	L	H	L	H	L	BA	CA, AP	Begin Read; Latch CA; Determine AP
	L	H	L	H	H	X	X	ILLEGAL
	L	H	L	L	L	BA	CA, AP	Begin Write; Latch CA; Determine AP
	L	H	L	L	H	BA	CA, AP	Begin Write; Latch CA; Determine AP
	L	L	H	H	X	BA	RA	ILLEGAL(2)
	L	L	H	L	L	BA	RA	Precharge
	L	L	H	L	H	X	X	ILLEGAL
	L	L	L	H	X	X	X	ILLEGAL
	L	L	L	L	L	X	X	ILLEGAL
	L	L	L	L	H	OP Code		Special Mode Register Access(6)
Read	H	X	X	X	X	X	X	NOP (Continue Burst to End → • Row Active)
	L	H	H	H	X	X	X	NOP (Continue Burst to End → • Row Active)
	L	H	H	L	L	X	X	Term burst → Row active
	L	H	H	L	H	X	X	ILLEGAL
	L	H	L	H	L	BA	CA,AP	Term burst, Begin Read; Latch CA; Determine AP(3)
	L	H	L	H	H	X	X	ILLEGAL
	L	H	L	L	L	BA	CA, AP	Term burst, Begin Write; Latch CA; Determine AP(3)
	L	H	L	L	H	BA	CA, AP	Term burst. Begin Write; Latch CA; Determine AP(3)
	L	L	H	H	X	BA	RA	ILLEGAL(2)
	L	L	H	L.	L	BA	PA	Term Burst, Precharge timing for Reads(3)
	L	L	H	L	H	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL

Table 14. Function Truth Table *(continued)*

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BA (A10)	ADDR	Action
Write	H	X	X	X	X	X	X	NOP (Continue Burst to End → • Row Active)
	L	H	H	H	X	X	X	NOP (Continue Burst to End → • Row Active)
	L	H	H	L	L	X	X	Term burst → • Row Active
	L	H	H	L	H	X	X	ILLEGAL
	L	H	L	H	L	BA	CA, AP	Term burst, Begin Read; Latch CA; Determine AP(3)
	L	H	L	H	H	X	X	ILLEGAL
	L	H	L	L	L	BA	CA, AP	Term burst, Begin Write; Latch CA; Determine AP(3)
	L	H	L	L	H	BA	CA, AP	Term burst, Begin Write; Latch CA; Determine AP(3)
	L	L	H	H	X	BA	RA	ILLEGAL(2)
	L	L	H	L	L	BA	RA	Term Burst: Precharge timing for Writes(3)
	L	L	H	H	H	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	X	NOP (Continue Burst to End → Precharge)
	L	H	H	H	X	X	X	NOP (Continue Burst to End → Precharge)
	L	H	H	L	X	X	X	ILLEGAL
	L	H	L	H	X	BA	CA, AP	ILLEGAL(2)
	L	H	L	L	X	BA	CA, AP	ILLEGAL(2)
	L	L	H	X	X	BA	RA, PA	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL(2)
Write with Auto Precharge	H	X	X	X	X	X	X	NOP (Continue Burst to End → Precharge)
	L	H	H	H	X	X	X	NOP (Continue Burst to End → Precharge)
	L	H	H	L	X	X	X	ILLEGAL
	L	H	L	H	X	BA	CA, AP	ILLEGAL(2)
	L	H	L	L	X	BA	CA, AP	ILLEGAL(2)
	L	L	H	X	X	BA	RA, PA	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL(2)
Pre-charging	H	X	X	X	X	X	X	NOP → Idle after t_{RP}
	L	H	H	H	X	X	X	NOP → Idle after t_{RP}
	L	H	H	L	X	X	X	ILLEGAL
	L	H	L	X	X	BA	CA, AP	ILLEGAL(2)
	L	L	H	H	X	BA	RA	ILLEGAL(2)
	L	L	H	L	X	BA	PA	NOP → Idle after t_{RP}(2)
	L	L	L	X	X	X	X	ILLEGAL(4)
Block Write Recovering	H	X	X	X	X	X	X	NOP → Row Active after t_{BWC}
	L	H	H	H	X	X	X	NOP → Row Active after t_{BWC}
	L	H	H	L	X	X	X	ILLEGAL
	L	H	L	X	X	BA	CA, AP	ILLEGAL(2)
	L	L	H	H	X	BA	RA	ILLEGAL(2)
	L	L	H	L	X	BA	PA	Term Block Write: Precharge timing for Block Write(2)
	L	L	L	X	X	X	X	ILLEGAL(2)

Table 14. Function Truth Table *(continued)*

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BA (A10)	ADDR	Action
Row	H	X	X	X	X	X	X	NOP → Row Active after t_{RCD}
Activating	L	H	H	H	X	X	X	NOP → Row Active after t_{RCD}
	L	H	H	L	X	X	X	ILLEGAL(2)
	L	H	L	X	X	BA	CA,AP	ILLEGAL(2)
	L	L	H	H	X	BA	RA	ILLEGAL(2)
	L	L	H	L	X	BA	PA	ILLEGAL(2)
	L	L	L	X	X	X	X	ILLEGAL(2)
Refreshing	H	X	X	X	X	X	X	NOP → Idle after t_{RC}
	L	H	H	X	X	X	X	NOP → Idle after t_{RC}
	L	H	L	X	X	X	X	ILLEGAL
	L	L	H	X	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL

Abbreviations:

RA = Row Address (A0-A9) BA = Bank Address (A10) PA = Precharge All (A9)
NOP = No Operation Command CA = Column Address (A0-A7) AP = Auto Precharge (A9)

Notes:

1. All entries assume the CKE was active (High) during the preceding clock cycle and the current clock cycle.
2. Illegal to bank in specified state; Function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA (and PA).
5. Illegal if any bank is not idle.
6. Legal only if all banks are in idle or row active state.

Table 15. Function Truth Table for CKE

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	ADDR	Action
Self Refresh									
	H	X	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	X	Exit Self Refresh → • • • after t_{RC}(1)
	L	H	L	H	H	H	X	X	Exit Self Refresh → • • • after t_{RC}(1)
	L	H	L	H	H	L	X	X	ILLEGAL
	L	H	L	H	L	X	X	X	ILLEGAL
	L	H	L	L	X	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	X	NOP (Maintain Self Refresh)
Both Bank Precharge Power Down									
	H	X	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	X	Exit Power Down → ABI(2)
	L	H	L	H	H	H	X	X	Exit Power Down → ABI(2)
	L	H	L	H	H	L	X	X	ILLEGAL
	L	H	L	H	L	X	X	X	ILLEGAL
	L	H	L	L	X	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	X	NOP (Maintain Low Power Mode)
All Banks Idle									
	H	H	X	X	X	X	X	X	Refer to Table 14
	H	L	H	X	X	X	X	X	Enter Power Down(3)
	H	L	L	H	H	H	X	X	Enter Power Down(3)
	H	L	L	H	H	L	X	X	ILLEGAL
	H	L	L	H	L	X	X	X	ILLEGAL
	H	L	L	L	H	X	X	X	ILLEGAL
	H	L	L	L	L	H	X	X	Enter Self Refresh
	H	L	L	L	L	L	X	X	ILLEGAL
	L	L	X	X	X	X	X	X	NOP
Any State Other Than Listed Above									
	H	H	X	X	X	X	X	X	Refer to Operations in Table 14
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle(4)
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle(4)
	L	L	X	X	X	X	X	X	Maintain Clock Suspend

Abbreviations:
ABI = All Banks Idle

Notes:
1. After CKEs low-to-high transition to exit self refresh mode. And a time of t_{RC}(min) has to be elapse after CKEs low-to-high transition to issue a new command.
2. CKE low to high transition is asynchronous as if restart internal clock.
   A minimum setup time "t_{SS} + one clock" must be satisfy before any command other than exit.
3. Power down and self refresh can be entered only from the all banks idle state.
4. Must be a legal command.

Table 16. Absolute Maximun Ratings(1)

Symbol	Parameters	Rating	Unit
$V_{CC\ MAX}$	Maximum Supply Voltage	–1.0 to +4.6	V
$V_{CCQ\ MAX}$	Maximum Supply Voltage for Output Buffer	–1.0 to +4.6	V
V_{IN}	Input Voltage	–1.0 to +4.6	V
V_{OUT}	Output Voltage	–1.0 to +4.6	V
$P_{D\ MAX}$	Allowable Power Dissipation	1	W
I_{CS}	Output Shorted Current	50	mA
T_{OPR}	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	–55 to +150	°C

Table 17. DC Recommended Operating Conditions(2) (At T_A = 0 to +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}, V_{CCQ}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	—	Vcc + 0.3	V
V_{IL}	Input Low Voltage	–0.3	—	+0.8	V

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to GND.
3. V_{IH} (max) = 5.5V for pulse width ≤ 5 ns.
4. V_{IL} (min) = 1.5V for pulse width ≤ 5 ns.

Table 18. Capacitance Characteristics (At T_A = 0 to +25°C, V_{CC} = V_{CCQ} = 3.3V ± 0.3V, f = 1 MHz)

Symbol	Parameter	Typ.	Max.	Unit
$C_{IN}1$	Input Capacitance: A0-A10	—	4	pF
$C_{IN}2$	Input Capacitance: CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM0-3	—	4	pF
CI/O	Data Input/Output Capacitance: DQ0-DQ31	—	5	pF

Table 19. DC Electrical Characteristics (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition		Speed	Min.	Max.	Unit
I_{IL}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}, with pins other than the tested pin at 0V			–5	5	µA
I_{OL}	Output Leakage Current	Output is disabled 0V ≤ V_{OUT} ≤ V_{CC}			–5	5	µA
V_{OH}	Output High Voltage Level	I_{OUT} = –2 mA			2.4	—	V
V_{OL}	Output Low Voltage Level	I_{OUT} = +2 mA			—	0.4	V
I_{CC1}	Operating Current(1,2)	One Bank Operation, Burst Length=1		-7	—	145	mA
		t_{RC} ≥ t_{RC} (min), I_{OL} = 0 mA		-8	—	180	
		t_{CK} ≥ t_{CK} (min)		-10	—	170	
I_{CC2P}	Precharge Standby Current	CKE ≤ V_{IL} (max)	t_{CK} = t_{CK} (min)		—	3	mA
I_{CC2PS}	(In Power-Down Mode)		t_{CK} = ∞		—	2	
I_{CC2N}	Precharge Standby Current	CKE ≥ V_{IH} (min)	t_{CK} = t_{CK} (min)		—	30	mA
I_{CC2NS}	(In Non Power-Down Mode)		t_{CK} = ∞		—	15	
I_{CC3P}	Active Standby Current	CKE ≤ V_{IL} (max)	t_{CK} = t_{CK} (min)		—	3	mA
I_{CC3PS}	(In Power-Down Mode)		t_{CK} = ∞		—	2	
I_{CC3N}	Active Standby Current	CKE ≥ V_{IH} (min)	t_{CK} = t_{CK} (min)		—	50	mA
I_{CC3NS}	(In Non Power-Down Mode)		t_{CK} = ∞		—	30	
I_{CC4}	Operating Current	t_{CK} = t_{CK} (min)	$\overline{CAS}$ latency = 3	-7	—	195	mA
	(In Burst Mode)(1)	I_{OL} = 0 mA		-8	—	170	
		All banks activated		-10	—	140	
			$\overline{CAS}$ latency = 2	-7	—	195	mA
				-8	—	170	
				-10	—	140	
I_{CC5}	Auto-Refresh Current	t_{RC} = t_{RC} (min)		-7	—	195	mA
				-8	—	170	
				-10	—	140	
I_{CC6}	Self-Refresh Current	CKE ≤ 0.2V			—	2	mA
I_{CC7}	Operating Current	t_{RC} ≥ t_{RC} (min)	I_{OL} = 0 mA, t_{BWC} (min)	-7	—	190	mA
	(one Bank Block Write)			-8	—	180	
				-10	—	170	

Notes:
1. These are the values at the minimum cycle time. Since the currents are transient, these values decrease as the cycle time increases. Also note that a bypass capacitor of at least 0.01 µF should be inserted between Vcc and GND for each memory chip to suppress power supply voltage noise (voltage drops) due to these transient currents.
2. Icc1 and Icc4 depend on the output load. The maximum values for Icc1 and Icc4 are obtained with the output open state.

Table 20. AC Characteristics[1,2,3]

Symbol	Parameter		-7 Min.	-7 Max.	-8 Min.	-8 Max.	-10 Min.	-10 Max.	Units
t_{CK}	Clock Cycle Time	CAS Latency = 3	7	—	8	—	10	—	ns
		CAS Latency = 2	10	—	12	—	13	—	
t_{AC}	Access Time From CLK[4]	CAS Latency = 3	—	6	—	6.5	—	7	ns
		CAS Latency = 2	—	7	—	8	—	9	
t_{CHI}	CLK HIGH Level Width		2.5	—	3	—	3.5	—	ns
t_{CL}	CLK LOW Level Width		2.5	—	3	—	3.5	—	ns
t_{OH}	Output Data Hold Time	CAS Latency = 3	2.5	—	2.5	—	2.5	—	ns
		CAS Latency = 2	2.5	—	2.5	—	2.5	—	
		CAS Latency = 1	2.5	—	2.5	—	2.5	—	
t_{LZ}	Output LOW Impedance Time		0	—	0	—	0	—	ns
t_{HZ}	Output HIGH Impedance Time[5]	CAS Latency = 3	4	6	4	8	4	10	ns
		CAS Latency = 2	4	10	4	12	4	14	
t_{DS}	Input Data Setup Time		2	—	2.5	—	3	—	ns
t_{DH}	Input Data Hold Time		1	—	1	—	1	—	ns
t_{AS}	Address Setup Time		2	—	2.5	—	3	—	ns
t_{AH}	Address Hold Time		1	—	1	—	1	—	ns
t_{CKS}	CKE Setup Time		2	—	2.5	—	3	—	ns
t_{CKH}	CKE Hold Time		1	—	1	—	1	—	ns
t_{CKA}	CKE to CLK Recovery Delay Time		1CLK+3	—	1CLK+3	—	1CLK+3	—	ns
t_{CS}	Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, DSF)		2	—	2.5	—	3	—	ns
t_{CH}	Command Hold Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, DSF)		1	—	1	—	1	—	ns
t_{RC}	Command Period (REF to REF / ACT to ACT)		63	—	72	—	90	—	ns
t_{RAS}	Command Period (ACT to PRE)		45	100,000	48	102,000	50	102,000	ns
t_{RP}	Command Period (PRE to ACT)		21	—	24	—	26	—	ns
t_{RCD}	$\overline{CAS}$ to $\overline{RAS}$ Delay		20	—	20	—	20	—	ns
t_{RRD}	Command Period (ACT [0] to ACT[1])		14	—	16	—	20	—	ns
t_{DPL}	Last Data In To Precharge	CAS Latency = 3	14	—	16	—	20	—	ns
	Command Delay Time	CAS Latency = 2	14	—	16	—	20	—	
t_{DAL}	Last Data In To Active / Refresh	CAS Latency = 3	35	—	40	—	50	—	ns
	Command Delay time	CAS Latency = 2	35	—	40	—	50	—	
	(Auto-Precharge, same bank)								
t_{BDPL}	Block Write to Precharge Command Delay Time		14	—	16	—	20	—	ns
t_{BWC}	Block Write Cycle Time		14	—	16	—	20	—	ns
t_T	Transition Time		1	30	1	30	1	30	ns
t_{REF}	Refresh Cycle Time		—	32	—	32	—	32	ns

Notes:

1. When power is first applied, memory operation should be started 100 µs after Vcc and VccQ reach their stipulated voltages. Also note that the power-on sequence must be executed before starting memory operation.
2. Measured with t_T = 1 ns.
3. The reference level is 1.4V when measuring input signal timing. Rise and fall times are measured between V_{IH} (min.) and V_{IL} (max.).
4. Access time is measured at 1.4V with the load shown in the figure below.
5. The time t_{HZ} (max.) is defined as the time required for the output voltage to transition by ± 200 mV from V_{OH} (min.) or V_{OL} (max.) when the output is in the high impedance state.

Figure 21. Operating Frequency / Latency Relationships

Symbol	Parameter	-7		-8		-10		Units
CL		**3**	**2**	**3**	**2**	**3**	**2**	
t_{CK}	Clock Cycle Time	7	10	8	12	10	15	ns
—	Operating Frequency	143	100	125	83	100	66	MHz
t_{CAC}	$\overline{CAS}$ Latency	3	2	3	2	3	2	cycle
t_{RCD}	Active Command to Read/Write Command Delay Time	3	2	3	2	3	2	cycle
t_{RAC}	$\overline{RAS}$ Latency (t_{RCD} + t_{CAC})	6	4	6	4	6	4	cycle
t_{RC}	Command Period (REF to REF/ACT to ACT)	9	6	9	6	9	6	cycle
t_{RAS}	Command Period (ACT to PRE)	6	4	6	4	6	4	cycle
t_{RP}	Command Period (PRE to ACT)	3	2	3	2	3	2	cycle
t_{RRD}	Command Period (ACT[0] to ACT [1])	2	2	3	2	2	3	cycle
t_{CCD}	Column Command Delay Time (READ, READA, WRIT, WRITA)	1	1	1	1	1	1	cycle
t_{DPL}	Last Data In to Precharge Command Delay Time	2	2	2	2	2	2	cycle
t_{DAL}	Last Data In to Active/Refresh Command Delay Time (Auto-Precharge, Same Bank)	5	4	5	4	5	4	cycle
t_{RBD}	Burst Stop Command to Output in HIGH-Z Delay Time (Read)	3	2	3	2	3	2	cycle
t_{WBD}	Burst Stop Command to Input in Invalid Delay Time (Write)	0	0	0	0	0	0	cycle
t_{RQL}	Precharge Command to Output in HIGH-Z Delay Time (Read)	3	2	3	2	3	2	cycle
t_{WDL}	Precharge Command to Input in Invalid Delay Time (Write)	0	0	0	0	0	0	cycle
t_{BDAL}	Block Write to Active Command (Auto Precharge, Same Bank)	6	5	6	5	6	5	cycle
t_{EP}	Last Data Out to Precharge Command	–2	–1	–2	–1	–2	–1	cycle
t_{SMCD}	Special Mode Register Set to Command	1	1	1	1	1	1	cycle
t_{RR}	Register Set Command to Register Set Command	2	2	2	2	2	2	cycle
t_{PQL}	Last Output to Auto-Precharge Start Time (Read)	–2	–1	–2	–1	–2	–1	cycle
t_{QMD}	DQM to Output Delay Time (Read)	2	2	2	2	2	2	cycle
t_{DMD}	DQM to Input Delay Time (Write)	0	0	0	0	0	0	cycle
t_{MCD}	Mode Register Set to Command Delay Time	1	1	1	1	1	1	cycle

AC TIMING WAVEFORMS

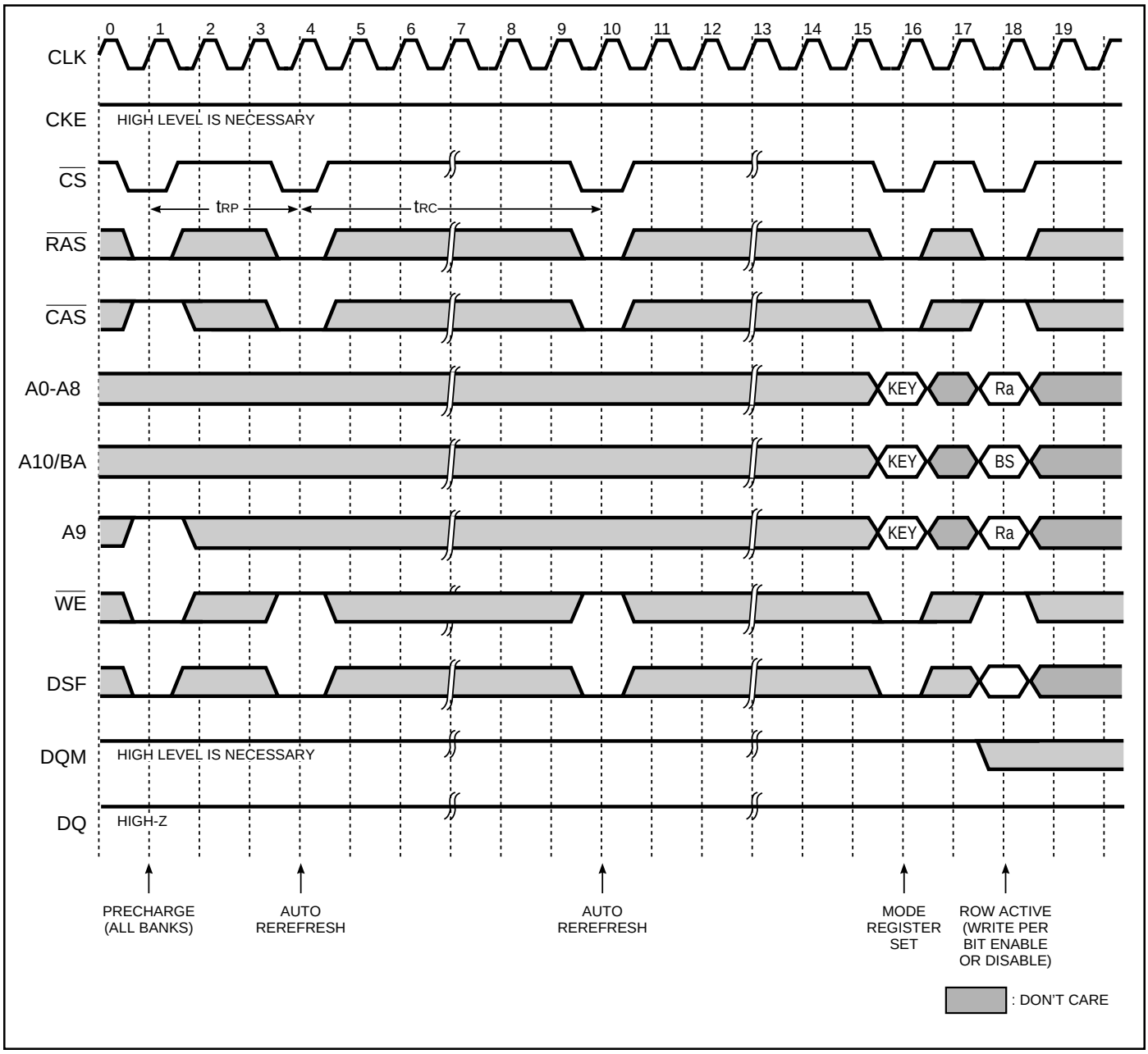


Figure 18. Power On Sequence and Auto Refresh

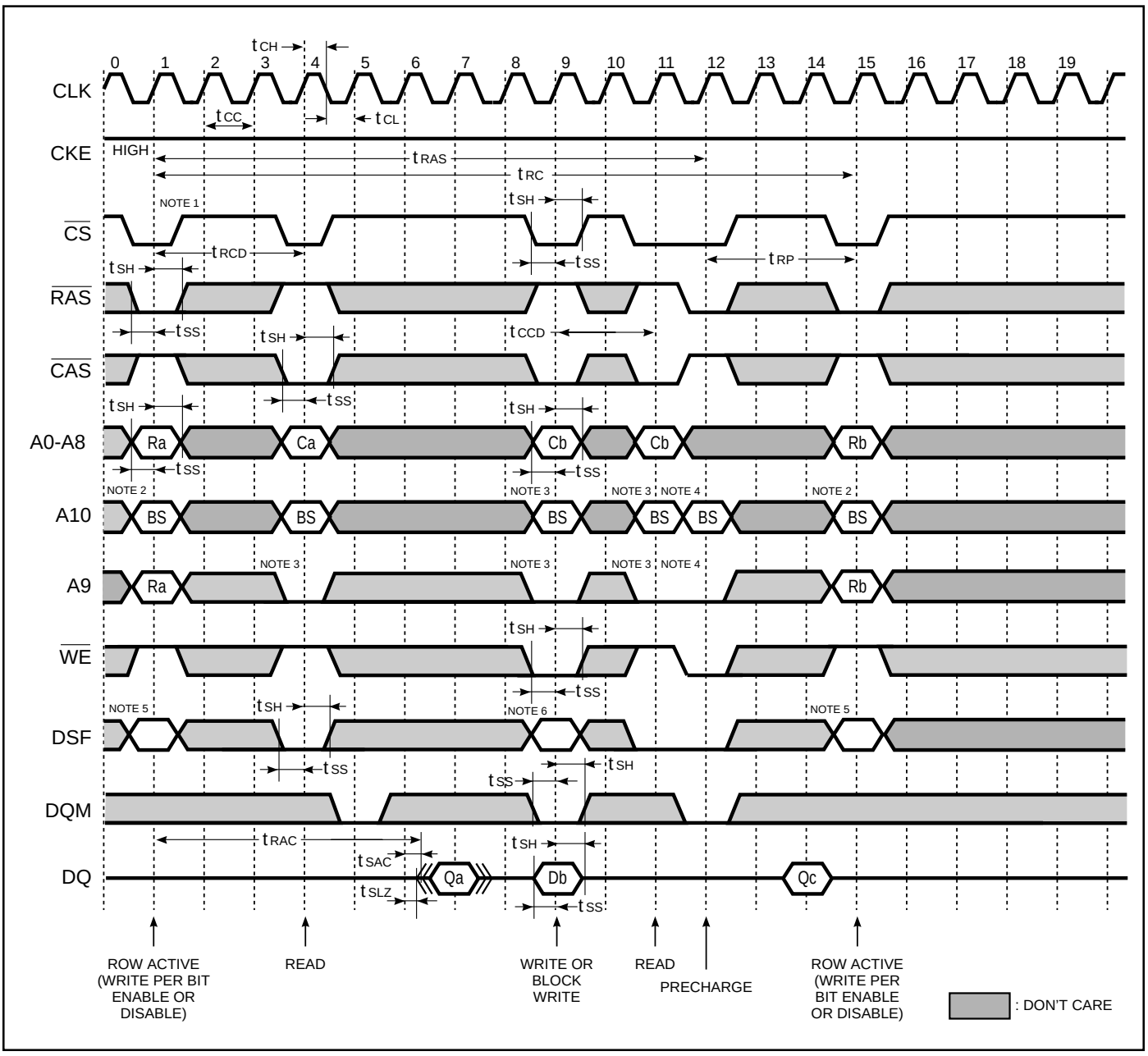


Figure 19. Single Bit Read-Write-Read Cycle (Same Page) at $\overline{\text{CAS}}$ Latency = 3, Burst Length = 1

Notes:

1. All inputs can be "Don't Care" when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active and read/write are controlled by A10.

A10	Active and Read/Write
0	Bank A
1	Bank B

3. Enable and disable auto precharge function are controlled by A9 in read/write command.

A9	A10	Operation
0	0	Disable auto precharge, leave bank A active at end of burst.
0	1	Disable auto precharge, leave bank B active at end of burst.
1	0	Enable auto precharge, precharge bank A at end of burst.
1	1	Enable auto precharge, precharge bank B at end of burst.

4. A9 and A10 control bank precharge when precharge command is asserted.

A9	A10	Precharge
0	0	Bank A
0	1	Bank B
1	X	Both Bank

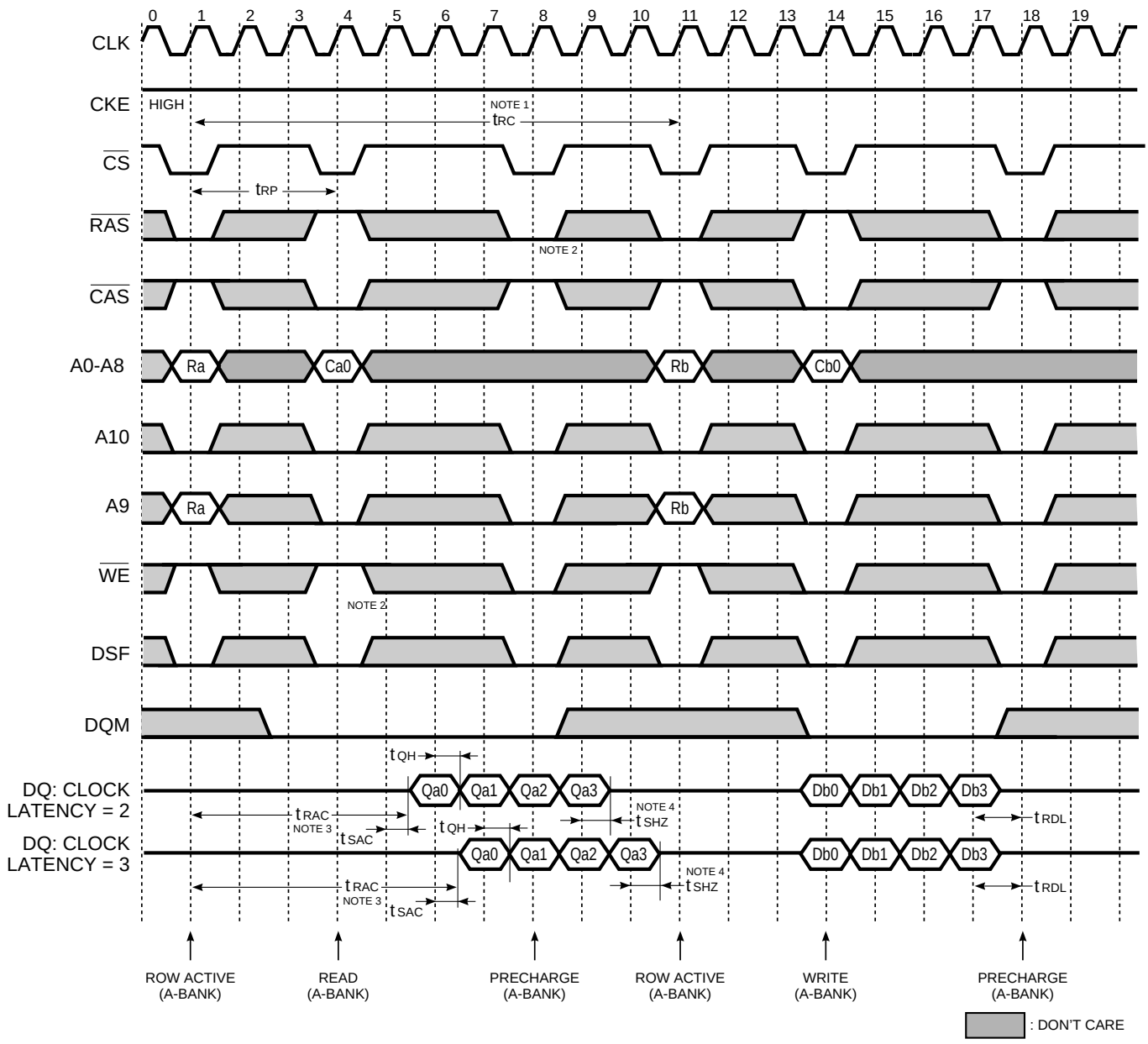
5. Enable and disable Write-per Bit function are controlled by DSF in Row Active command.

A10	DSF	Operation
0	L	Bank A row active, disable write per bit function for bank A.
0	H	Bank A row active, enable write per bit function for bank A.
1	L	Bank B row active, disable write per bit function for bank B.
1	H	Bank B row active, enable write per bit function for bank B.

6. Block write/normal write is controlled by DSF.

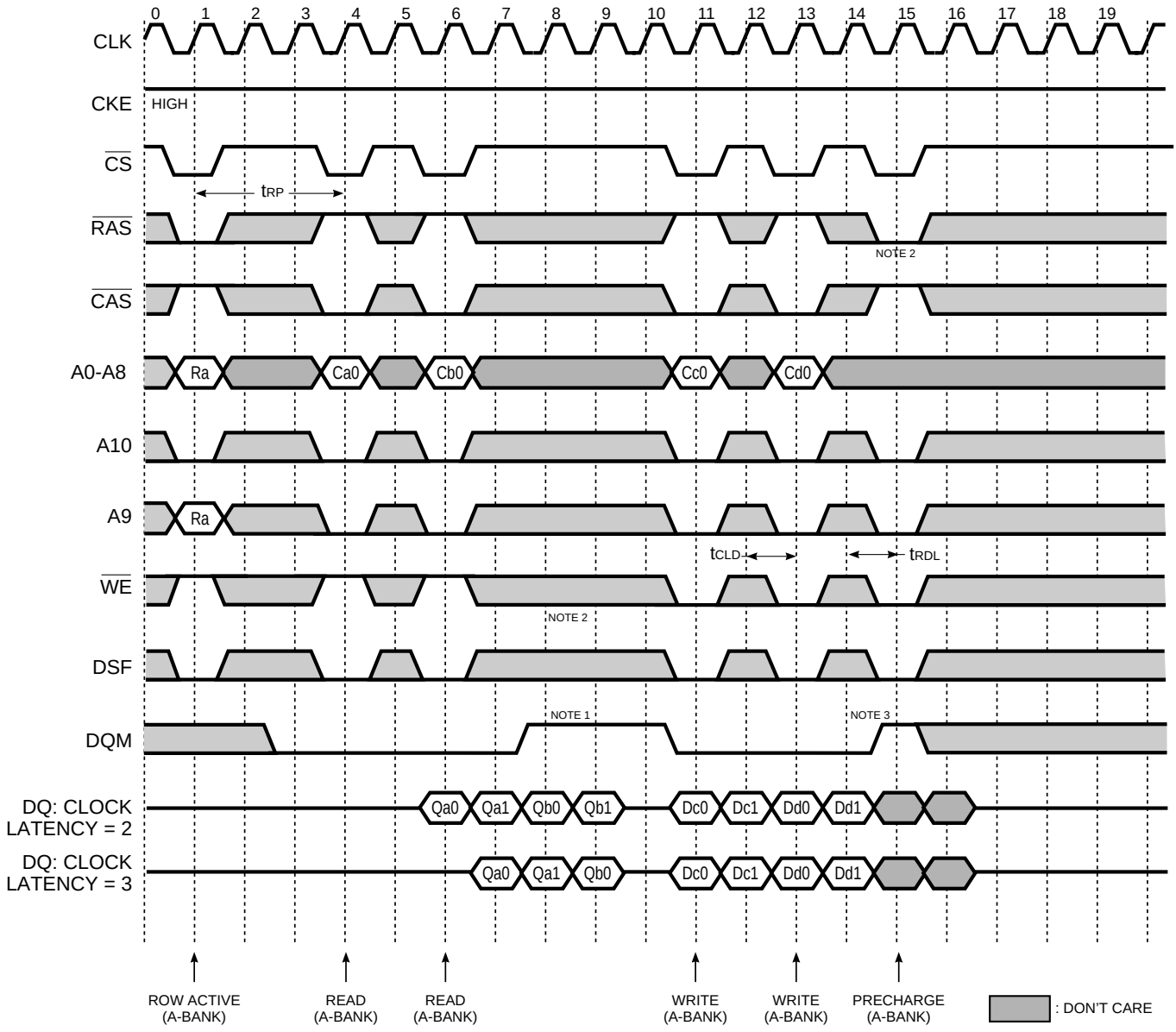
DSF	Operation	Minimum cycle time
L	Normal write	t_{CCD}
H	Block write	t_{BWC}

Figure 19. Single Bit Read-Write-Read Cycle (Same Page) at $\overline{CAS}$ Latency = 3, Burst Length = 1 *(continued)*



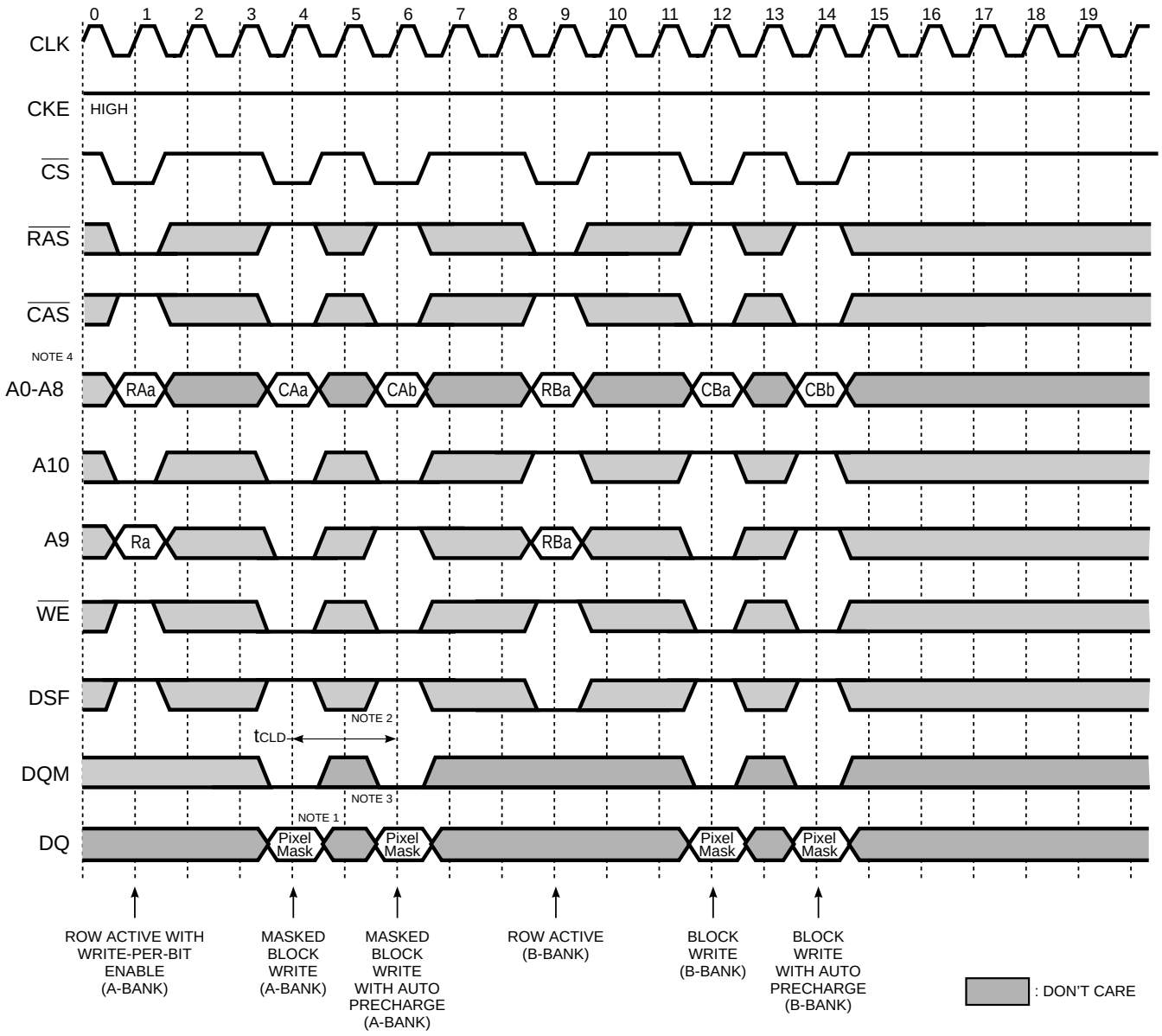
Notes:
1. Minimum cycle time is required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. [CAS Length = 1] valid output data available after Row enters precharge. Last valid output will be Hi-Z after t_{SHZ} from the clock.
3. Access time from Row address. t_{CC} x (t_{RCD} = CAS Latency = 1) + t_{SAC}.
4. Output will be Hi-Z after the end of burst (1, 2, 4, and 8). At Full page bit burst, burst is wrap-around.

Figure 20. Read and Write Cycle at Same Bank at Burst Length = 4



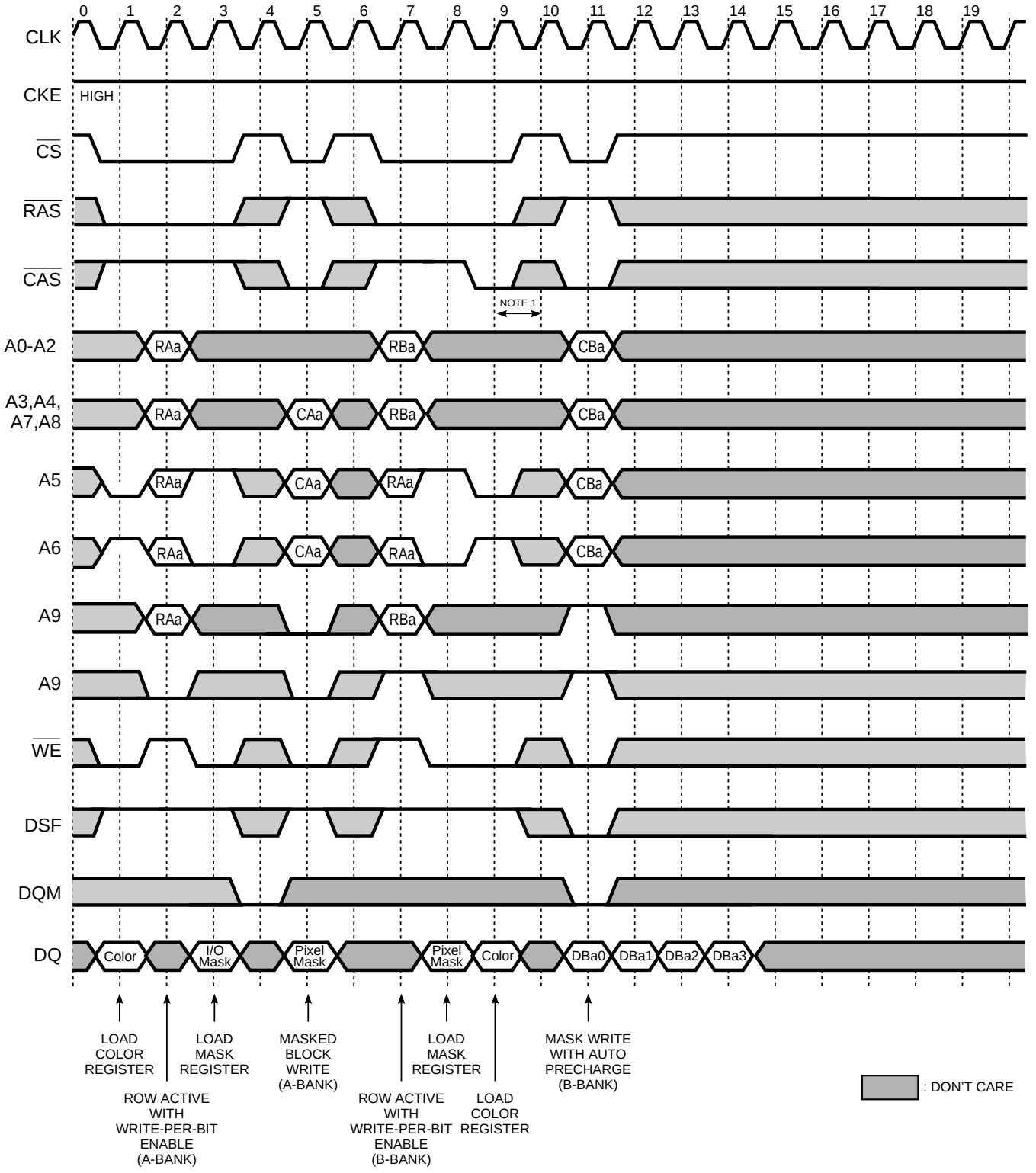
Notes:
1. To write data before burst read ends, DQM should be asserted three cycles prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

Figure 21. Page Read and Write Cycle Same Bank at Burst Length = 4



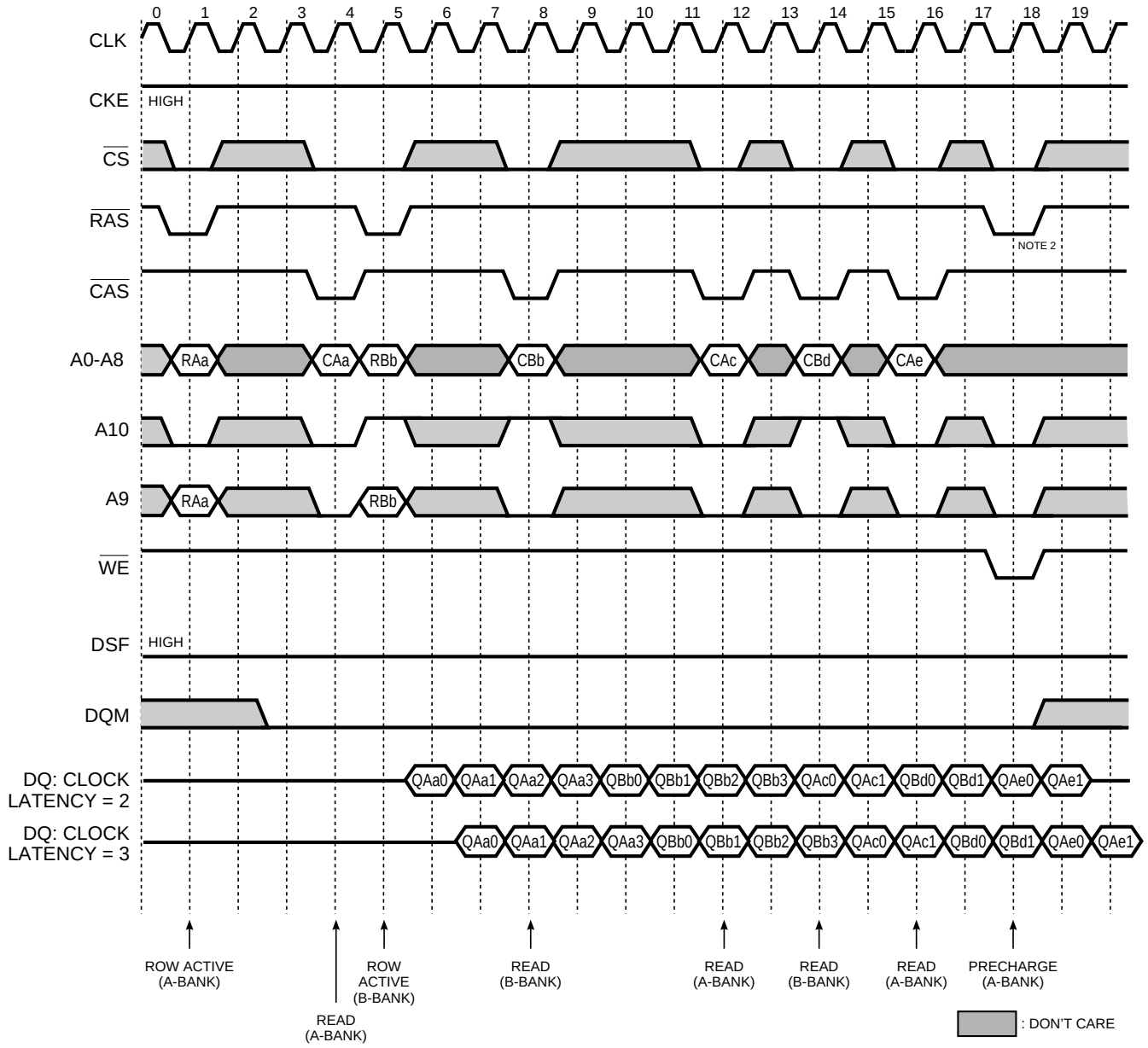
Notes:
1. Column Mask (DQi = L: Mask, DQi = H: Non-mask).
2. t_{BWC}: Block Write Cycle time.
3. At Block Write, second cycle should be in NOP.
   Other Bank can be active or precharge.
4. At Block Write, CA0-2 are ignored.

Figure 22. Block Write Cycle (with Auto Precharge)



Note:
1. At the next clock of special mode register set command, new command is possible.

Figure 23. SMRS and Block/Normal Write at Burst Length = 4



Notes:
1. $\overline{CS}$ can be "Don't Care" when $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are high at the clock high going edge.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Figure 24. Page Read Cycle at Different Bank at Burst Length = 4

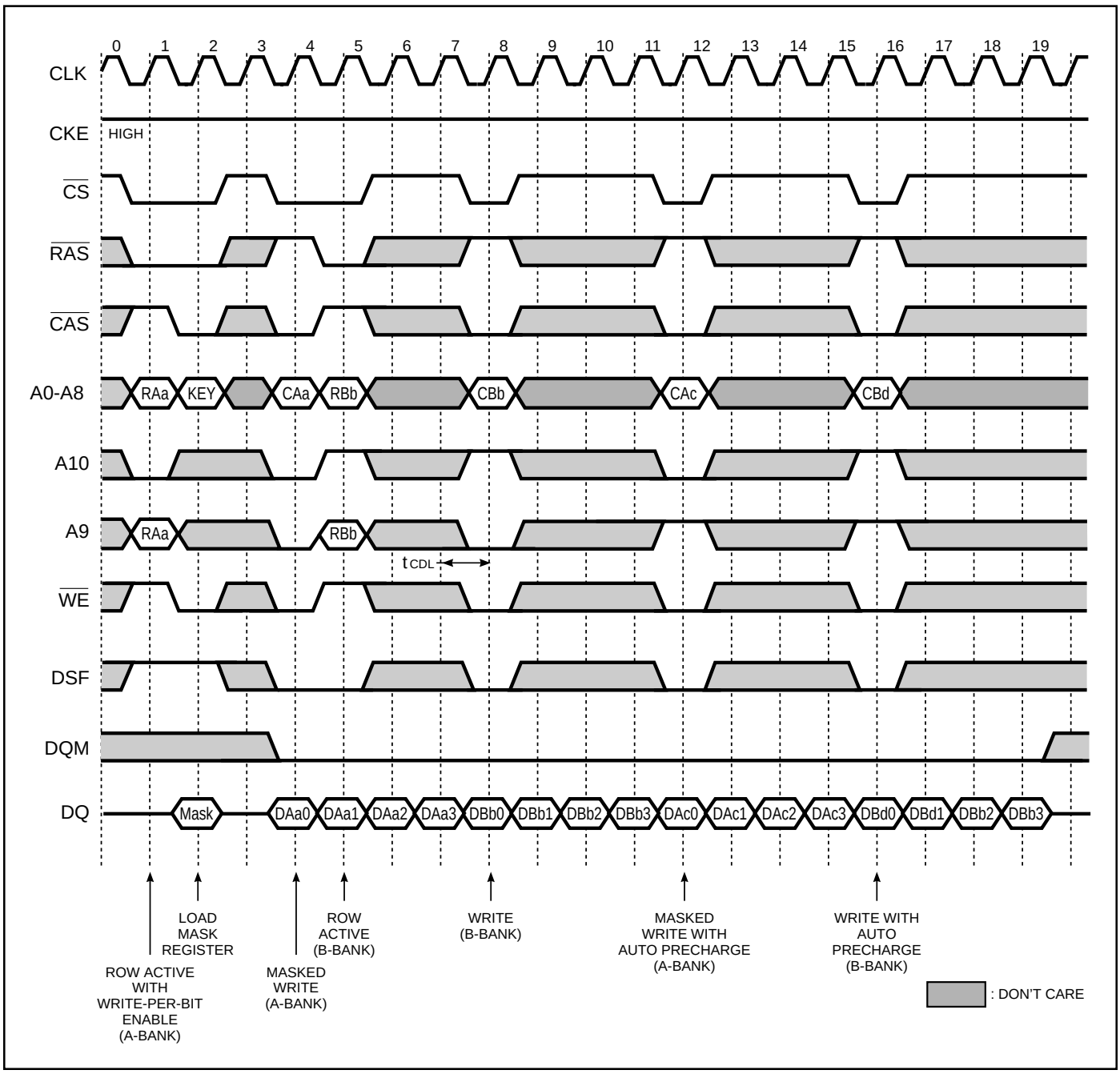
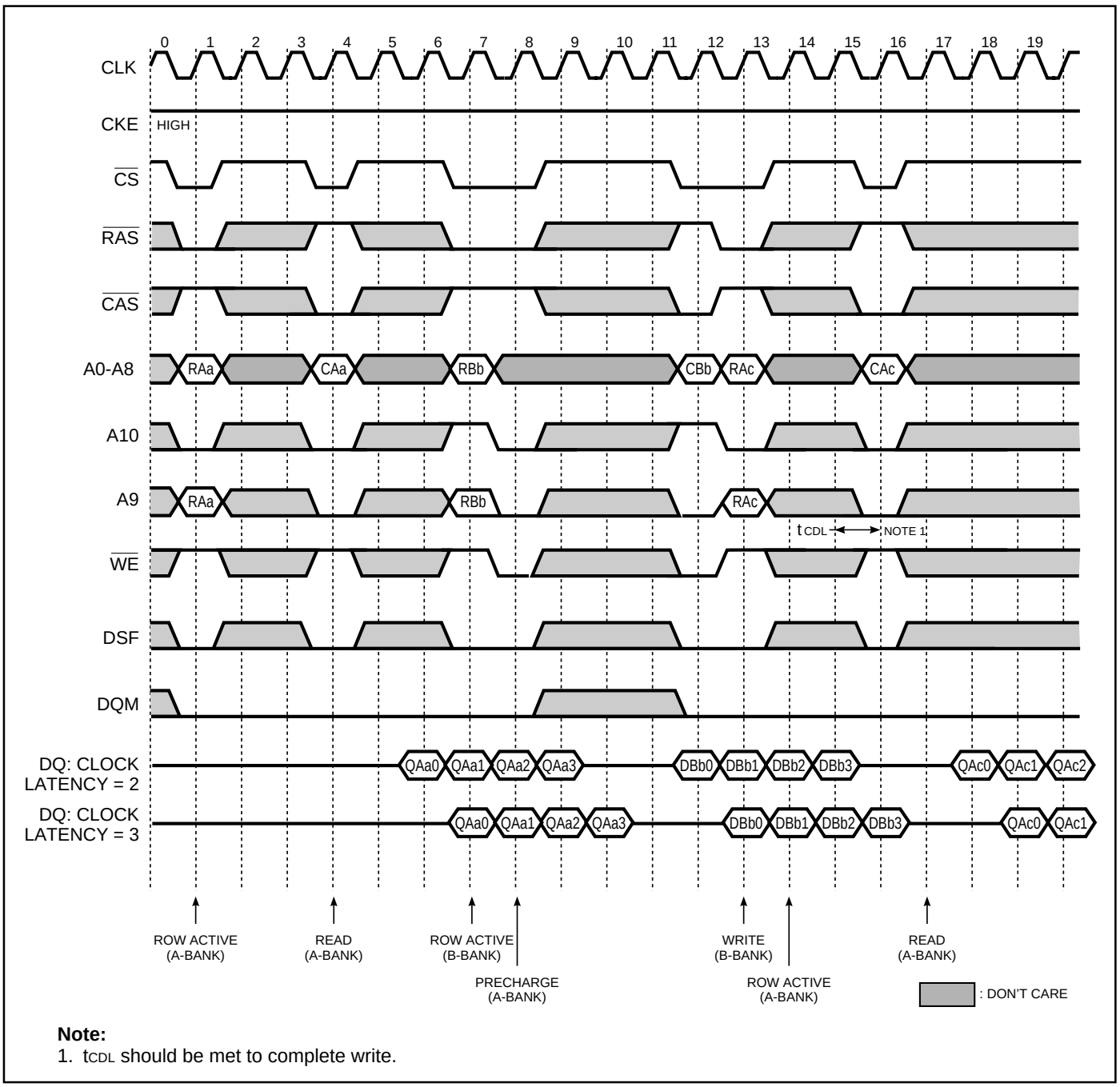
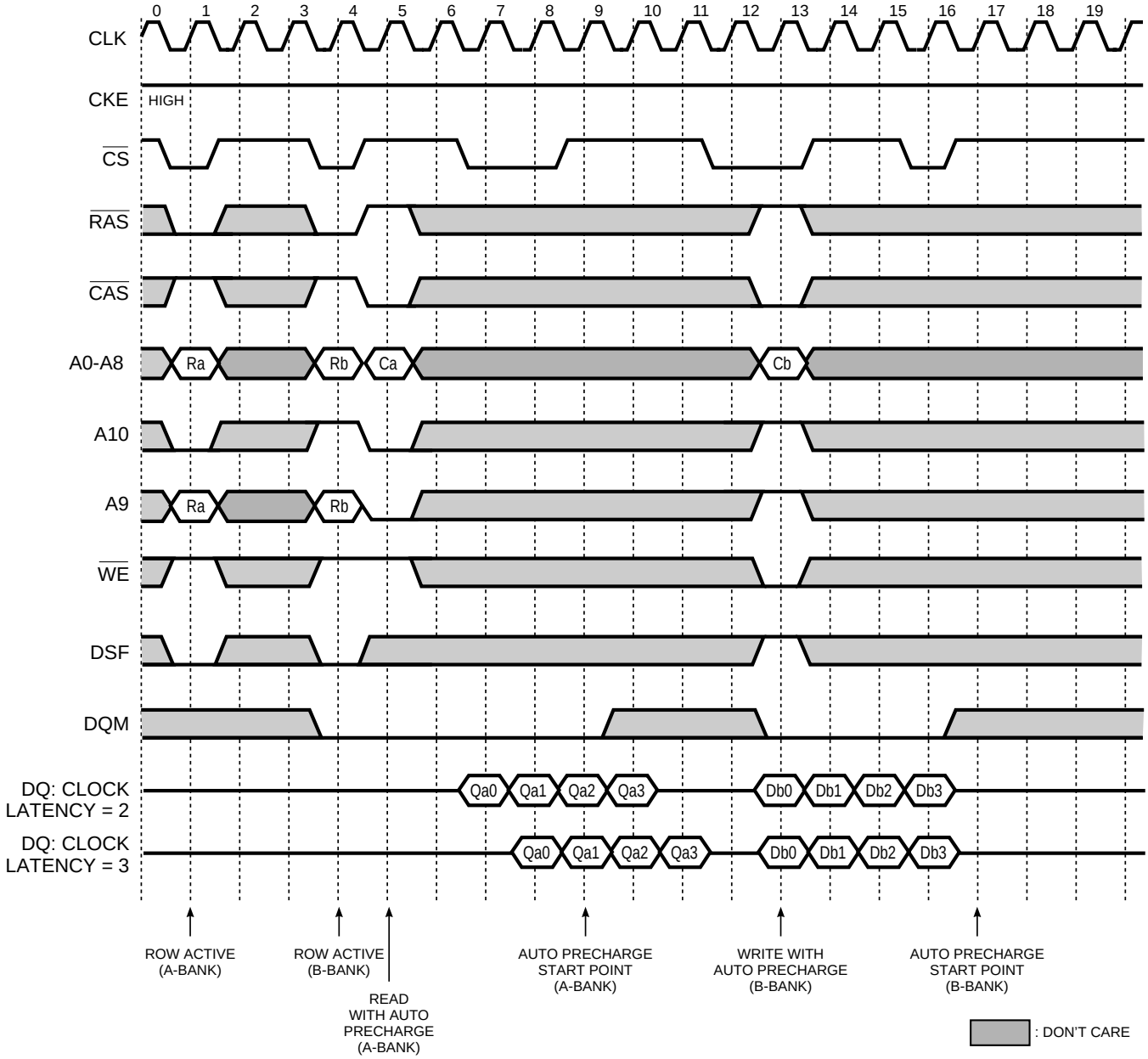


Figure 25. Page Write Cycle at Different Bank at Burst Length = 4



Note:
1. t_{CDL} should be met to complete write.

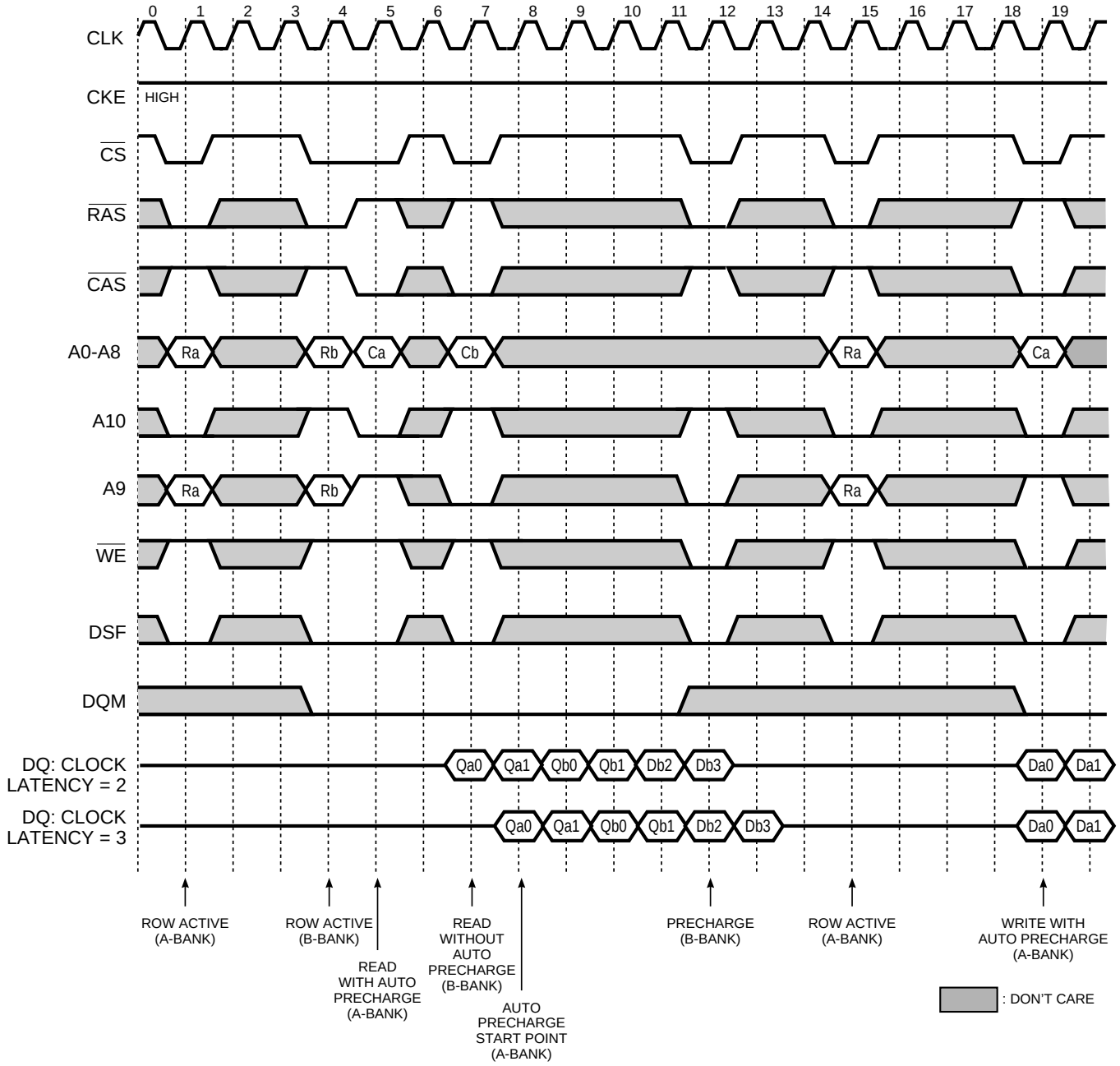
Figure 26. Read and Write Cycle at Different Bank at Burst Length = 4



Note:

1. t_{RDL} should be controlled to meet minimum t_{RAS} before internal precharge start (in the case of Burst Length = 1 and 2, BRSW mode and Block write).

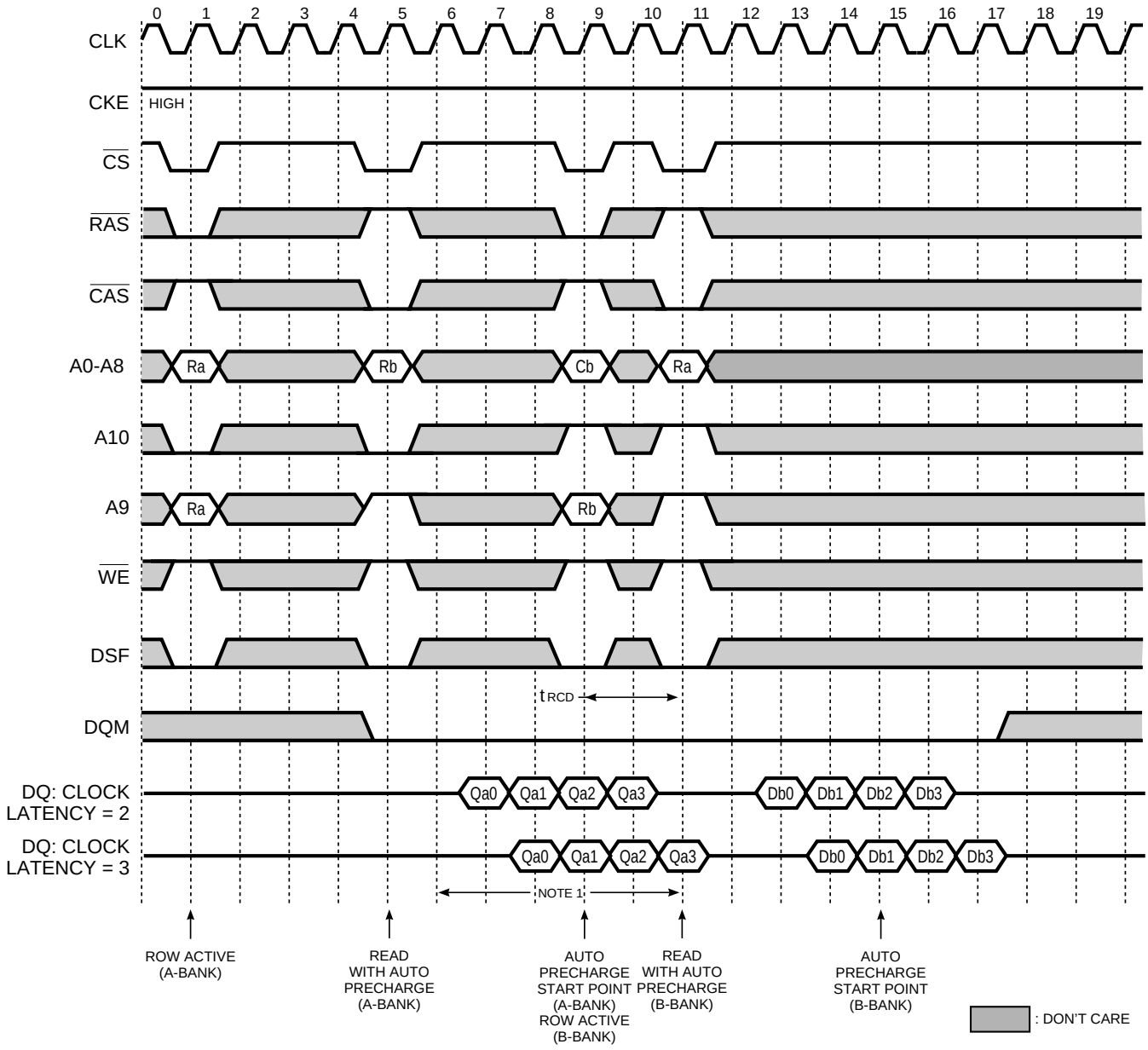
Figure 27. Read and Write Cycle with Auto Precharge at Burst Length = 4



Note:

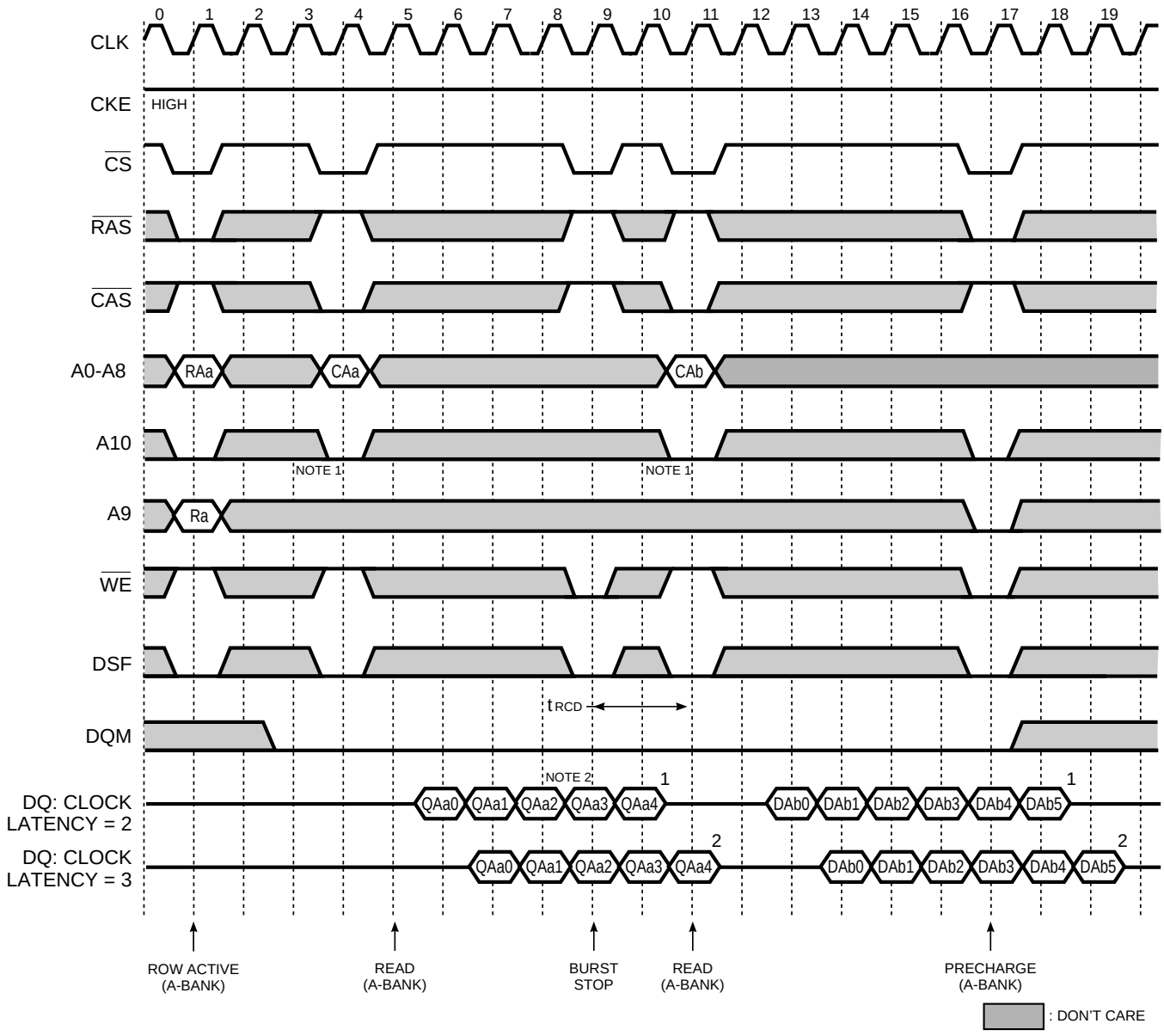
1. When Read (Write) command with auto precharge is issued at A-Bank after A and B Bank activation.
   — If Read (Write) command without auto precharge is issued at B-Bank before A Bank auto precharge starts, A Bank auto precharge will start at the next cycle of B Bank read command input point.
   — Any command can not be issued at A Bank during t_{RP} after A Bank auto precharge starts.

Figure 28. Read and Write Cycle with Auto Precharge II at Burst Length = 4



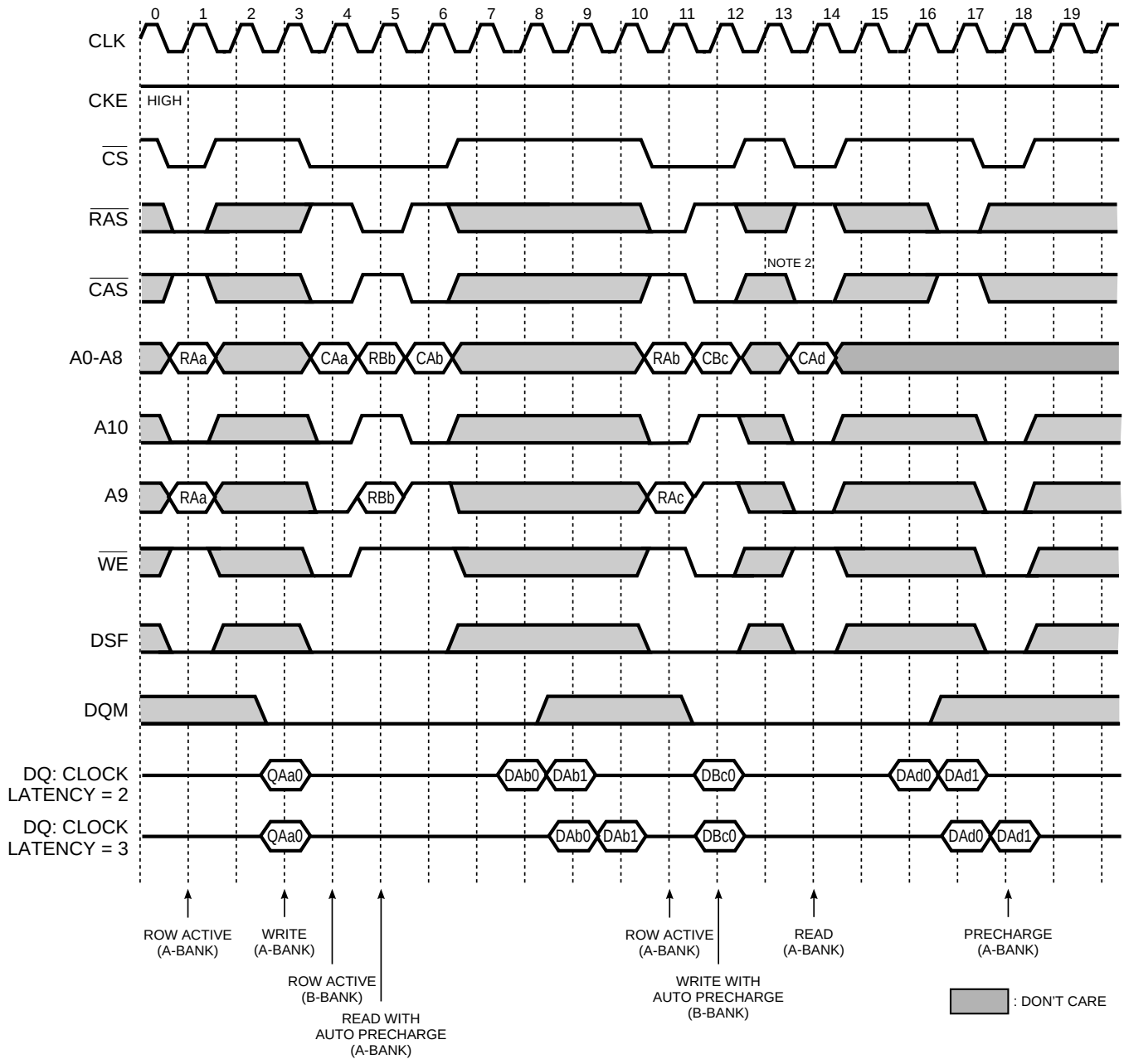
Note:
1. Any command to A Bank is not allowed in this period. t_{RP} is determined from at auto precharge start point.

Figure 29. Read and Write Cycle with Auto Precharge ••• at Burst Length = 4



Notes:
1. At full page mode, burst is wrap-around at the end of burst. So auto precharge is impossible.
2. About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt. both cases are illustrated above timing diagram. See the label 1,2 on them. But at burst write, Burst stop and $\overline{RAS}$ interrupt should be compared carefully. Refer to the timing diagram of "Full Page Write Burst Stop Cycle".
3. Burst stop is valid at full page mode.

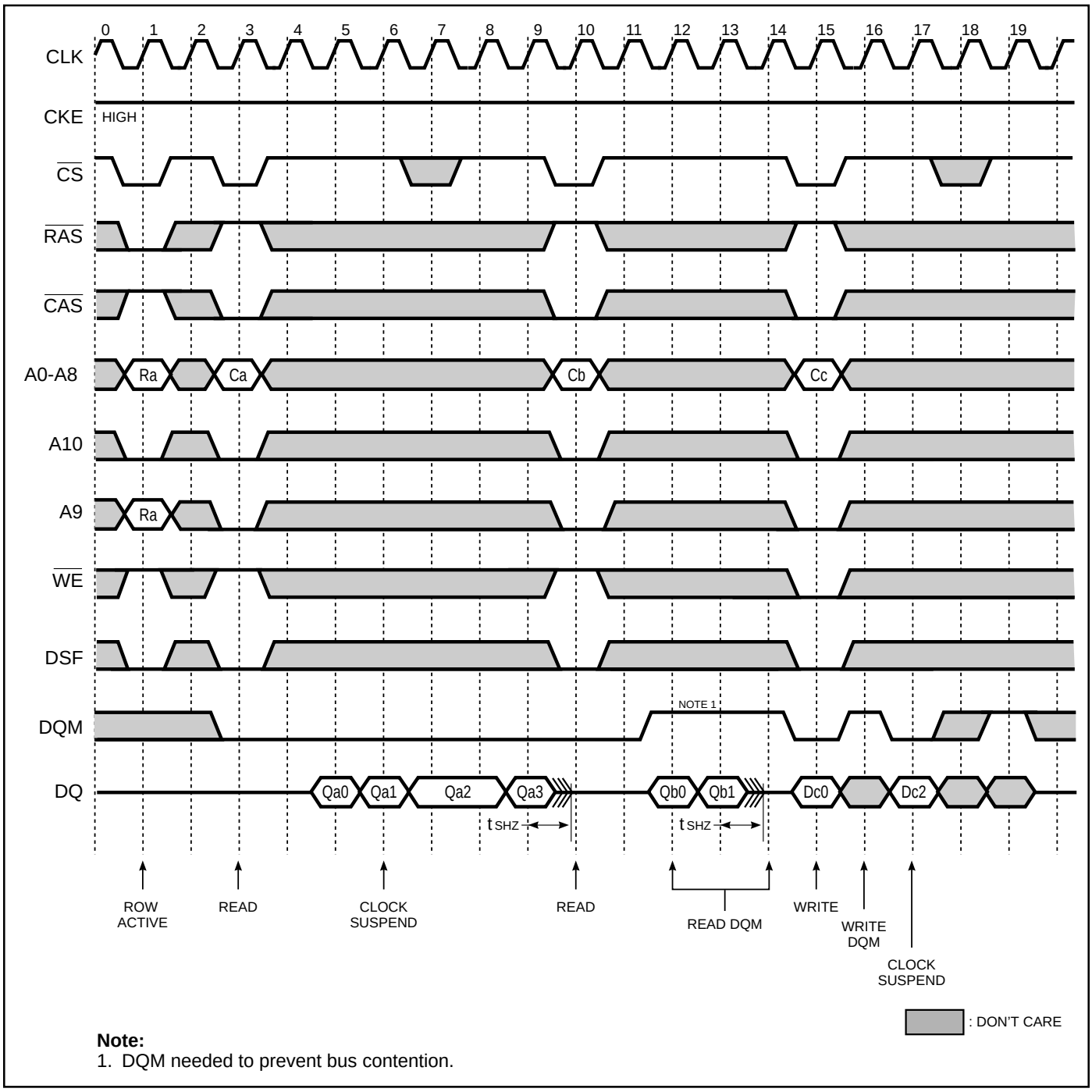
Figure 30. Read Interupted by Precharge Command and Read Burst Stop Cycle (at Full Page Only)



Notes:

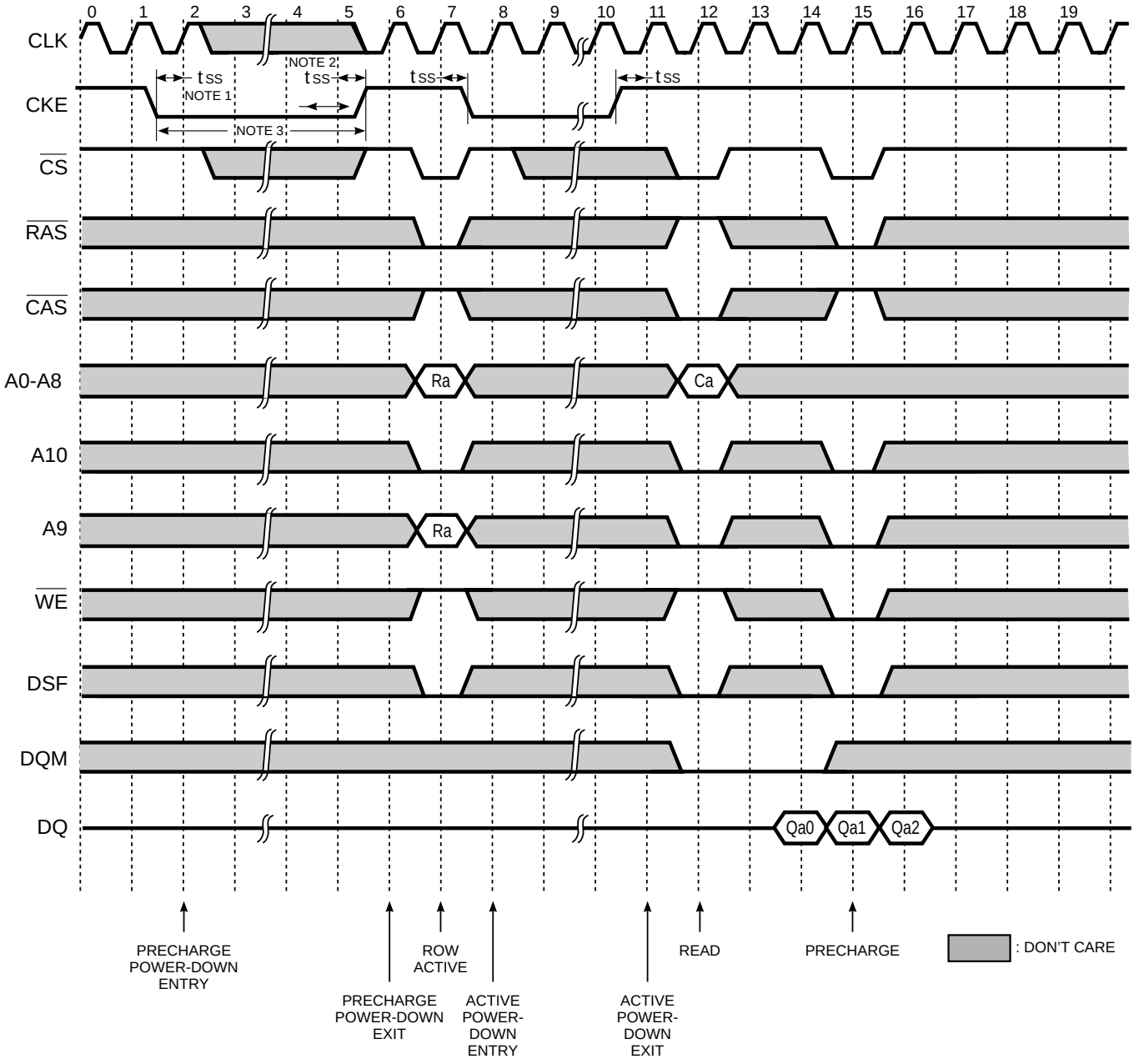
1. BRSW mode is enabled by setting A9 "High" at MRS (Mode Register Set). At the BRSW Mode, the burst length at write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated. Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command. The next cycle is also starts the precharge.
3. WPB function is also possible at BRSW mode.

Figure 32. Burst Read Single Bit Write Cycle at Burst Length = 2, BRSW



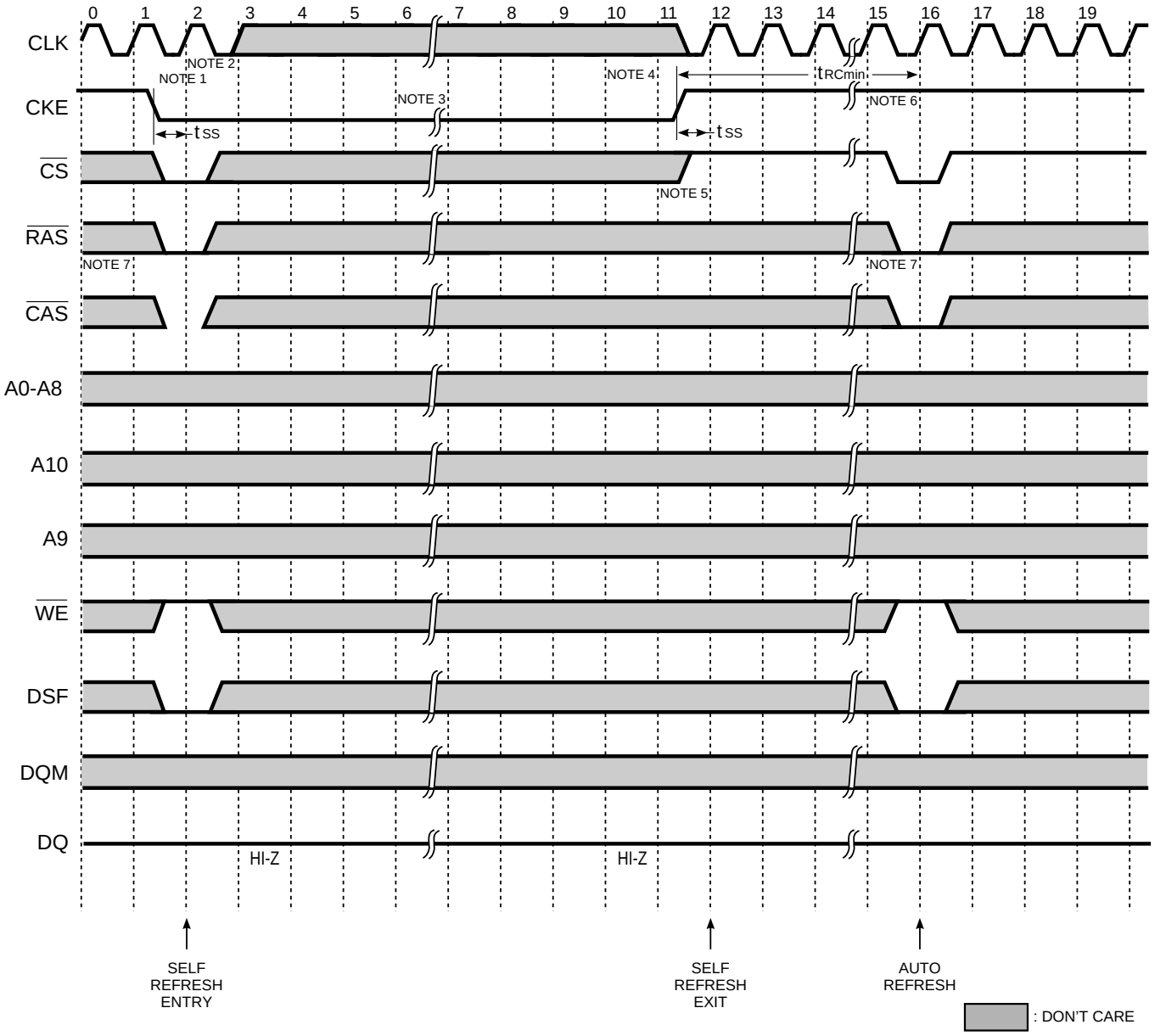
Note:
1. DQM needed to prevent bus contention.

Figure 33. Clock Suspension and DQM Operation Cycle at $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Notes:
1. All banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least "1CLK + tss" prior to Row active command.
3. Cannot violate minimum refresh specification (32 ms).

Figure 34. Active/Precharge Power Down Mode at $\overline{\text{CAS}}$ Latency = 2, Burst Length = 4



Notes:

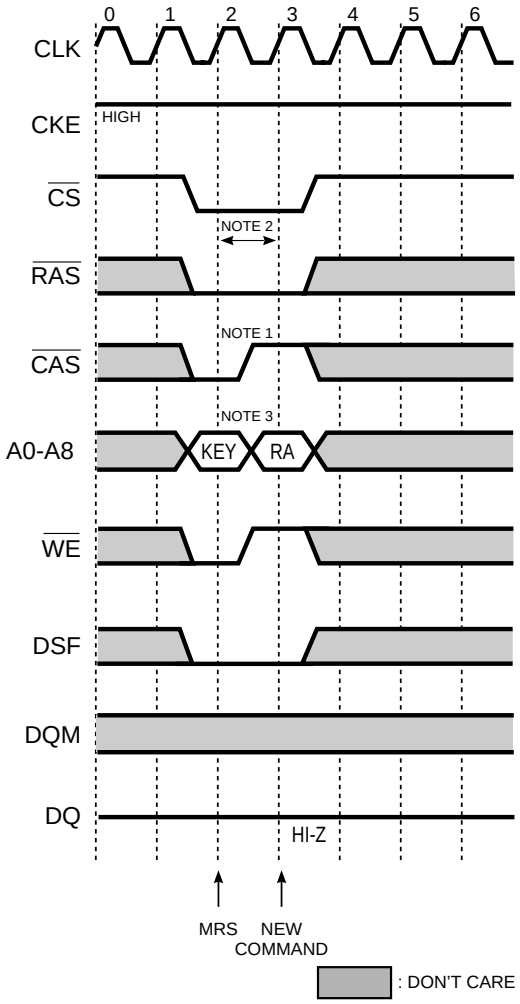
TO ENTER SELF REFRESH MODE

1. $\overline{CS}$, $\overline{RAS}$, and $\overline{CAS}$ with CKE should be low at the same clock cycle.
2. After one clock cycle, all the inputs including the system clock can be “Don’t Care” except for CKE.
3. The device remains in the self refresh mode as long as CKE stays “Low”. Once the device enters self refresh mode minimum t_{RAS} is required before exit from self refresh.

TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 2K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if system uses burst refresh.

Figure 35. Self Refresh Entry and Exit Cycle



Both bank precharge should be completed Mode Register Set cycle and auto refresh cycle.

Notes:
1. CS, raS, CAS, and WE activation and DSF of low at the same clock with address key will set internal mode register.
2. Minimum one clock cycle should be met before new RAS activation.
3. Please refer to Mode Register Set table.

Figure 36. Mode Register Set Cycle

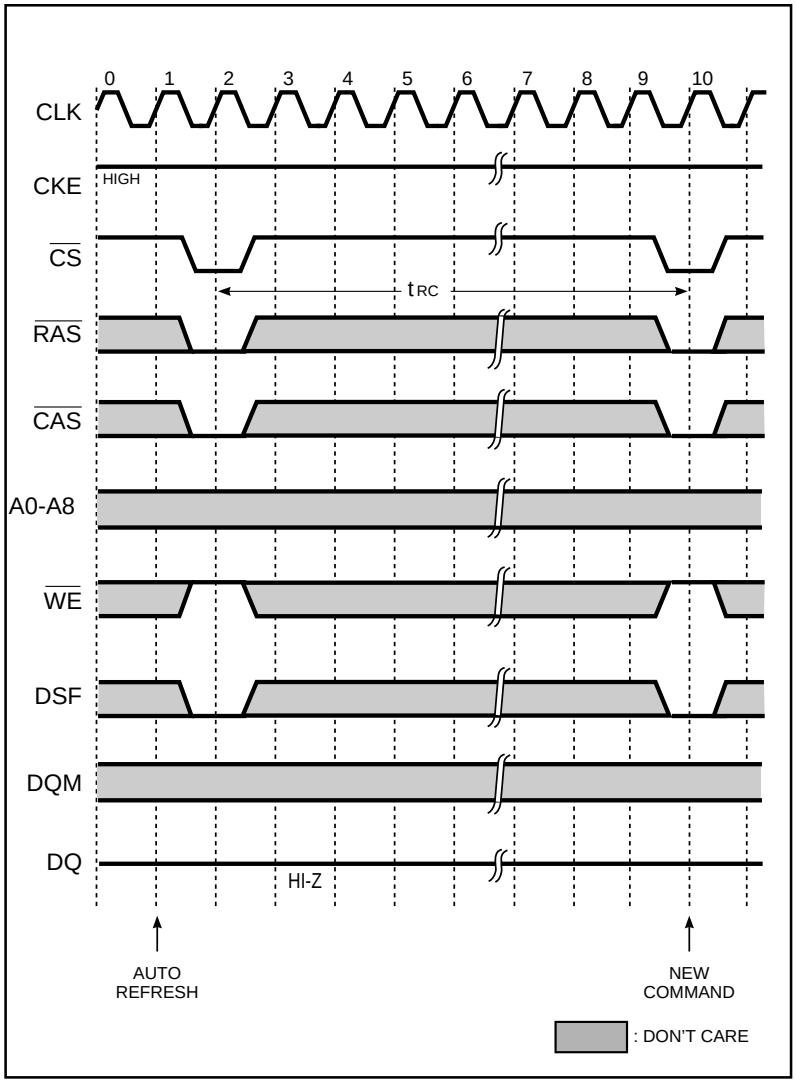


Figure 37. Auto Refresh Cycle

ORDERING INFORMATION

Commercial Range: 0°C to 70°C

Frequency	Speed (ns) Cycle Time	Order Part No.	Package
143 MHz	- 7	IS42G32256-7PQ	PQFP
125 MHz	- 8	IS42G32256-8PQ	PQFP
100 MHz	-10	IS42G32256-10PQ	PQFP

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