# IS42VS16400E-DIE

## 1 Meg Bits x 16 Bits x 4 Banks (64-MBIT) SYNCHRONOUS DYNAMIC RAM

**PRELIMINARY INFORMATION**
**APRIL 2007**

### FEATURES

- Clock frequency: 133, 100 MHz
- Fully synchronous; all signals referenced to a positive clock edge
- Internal bank for hiding row access/precharge
- Single 1.8V power supply
- LVTTL interface
- Programmable burst length
  – (1, 2, 4, 8, full page)
- Programmable burst sequence: Sequential/Interleave
- Self refresh modes
- 4096 refresh cycles every 64 ms
- Random column address every clock cycle
- Programmable $\overline{\text{CAS}}$ latency (2, 3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- Byte controlled by LDQM and UDQM
- Power Down and Deep Power Down Mode
- Partial Array Self Refresh
- Temperature Compensated Self Refresh
- Output Driver Strength Selection

### PIN DESCRIPTIONS

| | |
|---|---|
| A0-A11 | Address Input |
| BA0, BA1 | Bank Select Address |
| DQ0 to DQ15 | Data I/O |
| CLK | System Clock Input |
| CKE | Clock Enable |
| $\overline{\text{CS}}$ | Chip Select |
| $\overline{\text{RAS}}$ | Row Address Strobe Command |
| $\overline{\text{CAS}}$ | Column Address Strobe Command |
| $\overline{\text{WE}}$ | Write Enable |
| LDQM | Lower Bye, Input/Output Mask |
| UDQM | Upper Bye, Input/Output Mask |
| VDD | Power |

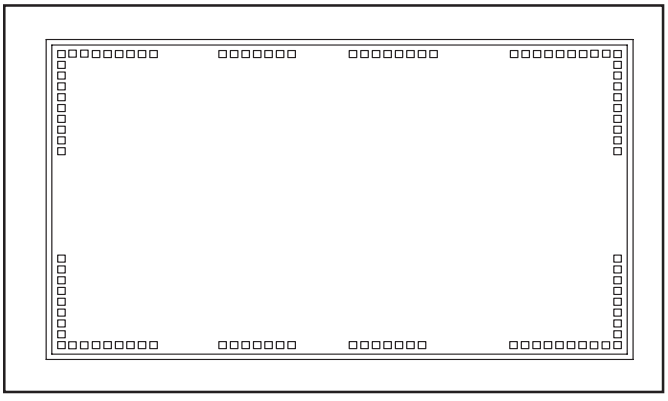
### OVERVIEW

*ISSI*'s 64Mb Synchronous DRAM IS42VS16400E is organized as 1,048,576 bits x 16-bit x 4-bank for improved performance. The synchronous DRAMs achieve high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input. Note: This is a summary datasheet specific to the die format. Please refer to the IS42VS16400E for complete device specifications.

### KEY TIMING PARAMETERS

| Parameter | -75 | -10 | Unit |
|---|---|---|---|
| Clk Cycle Time | | | |
| $\overline{\text{CAS}}$ Latency = 3 | 7.5 | 10 | ns |
| $\overline{\text{CAS}}$ Latency = 2 | 10 | 12 | ns |
| Clk Frequency | | | |
| $\overline{\text{CAS}}$ Latency = 3 | 133 | 100 | Mhz |
| $\overline{\text{CAS}}$ Latency = 2 | 100 | 83 | Mhz |
| Access Time from Clock | | | |
| $\overline{\text{CAS}}$ Latency = 3 | 6 | 8 | ns |
| $\overline{\text{CAS}}$ Latency = 2 | 8 | 9 | ns |

### BONDING DIAGRAM



| | |
|---|---|
| GND | Ground |
| VDDQ | Power Supply for DQ Pin |
| GNDQ | Ground for DQ Pin |
| NC | No Connection |