IS42VS16100E-DIE

512K Words x 16 Bits x 2 Banks (16-MBIT) SYNCHRONOUS DYNAMIC RAM

PRELIMINARY INFORMATION
NOVEMBER 2007

FEATURES

- Clock frequency: 133, 100, 83 MHz
- Power Supply: 1.8V
- Fully synchronous; all signals referenced to a positive clock edge
- Two banks can be operated simultaneously and independently
- Dual internal bank controlled by A11 (bank select)
- Programmable burst length (1, 2, 4, 8, full page)
- Programmable burst sequence: Sequential/Interleave
- Programmable full and half drive strength
- Programmable $\overline{CAS}$ latency (2, 3 clocks)
- 2048 refresh cycles every 32 ms
- Random column address every clock cycle
- Burst read/write and burst read/single write operations capability
- Byte controlled by LDQM and UDQM
- Auto Refresh and Self Refresh modes
- Partial Array Self-Refresh
- Power Down and Deep Power Down
- Pads located along edges of die

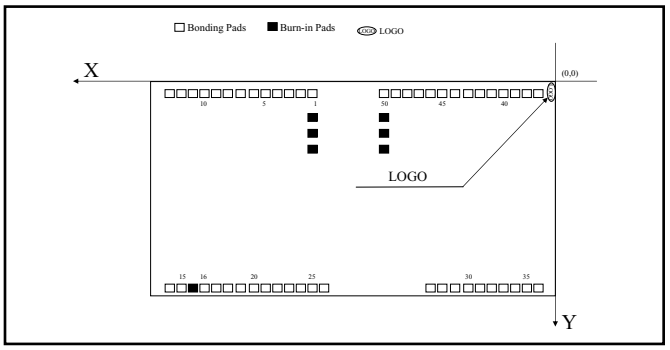
DESCRIPTION

ISSI's 16Mb Synchronous DRAM IS42VS16100E is organized as a 524,288-word x 16-bit x 2-bank for improved performance. The synchronous DRAMs achieve high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input. Note: This is a summary datasheet specific to the die format. Please refer to the IS42VS16100E datasheet for complete device specifications.

KEY TIMING PARAMETERS

Parameter	-7.5	-10	Unit
Clock Cycle Time			
$\overline{CAS}$ Latency = 3	7.5	10	ns
$\overline{CAS}$ Latency = 2	10	12	ns
Clock Frequency			
$\overline{CAS}$ Latency = 3	133	100	MHz
$\overline{CAS}$ Latency = 2	100	83	MHz
Access Time from Clock			
$\overline{CAS}$ Latency = 3	6	7	ns
$\overline{CAS}$ Latency = 2	8	8	ns

BONDING DIAGRAM



PIN DESCRIPTIONS

A0-A11	Address Input
A0-A10	Row Address Input
A11	Bank Select Address
A0-A7	Column Address Input
DQ0 to DQ15	Data DQ
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command
$\overline{WE}$	Write Enable
LDQM	Lower Bye, Input/Output Mask
UDQM	Upper Bye, Input/Output Mask
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for DQ Pin
V_{SSQ}	Ground for DQ Pin
NC	No Connection