# IS42S16100E-DIE

## 512K Words x 16 Bits x 2 Banks (16-MBIT) SYNCHRONOUS DYNAMIC RAM

**ADVANCED INFORMATION**
**JULY 2007**

### FEATURES

- Clock frequency: 166, 143 MHz
- Power supply: 3.3V
- Fully synchronous; all signals referenced to a positive clock edge
- Two banks can be operated simultaneously and independently
- Dual internal bank controlled by A11 (bank select)
- Programmable burst length – (1, 2, 4, 8, full page)
- Programmable burst sequence: Sequential/Interleave
- 2048 refresh cycles every 32 ms
- Random column address every clock cycle
- Programmable $\overline{\text{CAS}}$ latency (2, 3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- Byte controlled by LDQM and UDQM
- Pads located along edges

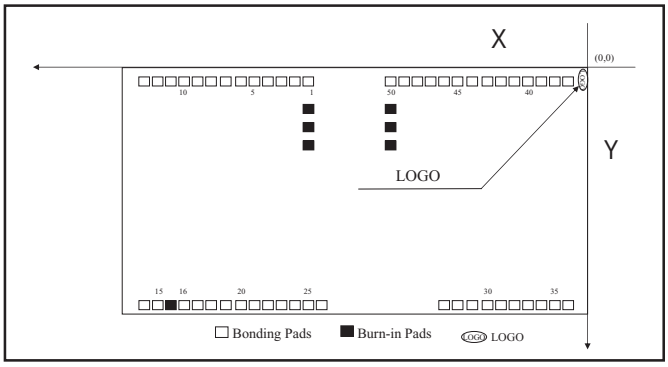
### DESCRIPTION

*ISSI*'s 16Mb Synchronous DRAM IS42S16100E is organized as a 524,288-word x 16-bit x 2-bank for improved performance. The synchronous DRAMs achieve high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input. Note: This is a summary datasheet specific to the die format. Please refer to the IS42S16100E for complete device specification.

### KEY TIMING PARAMETERS

| Parameter | -7 | -6 | Unit |
|---|---|---|---|
| Clock Cycle Time | | | |
| $\overline{\text{CAS}}$ Latency = 3 | 7 | 6 | ns |
| $\overline{\text{CAS}}$ Latency = 2 | 8 | 8 | ns |
| Clock Frequency | | | |
| $\overline{\text{CAS}}$ Latency = 3 | 143 | 166 | MHz |
| $\overline{\text{CAS}}$ Latency = 2 | 125 | 125 | MHz |
| Access Time from Clock | | | |
| $\overline{\text{CAS}}$ Latency = 3 | 5.5 | 5.5 | ns |
| $\overline{\text{CAS}}$ Latency = 2 | 6.0 | 6.0 | ns |

### BONDING DIAGRAM




### PIN DESCRIPTIONS

| | |
|---|---|
| A0-A11 | Address Input |
| A0-A10 | Row Address Input |
| A11 | Bank Select Address |
| A0-A7 | Column Address Input |
| DQ0 to DQ15 | Data DQ |
| CLK | System Clock Input |
| CKE | Clock Enable |
| $\overline{\text{CS}}$ | Chip Select |
| $\overline{\text{RAS}}$ | Row Address Strobe Command |
| $\overline{\text{CAS}}$ | Column Address Strobe Command |
| $\overline{\text{WE}}$ | Write Enable |
| LDQM | Lower Bye, Input/Output Mask |
| UDQM | Upper Bye, Input/Output Mask |
| VDD | Power |
| GND | Ground |
| VDDQ | Power Supply for DQ Pin |
| GNDQ | Ground for DQ Pin |
| NC | No Connection |