

IS62WV25616DALL/DBLL, IS65WV25616DALL/DBLL

256K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC SRAM

SEPTEMBER 2010

FEATURES

- High-speed access time: 35, 45, 55 ns
- CMOS low power operation
30 mW (typical) operating
6 μ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
1.65V--2.2V V_{DD} (IS62WV25616DALL)
2.5V--3.6V V_{DD} (IS62WV25616DBLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial and Automotive temperature support
- Lead-free available
- 2 CS option available

DESCRIPTION

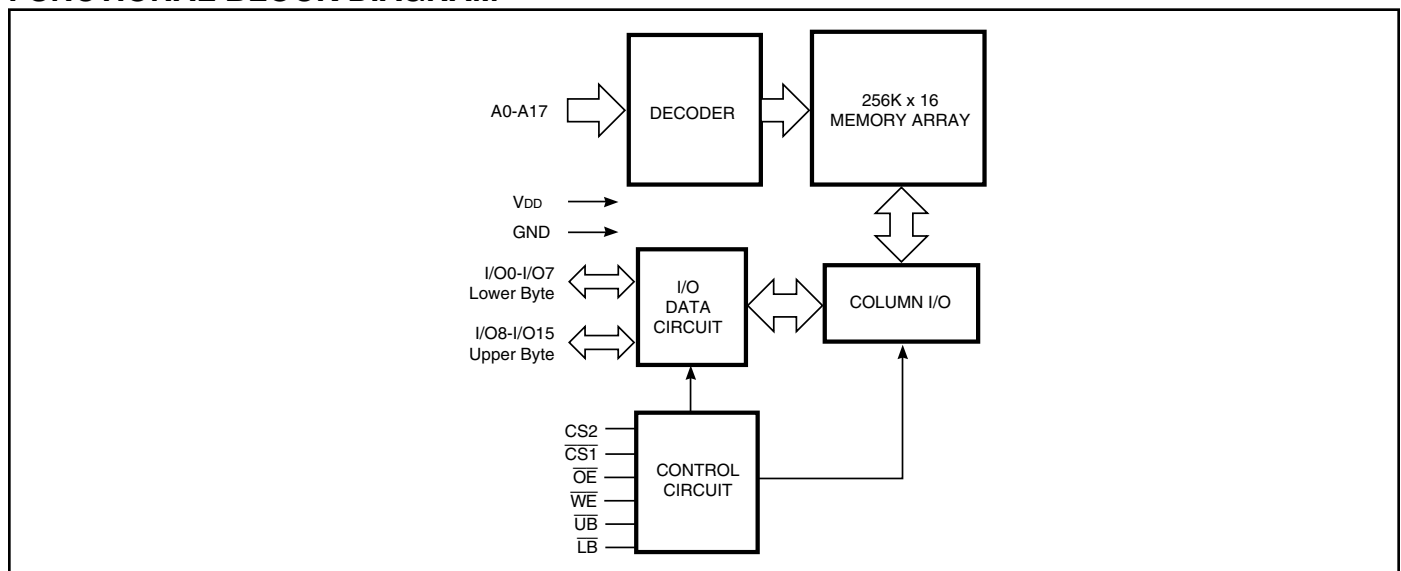
The *ISSI* IS62WV25616DALL/IS62WV25616DBLL are high-speed, low power, 4M bit SRAMs organized as 256K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when $CS2$ is LOW (deselected) or when $\overline{CS1}$ is LOW, $CS2$ is HIGH and both \overline{LB} and \overline{UB} are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory. A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

The IS62WV25616DALL/IS62WV25616DBLL are packaged in the JEDEC standard 44-Pin TSOP (TYPE II) and 48-pin mini BGA (6mmx8mm).

FUNCTIONAL BLOCK DIAGRAM



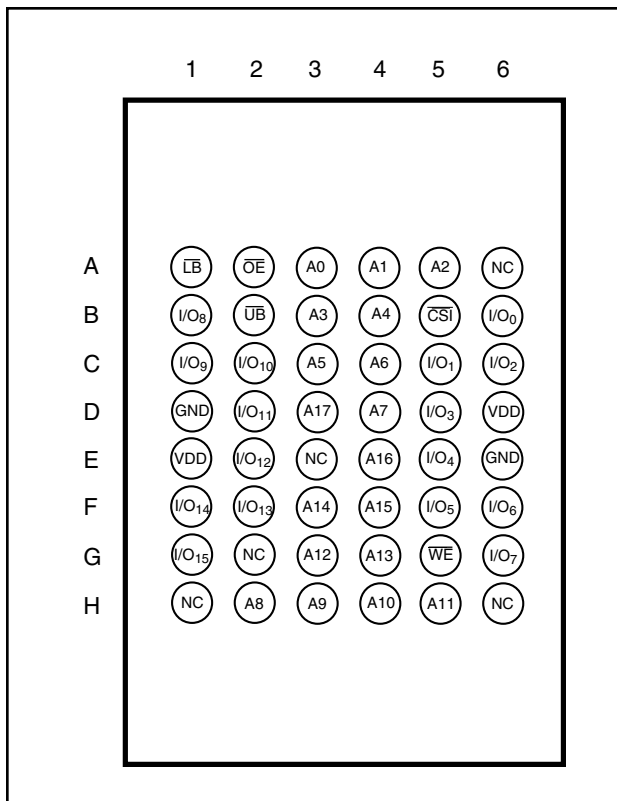
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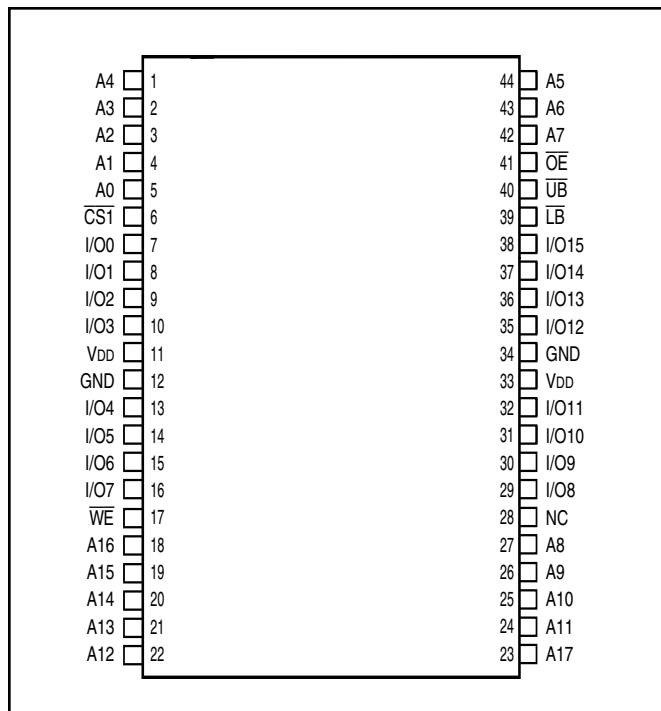
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN CONFIGURATIONS

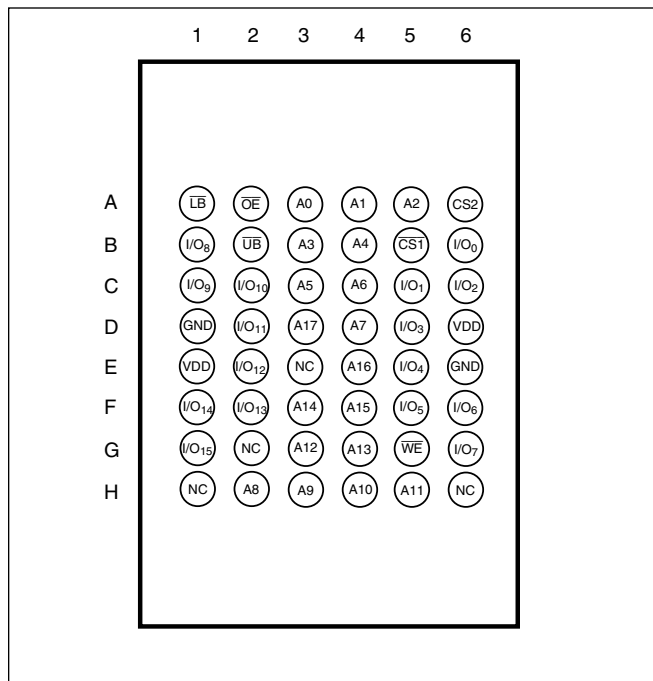
**48- ball mini BGA (6mm x 8mm)
(Package Code B)**



**44-Pin mini TSOP (Type II)
(Package Code T)**



**48-Pin mini BGA (6mm x 8mm)*
2 CS Option (Package Code B2)**



*Available upon request

PIN DESCRIPTIONS

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS1, CS2	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

TRUTH TABLE

Mode	\overline{WE}	$\overline{CS1}$	CS2	\overline{OE}	\overline{LB}	\overline{UB}	I/O PIN		V _{DD} Current
							I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	X	High-Z	High-Z	ISB1, ISB2
	X	X	L	X	X	X	High-Z	High-Z	ISB1, ISB2
	X	X	X	X	H	H	High-Z	High-Z	ISB1, ISB2
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I _{CC}
	H	L	H	H	X	L	High-Z	High-Z	I _{CC}
Read	H	L	H	L	L	H	DOUT	High-Z	I _{CC}
	H	L	H	L	H	L	High-Z	DOUT	
	H	L	H	L	L	L	DOUT	DOUT	
Write	L	L	H	X	L	H	DIN	High-Z	I _{CC}
	L	L	H	X	H	L	High-Z	DIN	
	L	L	H	X	L	L	DIN	DIN	

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to V _{DD} + 0.5	V
V _{DD}	V _{DD} Relates to GND	-0.3 to 4.0	V
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{I/O}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

AC TEST CONDITIONS

Parameter	Unit (2.3V-3.6V)	Unit (3.3V \pm 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to $V_{DD} - 0.3V$	0.4V to $V_{DD} - 0.3V$	0.4V to $V_{DD} - 0.3V$
Input Rise and Fall Times	1V/ ns	1V/ ns	1V/ ns
Input and Output Timing and Reference Level (V_{Ref})	$V_{DD} / 2$	$\frac{V_{DD}}{2} + 0.05$	0.9V
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2
R1 (Ω)	1005	1213	13500
R2 (Ω)	820	1378	10800
V_{TM} (V)	3.0V	3.3V	1.8V

AC TEST LOADS

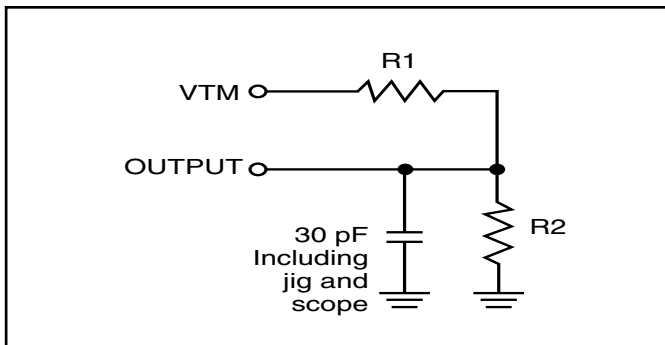


Figure 1.

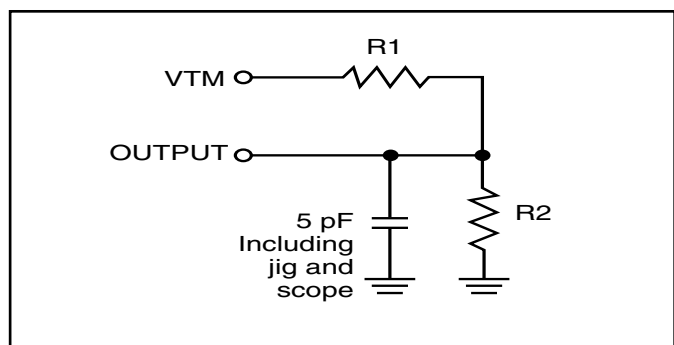


Figure 2.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

 $V_{DD} = 3.3V \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{DD} = \text{Min.}, I_{OH} = -1 \text{ mA}$	2.4	—	V
V_{OL}	Output LOW Voltage	$V_{DD} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$	—	0.4	V
V_{IH}	Input HIGH Voltage		2	$V_{DD} + 0.3$	V
V_{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I_{LI}	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$	-1	1	μA
I_{LO}	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled	-1	1	μA

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
 V_{IH} (max.) = $V_{DD} + 0.3V$ DC; V_{IH} (max.) = $V_{DD} + 2.0V$ AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

 $V_{DD} = 2.3V-3.6V$

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{DD} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$	1.8	—	V
V_{OL}	Output LOW Voltage	$V_{DD} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{DD} + 0.3$	V
V_{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I_{LI}	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$	-1	1	μA
I_{LO}	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled	-1	1	μA

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
 V_{IH} (max.) = $V_{DD} + 0.3V$ DC; V_{IH} (max.) = $V_{DD} + 2.0V$ AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

 $V_{DD} = 1.65V-2.2V$

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.1 \text{ mA}$	1.65-2.2V	1.4	—	V
V_{OL}	Output LOW Voltage	$I_{OL} = 0.1 \text{ mA}$	1.65-2.2V	—	0.2	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	$V_{DD} + 0.2$	V
$V_{IL}^{(1)}$	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
I_{LI}	Input Leakage	$GND \leq V_{IN} \leq V_{DD}$		-1	1	μA
I_{LO}	Output Leakage	$GND \leq V_{OUT} \leq V_{DD}$, Outputs Disabled		-1	1	μA

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width < 10 ns). Not 100% tested.
 V_{IH} (max.) = $V_{DD} + 0.3V$ DC; V_{IH} (max.) = $V_{DD} + 2.0V$ AC (pulse width < 10 ns). Not 100% tested.

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	V _{DD}	Speed
Commercial	0°C to +70°C	1.65V-2.2V	45ns
Industrial	-40°C to +85°C	1.65V-2.2V	55ns
Automotive	-40°C to +125°C	1.65V-2.2V	55ns

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	V _{DD} (45 ns)	V _{DD} (35 ns)
Commercial	0°C to +70°C	2.3V-3.6V	3.3V±5%
Industrial	-40°C to +85°C	2.3V-3.6V	3.3V±5%

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	V _{DD} (45 ns)
Automotive	-40°C to +125°C	2.3V-3.6V

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	-35		-45		-55		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max.,	Com.	—	20	—	15	—	15	mA
		I _{OUT} = 0 mA, f = f _{MAX}	Ind.	—	25	—	18	—	15	
		$\overline{CE} = V_{IL}$	Auto.	—	30	—	25	—	25	
		V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V	typ. ⁽²⁾	10						
I _{CC1}	Operating Supply Current	V _{DD} = Max.,	Com.	—	3	—	3	—	3	mA
		I _{OUT} = 0 mA, f = 0	Ind.	—	3	—	3	—	3	
		$\overline{CE} = V_{IL}$	Auto.	—	3	—	3	—	3	
		V _{IN} ≥ V _{DD} - 0.3V, or V _{IN} ≤ 0.4V								
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max.,	Com.	—	5	—	5	—	5	μA
		$\overline{CS1} \geq V_{DD} - 0.2V$,	Ind.	—	10	—	10	—	10	
		CS2 ≤ 0.2V,	Auto.	—	30	—	30	—	30	
		V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	typ. ⁽²⁾	2						
OR										
	ULB Control	V _{DD} = Max., $\overline{CS1} = V_{IL}$, CS2=V _{IH} V _{IN} ≤ 0.2V, f = 0; $\overline{UB} / \overline{LB} = V_{DD} - 0.2V$								

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

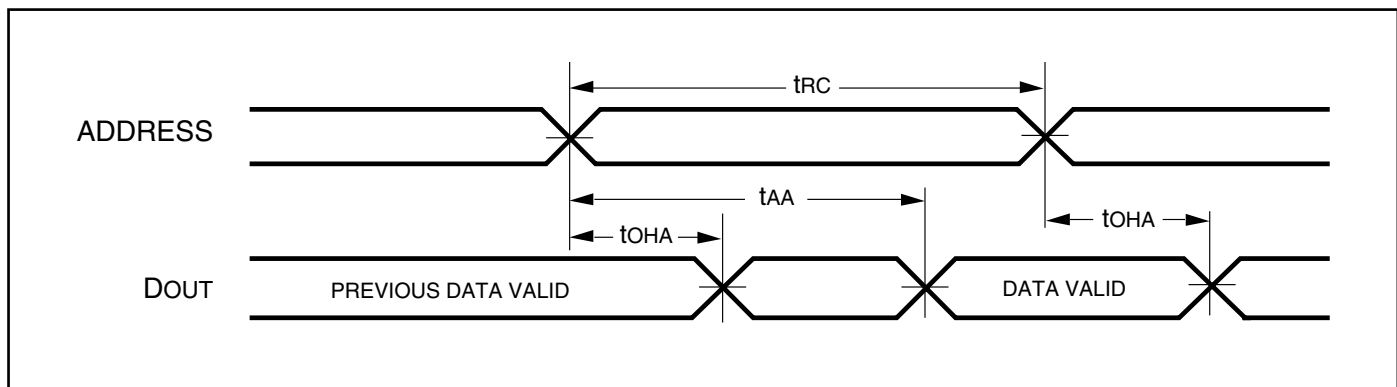
Symbol	Parameter	35 ns		45 ns		55 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t _{AA}	Address Access Time	—	35	—	45	—	55	ns
t _{OHA}	Output Hold Time	10	—	10	—	10	—	ns
t _{ACS1} /t _{ACS2}	CS1/CS2 Access Time	—	35	—	45	—	55	ns
t _{DOE}	OE Access Time	—	10	—	20	—	25	ns
t _{HZOE} ⁽²⁾	OE to High-Z Output	0	10	0	15	0	20	ns
t _{LZOE} ⁽²⁾	OE to Low-Z Output	3	—	5	—	5	—	ns
t _{HZCS1} /t _{HZCS2} ⁽²⁾	CS1/CS2 to High-Z Output	0	10	0	15	0	20	ns
t _{LZCS1} /t _{LZCS2} ⁽²⁾	CS1/CS2 to Low-Z Output	5	—	5	—	10	—	ns
t _{BA}	\overline{LB} , \overline{UB} Access Time	—	35	—	45	—	55	ns
t _{HZB}	\overline{LB} , \overline{UB} to High-Z Output	0	15	0	15	0	20	ns
t _{LZB}	\overline{LB} , \overline{UB} to Low-Z Output	0	—	0	—	0	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

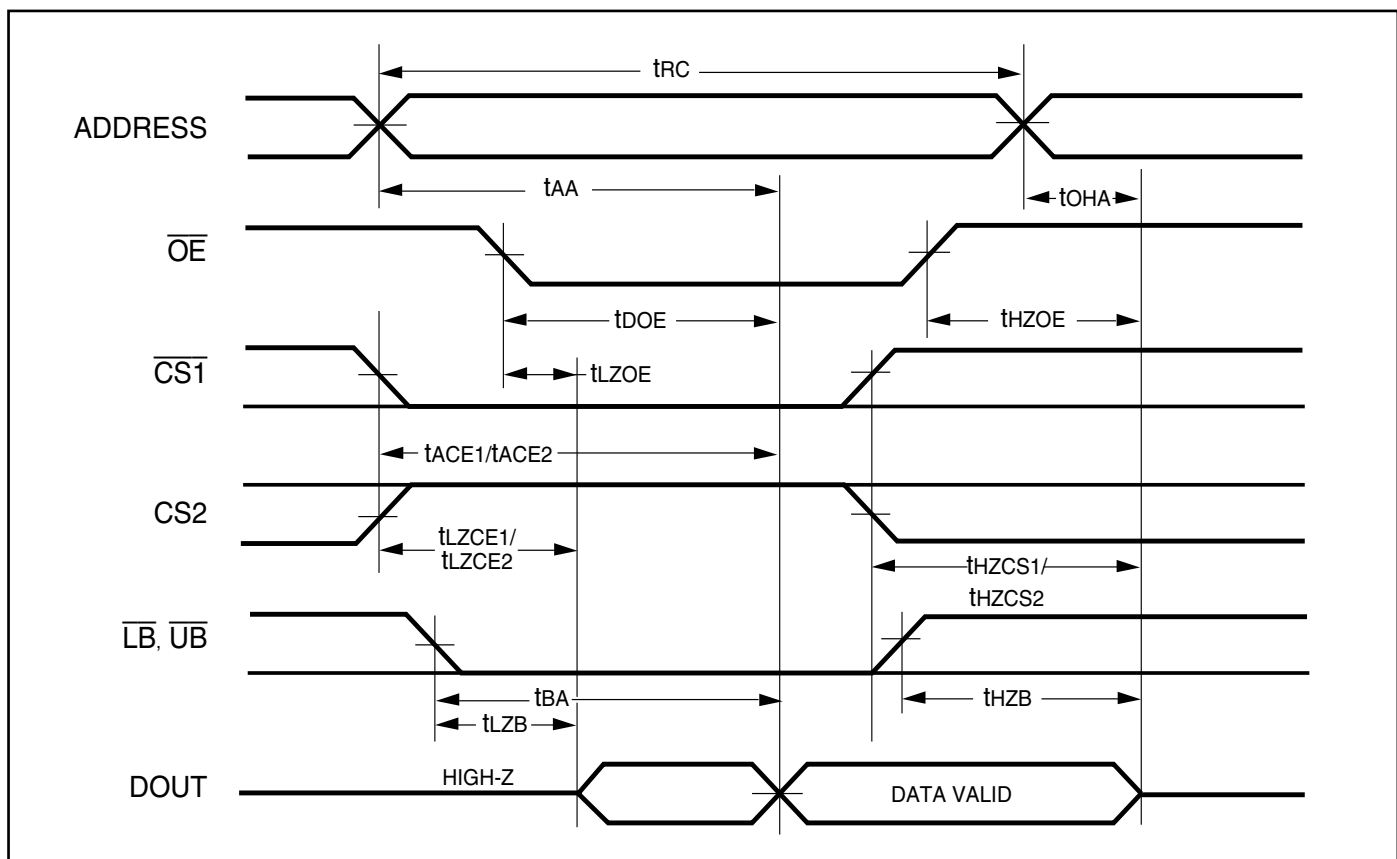
AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = \overline{WE} = V_{IH}$, \overline{UB} or $\overline{LB} = V_{IL}$)



AC WAVEFORMS

READ CYCLE NO. 2^(1,3) ($\overline{CS1}$, $CS2$, \overline{OE} , AND $\overline{UB}/\overline{LB}$ Controlled)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CS1}$, \overline{UB} , or $\overline{LB} = V_{IL}$. $CS2 = \overline{WE} = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

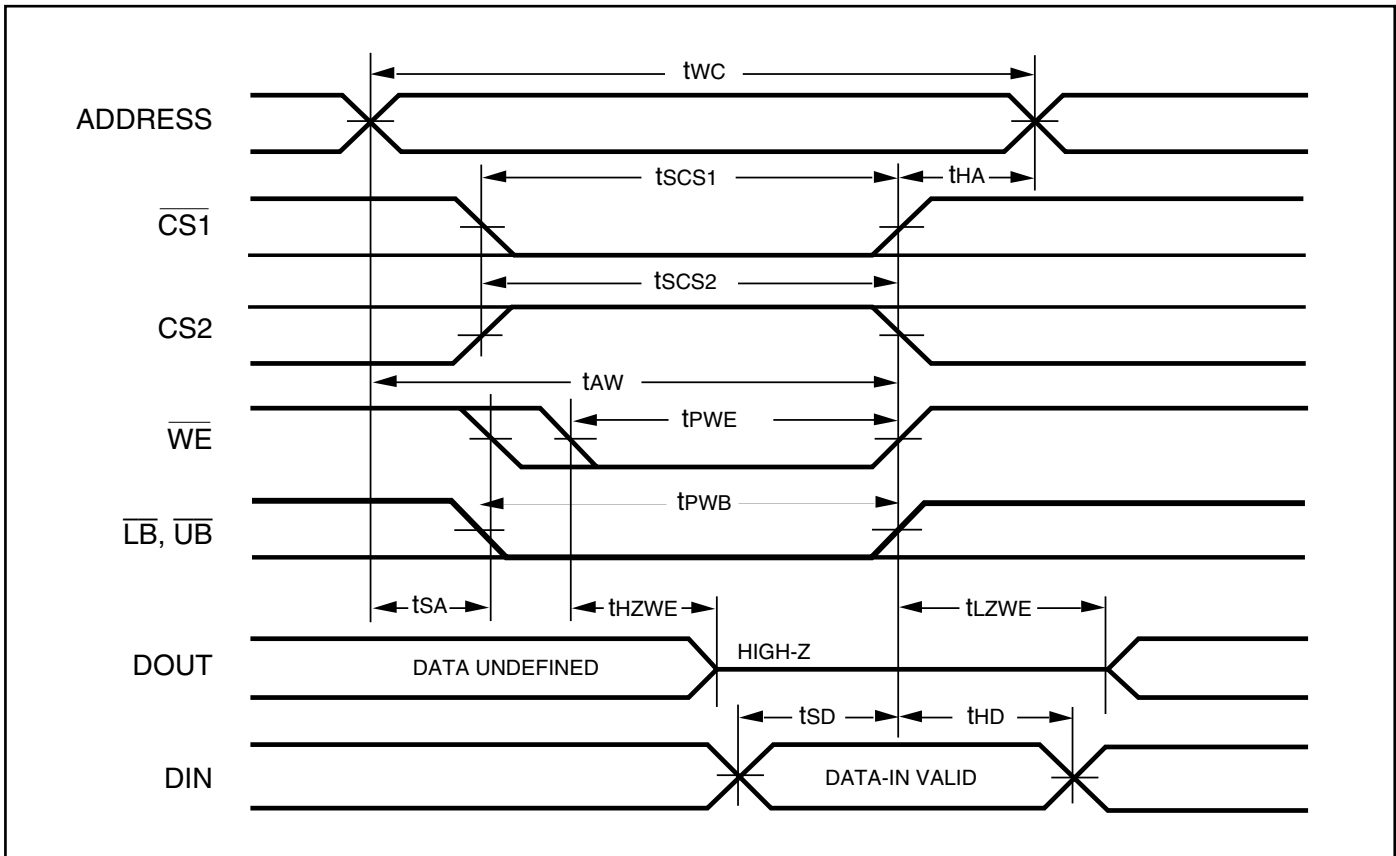
Symbol	Parameter	35 ns		45 ns		55 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t _{SCS1} /t _{SCS2}	$\overline{CS1}/\overline{CS2}$ to Write End	25	—	35	—	45	—	ns
t _{AW}	Address Setup Time to Write End	25	—	35	—	45	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	ns
t _{PWB}	\overline{LB} , \overline{UB} Valid to End of Write	25	—	35	—	45	—	ns
t _{PWE}	\overline{WE} Pulse Width	25	—	35	—	40	—	ns
t _{SD}	Data Setup to Write End	20	—	20	—	25	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{HZWE} ⁽³⁾	\overline{WE} LOW to High-Z Output	—	10	—	20	—	20	ns
t _{LZWE} ⁽³⁾	\overline{WE} HIGH to Low-Z Output	3	—	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V_{DD}-0.2V/V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and \overline{UB} or \overline{LB} , and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) ($\overline{CS1}$ Controlled, \overline{OE} = HIGH or LOW)

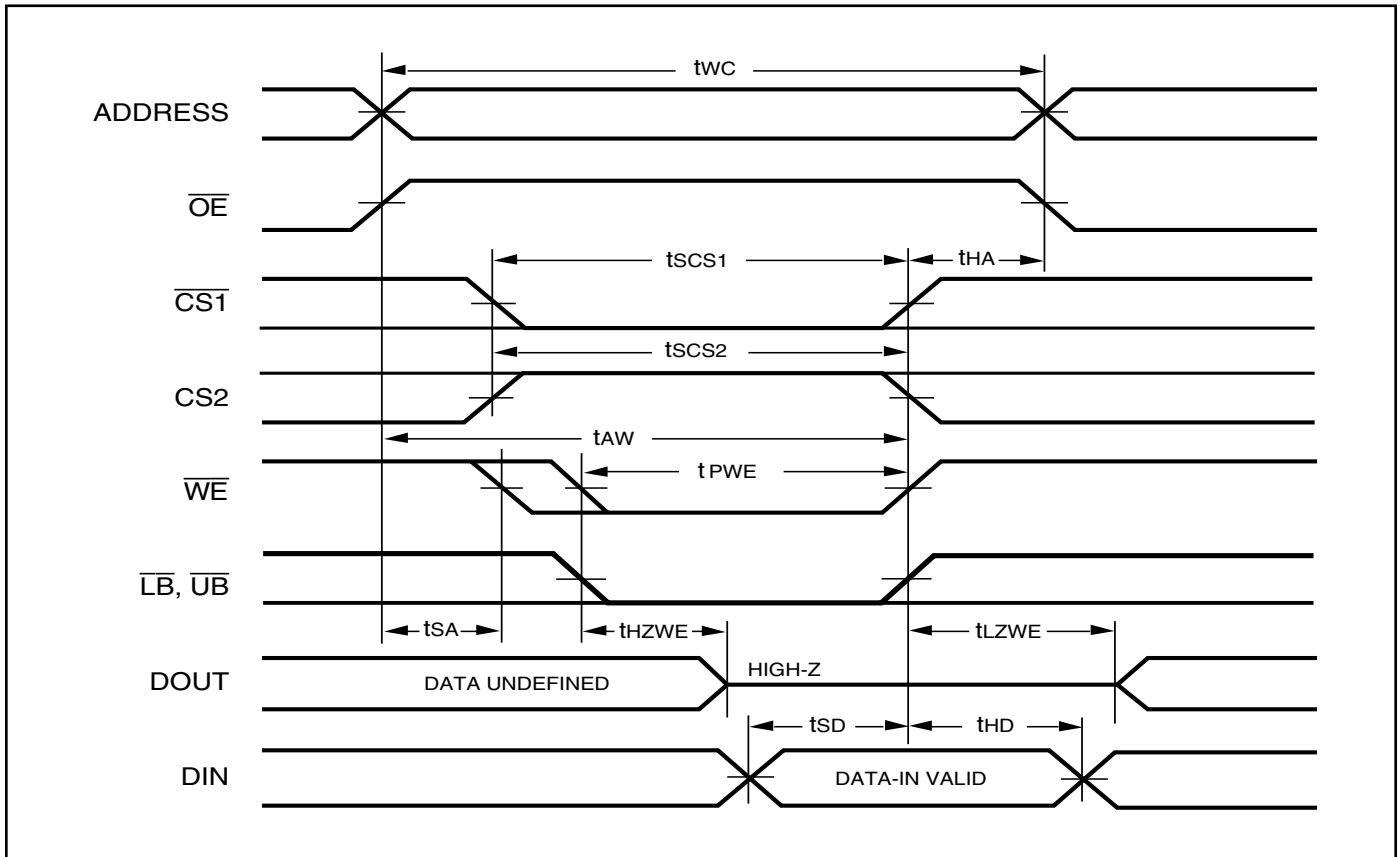


Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, $\overline{CS2}$ and \overline{WE} inputs and at least one of the \overline{LB} and \overline{UB} inputs being in the LOW state.
2. $WRITE = (\overline{CS1}) [(\overline{LB}) = (\overline{UB})] (\overline{WE})$.

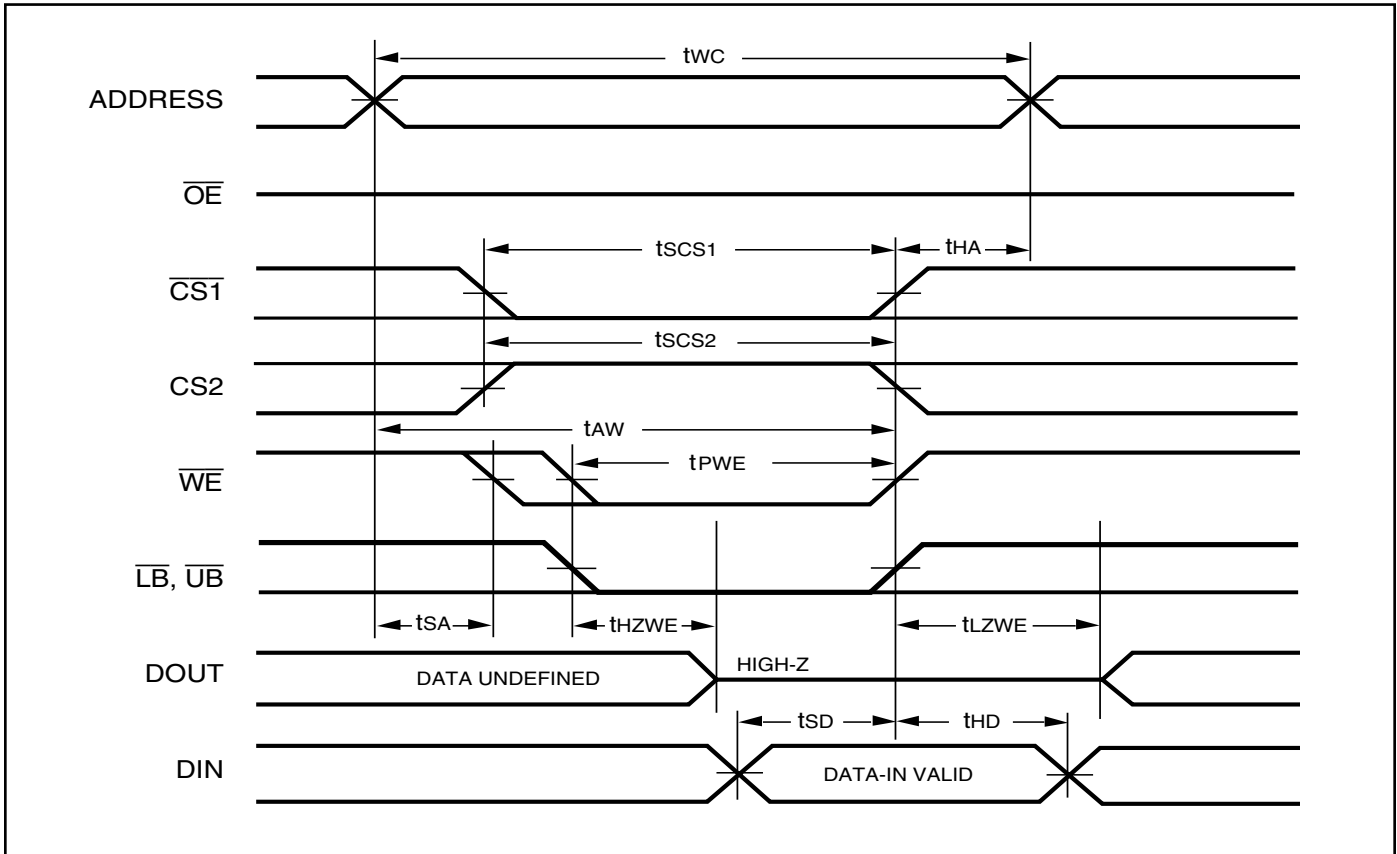
AC WAVEFORMS

WRITE CYCLE NO. 2 (\overline{WE} Controlled: \overline{OE} is HIGH During Write Cycle)



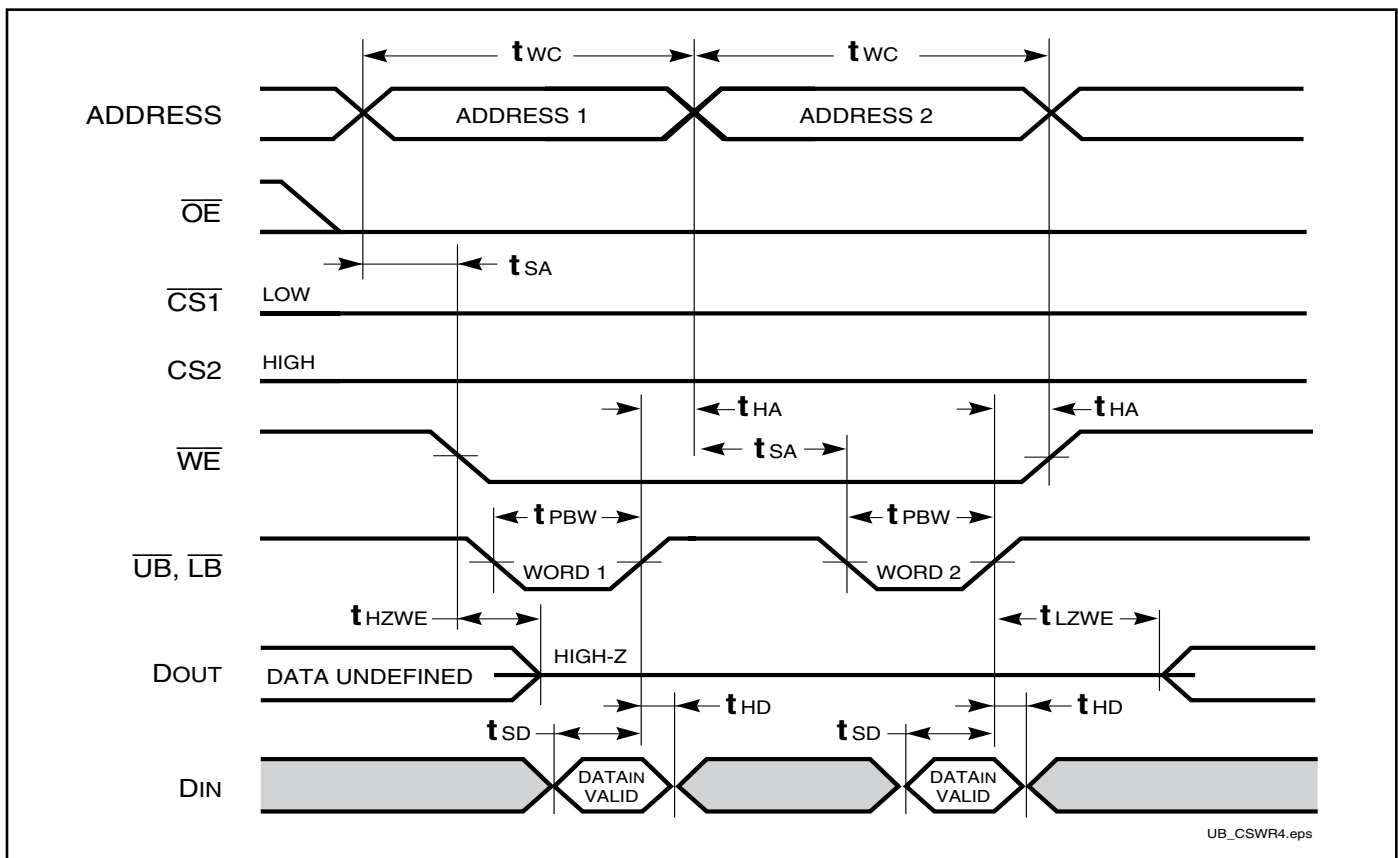
AC WAVEFORMS

WRITE CYCLE NO. 3 (\overline{WE} Controlled: \overline{OE} is LOW During Write Cycle)



AC WAVEFORMS

WRITE CYCLE NO. 4 ($\overline{UB}/\overline{LB}$ Controlled)

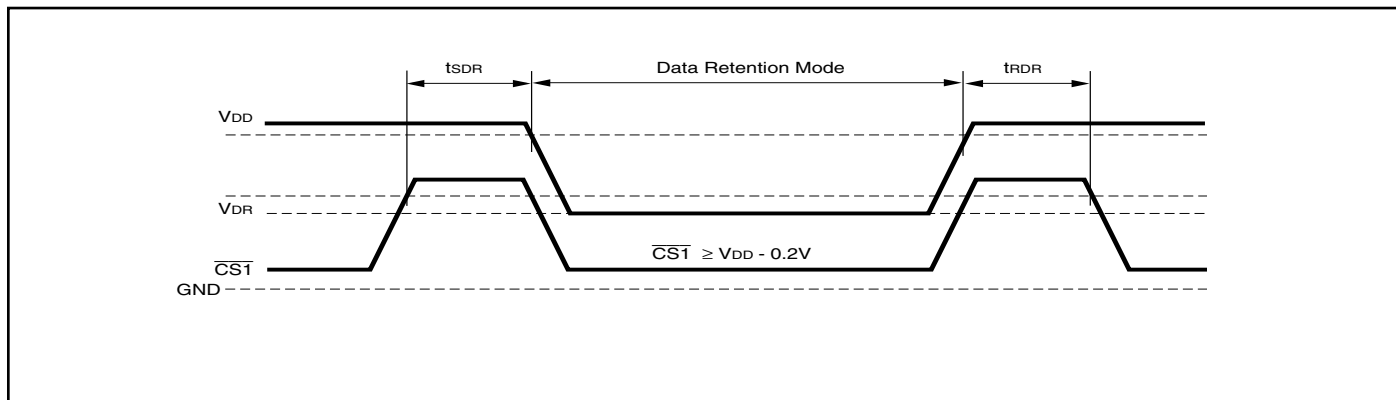


DATA RETENTION SWITCHING CHARACTERISTICS

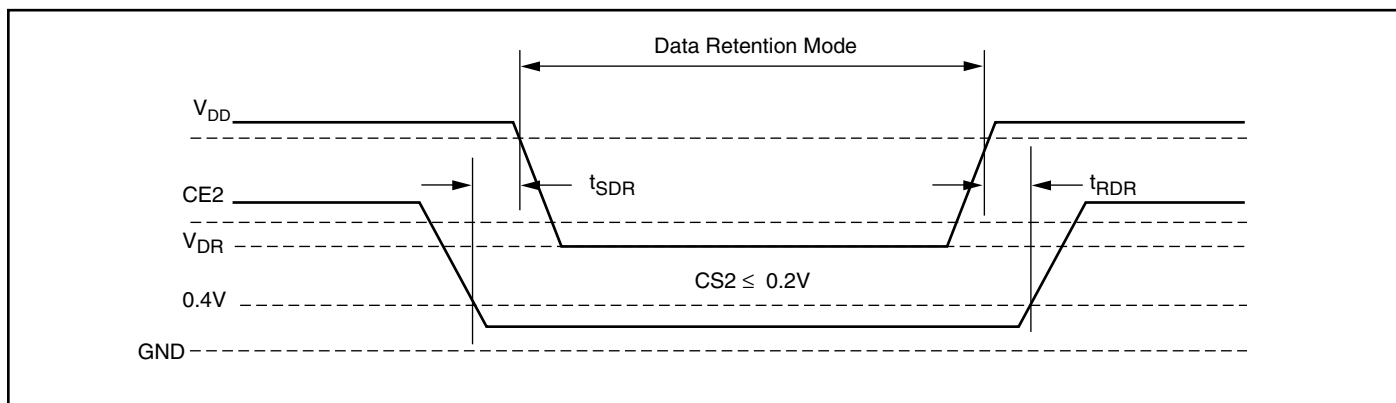
Symbol	Parameter	Test Condition	Min.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	See Data Retention Waveform	1.2	3.6	V
I _{DR}	Data Retention Current	V _{DD} = 1.2V, $\overline{CS1} \geq V_{DD} - 0.2V$	Com. Ind. Auto. typ. ⁽¹⁾	— — — 1	3 7 20 μA
t _{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t _{RDR}	Recovery Time	See Data Retention Waveform	t _{RC}	—	ns

Note: 1. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (CS2 Controlled)



ORDERING INFORMATION
IS62WV25616ALL (1.65V-2.2V)
Commercial Range: 0°C to +70°C

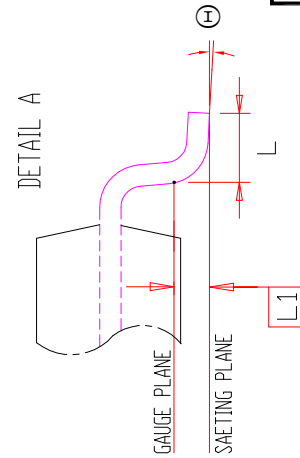
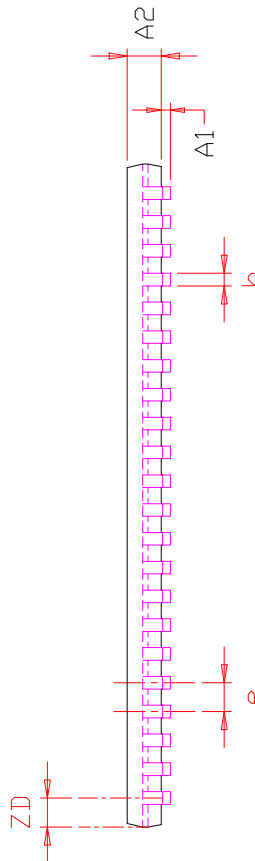
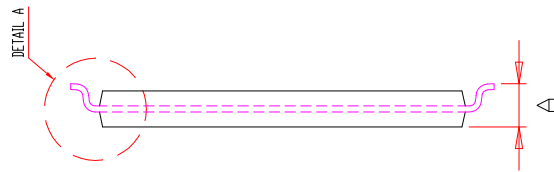
Speed (ns)	Order Part No.	Package
70	IS62WV25616DALL-55TL	TSOP, Lead-free

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV25616DALL-55TI	TSOP
	IS62WV25616DALL-55TLI	TSOP, Lead-free
55	IS62WV25616DALL-55BI	mini BGA (6mmx8mm)
	IS62WV25616DALL-55BLI	mini BGA (6mmx8mm), Lead-free

IS62WV25616BLL (2.3V - 3.6V)
Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62WV25616DBLL-45TI	TSOP
	IS62WV25616DBLL-45TLI	TSOP, Lead-free
45	IS62WV25616DBLL-45BI	mini BGA (6mmx8mm)
	IS62WV25616DBLL-45BLI	mini BGA (6mmx8mm), Lead-free
55	IS62WV25616DBLL-55TLI	TSOP, Lead-free



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e		0.80	BSC.		0.031	BSC.
L	0.40		0.69	0.016		0.027
L1		0.25	BSC.		0.010	BSC.
ZD		0.805	REF.		0.032	REF.
⊕	0		8°	0		8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



44L 400mil TSOP-2
Package Outline

F

REV.

DATE

06/04/2008

