Universal Standard Specification Series Serial EEPROM Series

Advantage Series Serial EEPROMs Microwire BUS

BR93C□□-10□U-1.8 family

No.10001EAT11

●Description

The BR93C46/56/66 series ICs are serial EEPROMs of 1K/2K/4Kbits, respectively, which feature low voltage operation and low power consumption, enabling compatibility with a wide range of applications. In addition, compact packages are available, contributing to end-product miniaturization.

●Features

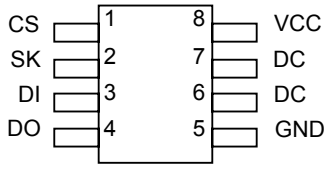
1) Microwire Bus interface
2) Single supply voltage: 1.8 to 5.5V
3) 16bit serial EEPROM
4) Automatic ERASE before WRITE and self-timed programming cycle
5) Ready /Busy status
6) 2MHz Clock Frequency, 10ms WRITE Time
7) Auto-increment of register address for READ mode
8) 1,000,000 WRITE/ERASE Cycles
9) 40-year data retention

●Pin configuration

Table1.Pin Configuration

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
DC	Don't Connect

8-lead SOIC



8-lead SOIC Rotated (1K JEDEC only)

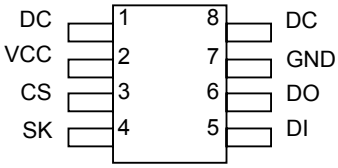


Figure1.Package

These EEPROMs utilize a three line serial interface consisting of Serial Data Input (DI), Serial Clock (SK), and Serial Data Output (DO)
After one READ instruction segment is received, if the Chip Select (CS) remains HIGH, the address pointer automatically cycles to the next higher register address, giving a continuous string of output data, depending on the device and the starting address.
When a WRITE or WRAL instruction is received, the previous data in the address locations are automatically overwritten, eliminating the need for an ERASE command.

When Chip Select (CS) is set to H after the WRITE command, the Status signal (Ready/Busy) becomes active at the Serial Data Output (DO) until the start bit of the next command. The Status signal is active when Chip Select (CS) is HIGH, and Serial Data Output (DO) pin outputs High – Z when Chip Select (CS) is LOW.

●Absolute maximum ratings

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		Min.	Max.	
Storage Temperature	T_{STG}	-65	125	℃
Output Range(Q=V_{OH} or Hi-Z)	V_{out}	-0.3	Vcc+0.3	V
Input range	V_{IN}	-0.3	V_{CC}+0.3	V
Supply Voltage	V_{CC}	-0.3	6.5	V

●Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Symbol	Ratings		Unit
		Min.	Max.	
Supply Voltage	V_{CC}	1.8	5.5	V
Ambient Operating Temperature	T_A	-40	85	℃

●Block Diagram

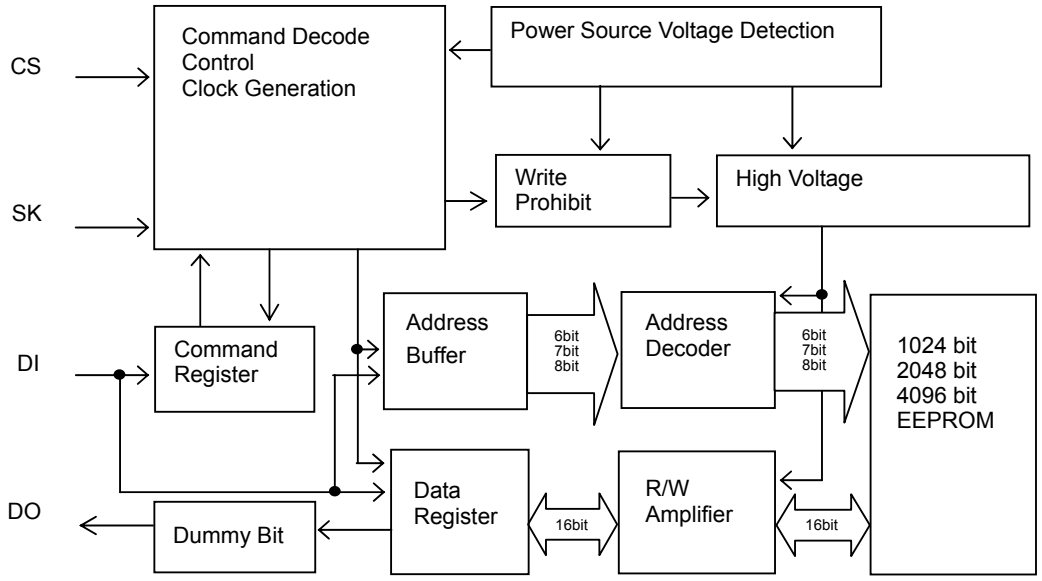


Figure 2: Block Diagram

●Electrical characteristics

Table 4: DC Characteristics (Unless otherwise specified, Ta=-40-85°C, V_{CC}=1.8-5.5V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max		
Supply Voltage	V_{CC}	1.8	-	5.5	V	
Supply Current	I_{CC}	-	-	2.0	mA	V_{CC}=5V, READ at f=1MHz
		-	-	2.0	mA	V_{CC}=5V, WRITE at f=1MHz
Standby Current	I_{SB}	-	-	10	μA	Vcc=2.7V,CS=0V
		-	-	30	μA	Vcc=5.0V,CS=0V
Input Leakage	I_{IL}	-	-	1.0	μA	$0V \leqq V_{IH} \leqq Vcc$
Output Leakage	I_{OL}	-	-	1.0	μA	$0 \leqq V_{OUT} \leqq V_{CC}$,DO in Hi-Z
Input Low Voltage Input High Voltage	V_{IL1} V_{IH1}	-0.3 2.0	- -	0.8 Vcc+0.3	V V	$4.0V \leqq V_{CC} \leqq 5.5V$
Input Low voltage Input High Voltage	V_{IL2} V_{IH2}	-0.3 $0.7V_{CC}$	- -	$0.2V_{CC}$ Vcc+0.3	V V	$V_{CC} \leqq 4.0$ V
Output Low Voltage Output High Voltage	V_{OL1} V_{OH1}	- 2.4	- -	0.4 -	V V	$2.7V \leqq V_{CC} \leqq 5.5V$ I_{OL}=2.1mA, I_{OH}=-0.4mA
Output Low Voltage Output High Voltage	V_{OL2} V_{OH2}	- V_{CC}-0.2	- -	0.2 -	V V	$1.8V \leqq V_{CC} \leqq 2.7V$ I_{OL}=0.15mA, I_{OH}=-100μA

Table 5: AC Characteristics (Unless otherwise specified, Ta=-40-85℃, V_{CC}=1.8-5.5V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max		
SK Clock Frequency	f_{SK}	0 0 0	- - -	2 1 0.25	MHz	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
SK High Time	t_{SKH} *1	250 250 1000	- - -	- - -	ns	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
SK Low Time	t_{SKL} *1	250 250 1000	- - -	- - -	ns	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
Minimum CS Low Time	t_{CS}	250 250 1000	- - -	- - -	ns	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
CS Set-up Time(relative to SK)	t_{CSS}	50 50 200	- - -	- - -	ns	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
DI Set-up Time(relative to SK)	t_{DIS}	100 100 400	- - -	- - -	ns	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
CS Hold Time(relative to SK)	t_{CSH}	0	-	-	ns	
DI Hold Time(relative to SK)	t_{DIH}	100 100 400	- - -	- - -	ns	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
Output Delay to “1”	t_{PD1}	-	-	250 250 1000	ns	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
Output Delay to “0”	t_{PD0}	-	-	250 250 1000	ns	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
CS to Status Vaid	t_{SV}	-	-	250 250 1000	ns	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
CS to Do in High Impedance	t_{DF}	-	-	100 100 400	ns	4.5V≦Vcc≦5.5V 2.7V≦Vcc≦5.5V 1.8V≦Vcc≦5.5V
Write Cycle time	t_{WP}	-	-	10	ms	
Endurance(5.0V,25℃)	-	1M	-	-	Write Cycle	

*1: t_{SKL}+ t_{SKH}≧1/fc

●Operating Instructions

The BR93□□ has a seven instruction set, shown in Tables 6 and 7. The timing charts depicted in Figures 3 to 10.
Input Data are clocked in from Serial Data Input (DI) at the rising edge of the Serial Clock (SK), while output data from the Serial Data Output (DO) toggles at the rising edge of the Serial Clock (SK) during READ mode.

The EEPROM recognizes the first 1 data received, after Chip Select (CS) goes HIGH, as the START bit. The input of many 0's before 1 will not make a difference – 1 will still be recognized as the START bit.

Table 6: Instruction Set (BR93C46)

Instruction	Start Bit	Op Code	Address*1						Data
READ	1	10	A5	A4	A3	A2	A1	A0	
EWEN	1	00	1	1	*	*	*	*	
ERASE	1	11	A5	A4	A3	A2	A1	A0	
WRITE	1	01	A5	A4	A3	A2	A1	A0	D15～D0
ERAL	1	00	1	0	*	*	*	*	
WRAL	1	00	0	1	*	*	*	*	D15～D0
EWDS	1	00	0	0	*	*	*	*	

*1: * = Inconsequential bit

Table 7: Instruction Set (BR93C56 and BR93C66)

Instruction	Start Bit	Op Code	Address*1, *2								Data
READ	1	10	A7	A6	A5	A4	A3	A2	A1	A0	
EWEN	1	00	1	1	*	*	*	*	*	*	
ERASE	1	11	A7	A6	A5	A4	A3	A2	A1	A0	
WRITE	1	01	A7	A6	A5	A4	A3	A2	A1	A0	D15～D0
ERAL	1	00	1	0	*	*	*	*	*	*	
WRAL	1	00	0	1	*	*	*	*	*	*	D15～D0
EWDS	1	00	0	0	*	*	*	*	*	*	

*1: * = Inconsequential bit
*2: Address bit A7 is not decoded by the BR93C56.

●Function Description

READ
The addressed 16 bits of data are clocked out after the READ instruction is received. During clocking of the 11th(1) bit the clock is HIGH and the EEPROM outputs '0' (dummy 0) as a sign to begin data output.
This device has an auto-increment feature that provides the whole memory array data using just one READ command.
It is recommended that Chip Select (CS) is HIGH and the Serial Clock (SK) keep clocking, since the EEPROM will output the next address data following the addressed 16 bits of data.

EWEN
The unit is in disable mode after power ON.
The EWEN instruction must precede any WRITE commands. After EWEN is executed the EEPROM will be in enable mode until power OFF or EWDS instruction is received. Neither the EWEN nor the EWDS instruction has any effect on the READ instruction. The state (H or L) of the Serial Data Input (DI) after the 6th clock of the Serial Clock (SK) doesn't matter, either. Therefore, it is recommended that eight more Serial Clock (SK) signals be inputted.

EWDS
This command puts the EEPROM into disable mode – similar to the status after power ON. The READ command can be preceded even in disable mode. It is recommended that the EWDS command be executed after any WRITE commands in order to prevent inadvertent writing. The state (H or L) of Serial Data Input (DI) after the 6th clock of the Serial Clock (SK) does not matter. Therefore, the inputting of eight more Serial Clock (SK) signals is recommended as well.

ERASE
The ERASE command writes '1' to all bits in the specified address. Between the rising edge of the 11th and 12th(2) clock cycles the falling edge of Chip Select (CS) initiates a high voltage cycle that writes the data into the non-volatile memory array. The Serial Data Output (DO) pin indicates the Ready/Busy status.

WRITE
The WRITE command writes 16 bits of data into the specified address.
Between the rising edge of the 27th and 28th(3) clock cycles the falling edge of Chip Select (CS) initiates a high voltage cycle that writes the data into the non-volatile memory array.
The Serial Data Output (DO) pin indicates the Ready/Busy status. During this high voltage cycle (busy state), the EEPROM does not receive any commands.
The unit will not write the data into non-volatile memory array if Chip Select (CS) is L after input of the 28th(4) or more cycle of the Serial Clock (SK)

ERAL
The ERAL command writes '1' in all bits at the specified address. Between the rising edge of 11th and 12th(5) clock cycles the falling edge of Serial Clock (SK) initiates a high voltage cycle that writes the data into the non-volatile memory array. Serial Data Output (DO) gives an indication of the Ready/Busy status. The time from the rising edge of the 11th(6) clock to the falling edge of S should be more than t_{SKH}.

WRAL
This command writes 16 bits of data to the specified address. It takes maximum 5ms, since all of the data are written into the memory array at the same time. Between the rising edge of the 27th and 28th(7) clock cycles the falling edge of Chip Select (CS) initiates a high voltage cycle that writes the data into the non-volatile memory array. The EEPROM will not write the data into the non-volatile memory array if Chip Select (CS) is L after input of the 28th(8) or more cycle of the Serial Clock (SK).

(1),(6) BR93C46 : 9th
BR93C56/66 : 11th
(2),(5) BR93C46 : 9th and 10th
BR93C56/66 : 11th and 12th
(3),(7) BR93C46 : 25th and 26th
BR93C56/66 : 27th and 28th
(4),(8) BR93C46 : 26th
BR93C56/66 : 28th

●Timing Diagrams

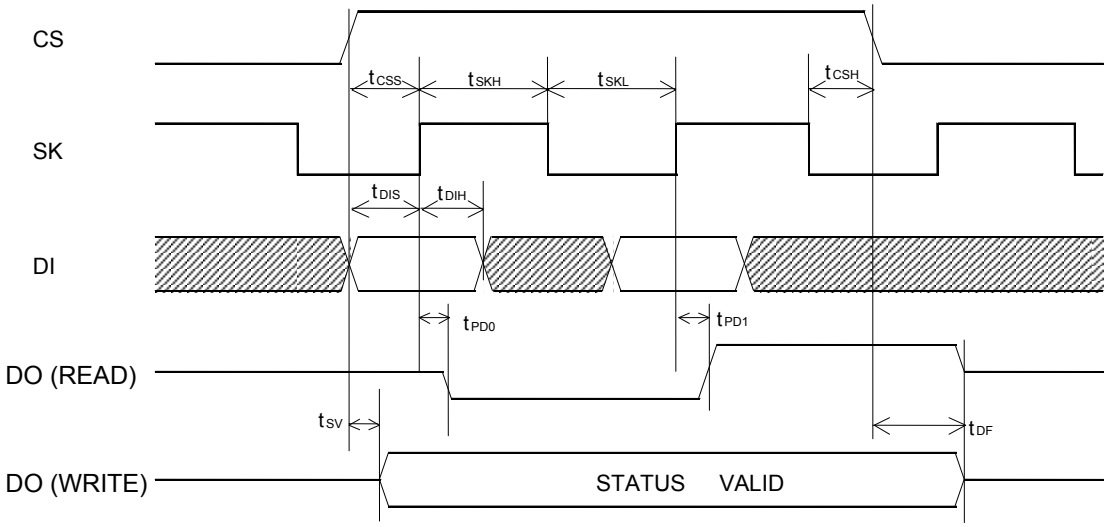


Figure 3: Synchronous Data Timing

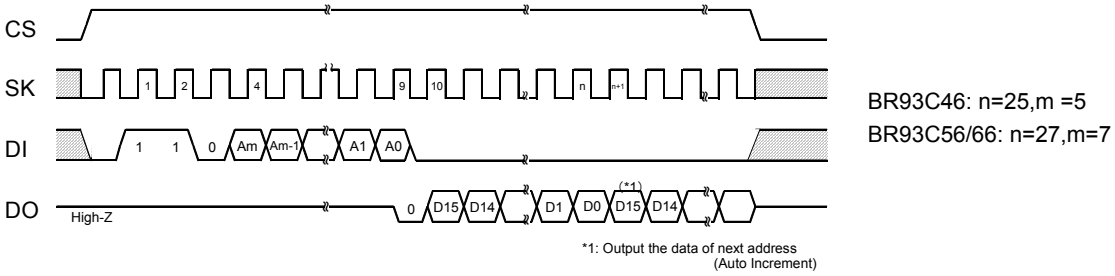


Figure 4: READ Sequence

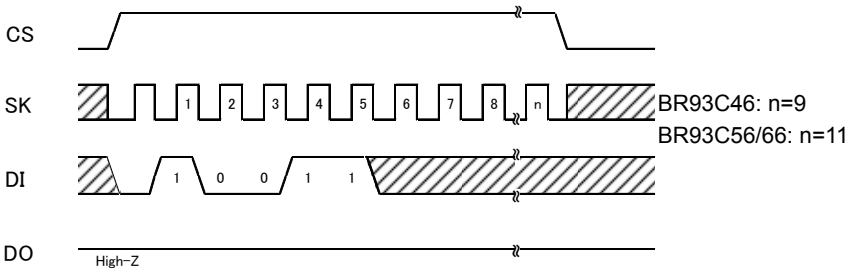


Figure 5: EWEN Sequence

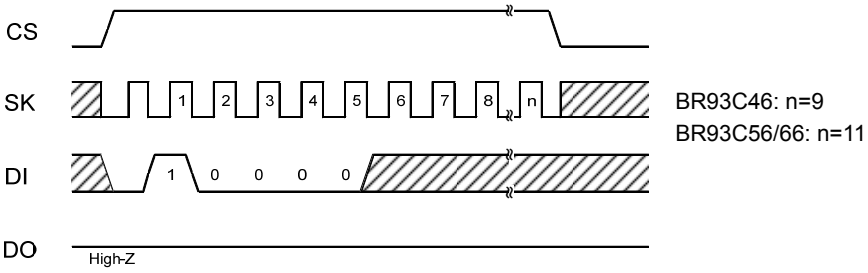
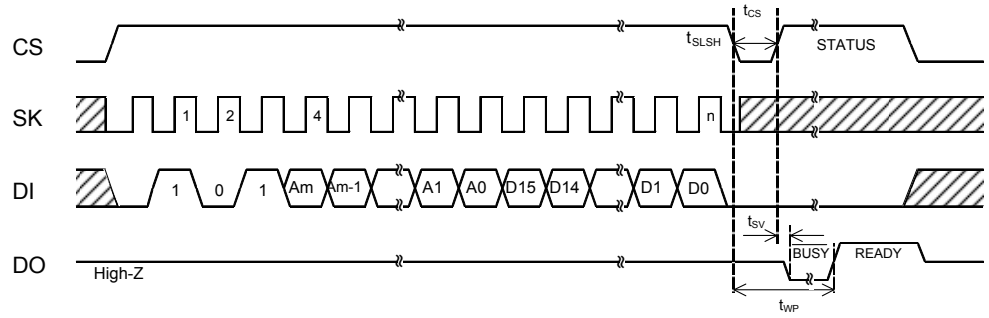
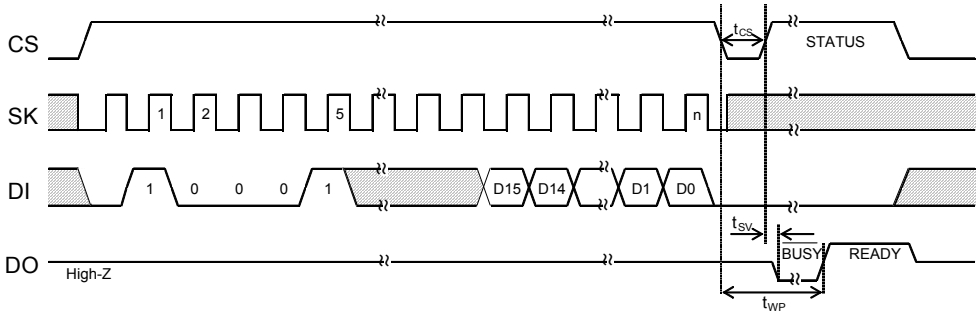


Figure 6: EWDS Sequence



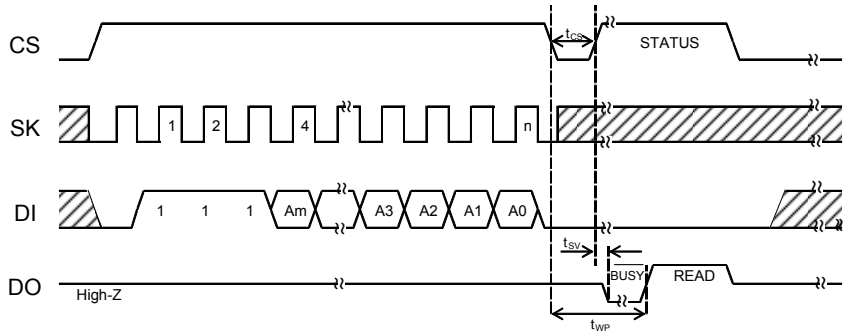
BR93C46: n=25,m =5
BR93C56/66: n=27,m=7

Figure 7: WRITE Sequence



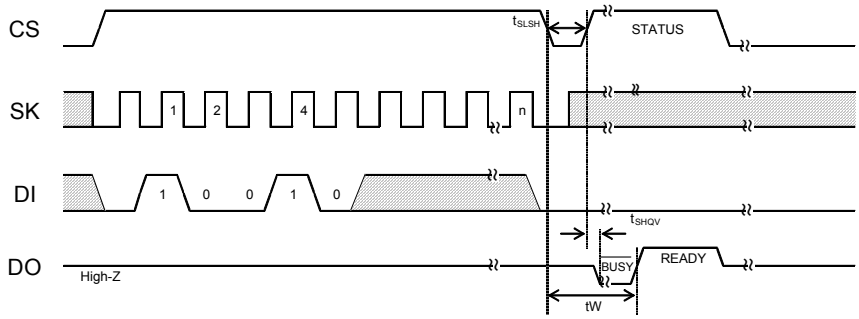
*Inconsequential Data
BR93C46: n=25
BR93C56/66: n=27

Figure 8: WRAL Sequence



BR93C46: n=9, m=5
BR93C56/66: n=11, m=7

Figure 9: ERASE Sequence



BR93C46: n=9
BR93C56/66: n=11

Figure 10: ERAL Sequence.

●Ordering Information

Table 8: BR93C46 Ordering Information

Ordering Code	Package	Operating Range
BR93C46R-10SU-1.8 BR93C46-10SU-1.8	JEDEC SOIC JEDEC SOIC	-40 to 85℃

Table 9: BR93C56 Ordering Information

Ordering Code	Package	Operating Range
BR93C56-10SU-1.8 BR93C56-10TU-1.8	JEDEC SOIC	-40 to 85℃

Table 10: BR93C66 Ordering Information

Ordering Code	Package	Operating Range
BR93C66-10SU-1.8 BR93C66-10TU-1.8	JEDEC SOIC	-40 to 85℃

●Package outline

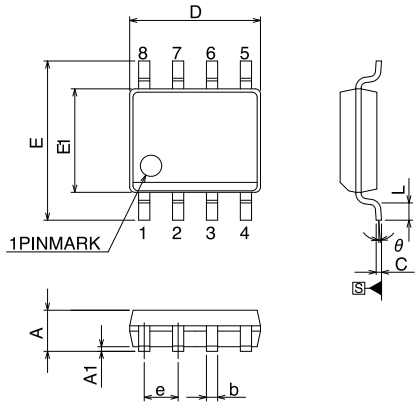


Figure 11. JEDEC SOIC Package outline

Table 11 JEDEC SOIC, Package Size Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	1.375	1.275	1.475	0.054	0.050	0.058
A1	0.175	-	-	0.007	-	-
b	0.42	0.32	0.52	0.017	0.013	0.02
c	0.20	0.10	0.30	0.008	0.004	0.012
D	4.90	4.70	5.10	0.193	0.185	0.201
e	1.27	—	—	0.05	—	—
E	6.00	5.70	6.30	0.236	0.224	0.248
E1	3.90	3.70	4.10	0.154	0.146	0.161
L	—	0.45	—	—	0.018	—
θ	4°	0°	10°	4°	0°	10°

Notes
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion, or gate burns.
3. Reference JEDEC MS-012 variation AA.

●Ordering part number

B	R	9	3	C	4	6	A	N	-	1	0	S	U	-	1.8

- ROHM prefix
- BUS type
  93C: Microwire
  24C: I^2C
  25: SPI
- Density

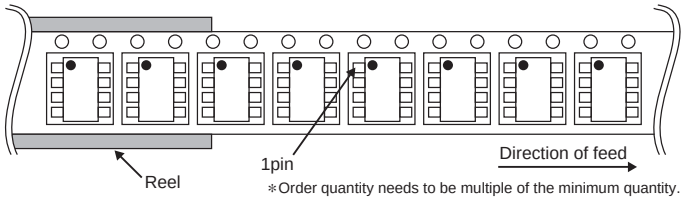
Microwire	I^2C	SPI
46=1K	01=1K	010=1K
56=2K	02=2K	020=2K
66=4K	04=4K	040=4K
76=8K	08=8K	080=8K
86=16K	16=16K	160=16K
	32=32K	320=32K
	64=64K	640=64K

- REV
- Pakage type
  □-10S:JEDECSOIC
  (Microwire,BR24C01)
  N-10S: JEDECSOIC
  (I2C[except BR24C01],SPI)
- Operating temperature
  U: -40°C~+85°C
  Pb-Free
- Supplyvoltage
  1.8:1.8V~5.5V
  2.7:2.7V~5.5V

●Tape and Real Information

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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