Features

- **Low Voltage Operation**
  - **2.7V Read**
  - **5V Program/Erase**
- **Fast Read Access Time - 120 ns**
- **Internal Erase/Program Control**
- **Sector Architecture**
  - **One 8K Words (16K bytes) Boot Block with Programming Lockout**
  - **Two 8K Words (16K bytes) Parameter Blocks**
  - **One 232K Words (464K bytes) Main Memory Array Block**
- **Fast Sector Erase Time - 10 seconds**
- **Word-By-Word Programming - 10 µs/Word**
- **Hardware Data Protection**
- **$\overline{\text{DATA}}$ Polling For End Of Program Detection**
- **Low Power Dissipation**
  - **25 mA Active Current**
  - **50 µA CMOS Standby Current**
- **Typical 10,000 Write Cycles**

Description

The AT49BV4096 and AT49LV4096 are 3-volt, 4-megabit Flash Memories organized as 256K words of 16 bits each. Manufactured with Atmel's advanced nonvolatile CMOS technology, the devices offer access times to 120 ns with power dissipation of just 67 mW at 2.7V read. When deselected, the CMOS standby current is less than 50 µA.

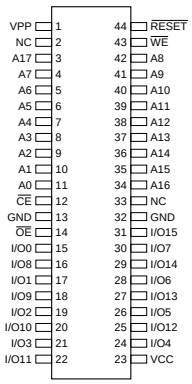
To allow for simple in-system reprogrammability, the AT49BV4096/LV4096 does not require high input voltages for programming. Reading data out of the device is similar

(continued)

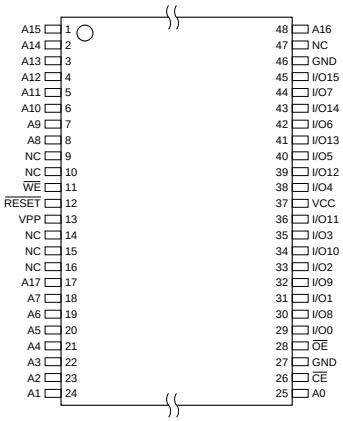
Pin Configurations

Pin Name	Function
A0 - A17	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RESET}}$	Reset
VPP	Program/Erase Power Supply
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

SOIC (SOP)



TSOP Top View
Type 1



4-Megabit (256K x 16) 3-volt Only Flash Memory

AT49BV4096
AT49LV4096

Rev. 0985B–10/98

to reading from an EPROM; it has standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs to avoid bus contention. Reprogramming the AT49BV4096/LV4096 is performed by first erasing a block of data and then programming on a word-by-word basis.

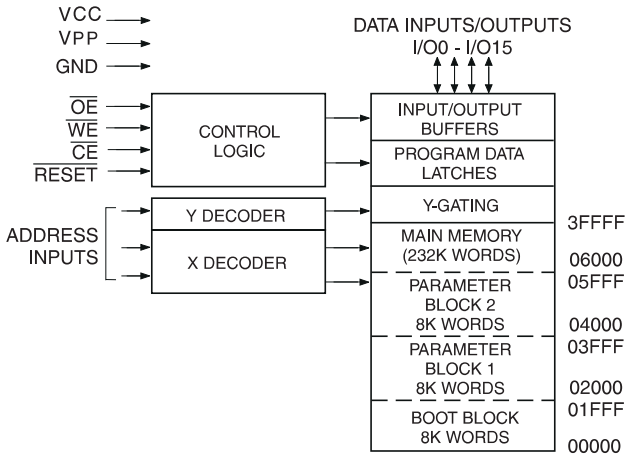
The device is erased by executing the erase command sequence; the device internally controls the erase operation. The memory is divided into three blocks for erase operations. There are two 8K word parameter block sections and one sector consisting of the boot block and the main memory array block. The AT49BV4096/LV4096 is programmed on a word-by-word basis.

The device has the capability to protect the data in the boot block; this feature is enabled by a command sequence. Once the boot block programming lockout feature is enabled, the data in the boot block cannot be changed when input levels of 3.6 volts or less are used. The typical number of program and erase cycles is in excess of 10,000 cycles.

The optional 8K word boot block section includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is protected from being reprogrammed.

During a chip erase, sector erase, or word programming, the V_{PP} pin must be at 5V ± 10%.

Block Diagram



Device Operation

READ: The AT49BV4096/LV4096 is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the Read or Standby mode, depending upon the state of the control inputs. By applying a 12V ± 0.5V input signal to the $\overline{RESET}$ pin the boot block array can be reprogrammed even if the boot block program lockout feature has been enabled (see Boot Block Programming Lockout Override section).

ERASURE: Before a word can be reprogrammed, it must be erased. The erased state of memory bits is a logical “1”. The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase commands.

CHIP ERASE: The entire device can be erased at one time by using the 6-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is t_{EC}.

If the boot block lockout has been enabled, the Chip Erase will not erase the data in the boot block; it will erase the main memory block and the parameter blocks only. After the chip erase, the device will return to the read or standby mode.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into three sectors that can be individually erased. There are two 8K word parameter block sections and one sector consisting of the boot block and the main memory array block. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched at the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together (from the same sector erase command). Once the boot region has been protected, only the main memory array sector will erase when its sector erase command is issued.

WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical “0”) on a word-by-word basis. Programming is accomplished via the internal device command register and is a 4 bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is completed after the specified t_{BP} cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K words. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the boot block is 00000H to 01FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed when input levels of 5.5V or less are used. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been enabled and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

BOOT BLOCK PROGRAMMING LOCKOUT OVERRIDE: The user can override the boot block programming lockout by taking the $\overline{RESET}$ pin to 12 ± 0.5 volts. By doing this protected boot block data can be altered through a chip erase, sector erase or word programming. When the $\overline{RESET}$ pin is brought back to TTL levels the boot block programming lockout feature is again active.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49BV4096/LV4096 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a “0” on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT49BV4096/LV4096 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49BV4096/LV4096 in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 2.7V to 3.6V power supply, the address inputs and control inputs ($\overline{OE}$, $\overline{CE}$, and $\overline{WE}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

Command Definition (in Hex)(1)

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA(4)(5)	30
Word Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout(2)	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit(3)	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit(3)	1	xxxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex).
2. The 8K word boot sector has the address range 00000H to 01FFFH.
3. Either one of the Product ID Exit commands can be used.
4. SA = sector addresses
   SA = 03XXX for PARAMETER BLOCK 1
   SA = 05XXX for PARAMETER BLOCK 2
   SA = 1FXXX for MAIN MEMORY ARRAY
5. When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	25.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49LV4096-12	AT49BV/LV4096-15	AT49BV/LV4096-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply	AT49LV4096	3.0V to 3.6V	3.0V to 3.6V	3.0V to 3.6V
	AT49BV4096	N/A	2.7V to 3.6V	2.7V to 3.6V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}
Program/ Erase[2]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	5V ± 10%	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}	V_{IL}		
Program Inhibit	X	V_{IL}	X	V_{IH}	V_{IL}		
Output Disable	X	V_{IH}	X	V_{IH}	X		High Z
Reset	X	X	X	V_{IL}	X	X	High Z
Product Identification							
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}		A1 - A17 = V_{IL}, A9 = V_H,[3] A0 = V_{IL}	Manufacturer Code[4]
						A1 - A17 = V_{IL}, A9 = V_H,[3] A0 = V_{IH}	Device Code[4]
Software [5]				V_{IH}		A0 = V_{IL}, A1 - A17 = V_{IL}	Manufacturer Code[4]
						A0 = $V_{IH,}$ A1 - A17 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: 92H
5. See details under Software Product Identification Entry/Exit.

DC Characteristics

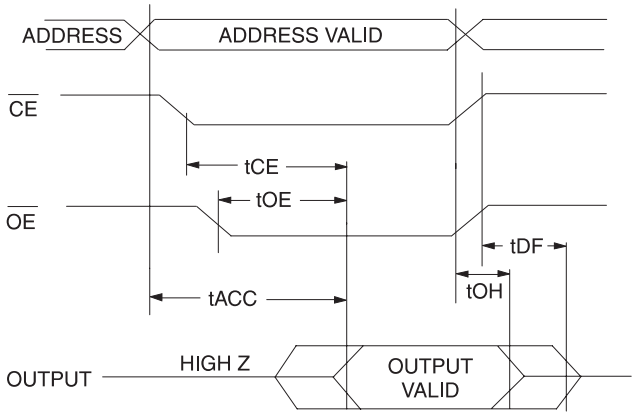
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		50	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		1	mA
I_{CC}[1]	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		25	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Note: 1. In the erase mode, I_{CC} is 50 mA.

AC Read Characteristics

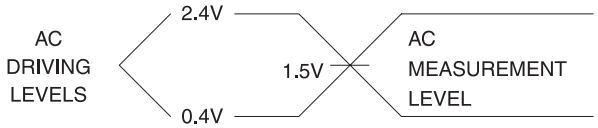
Symbol	Parameter	AT49LV4096-12		AT49BV/LV4096-15		AT49BV/LV4096-20		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		120		150		200	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	50	0	100	0	100	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	30	0	50	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms[1][2][3][4]

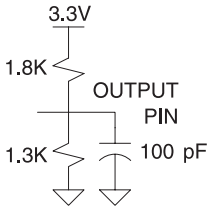


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on tACC.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

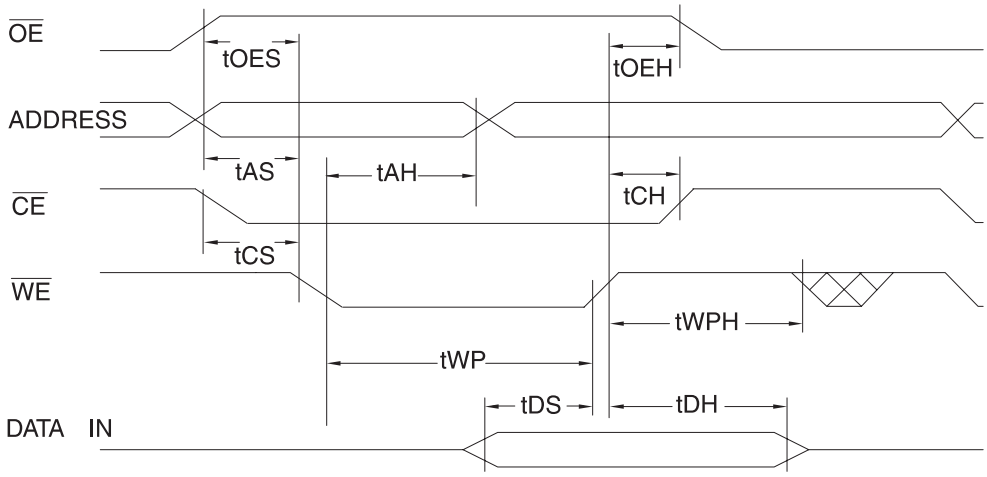
Note: 1. This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

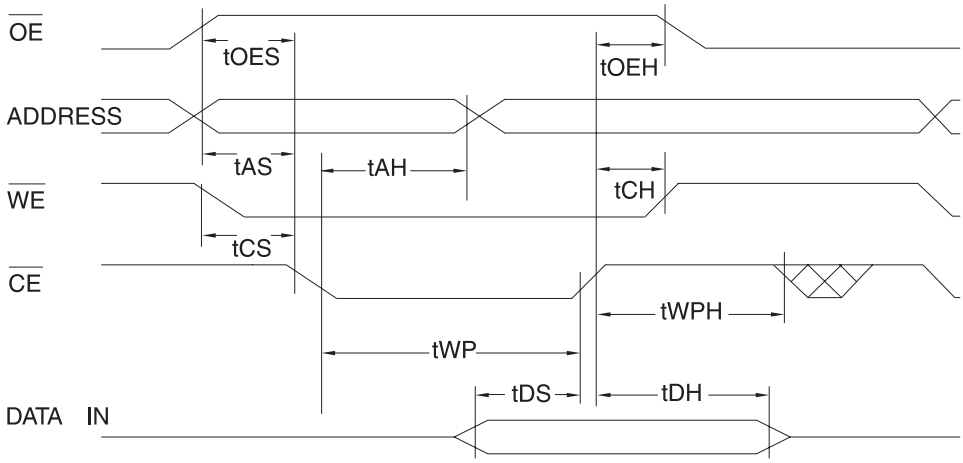
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	200		ns
t_{DS}	Data Set-up Time	100		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	200		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



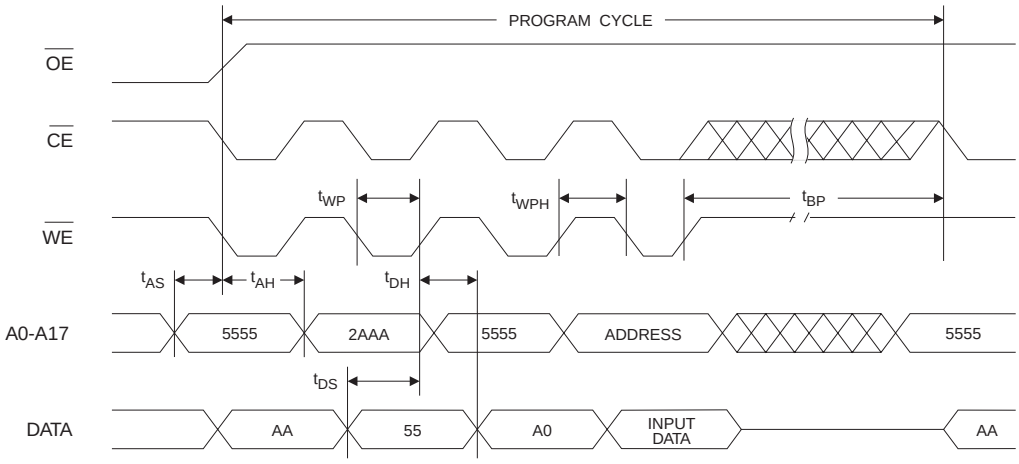
$\overline{CE}$ Controlled



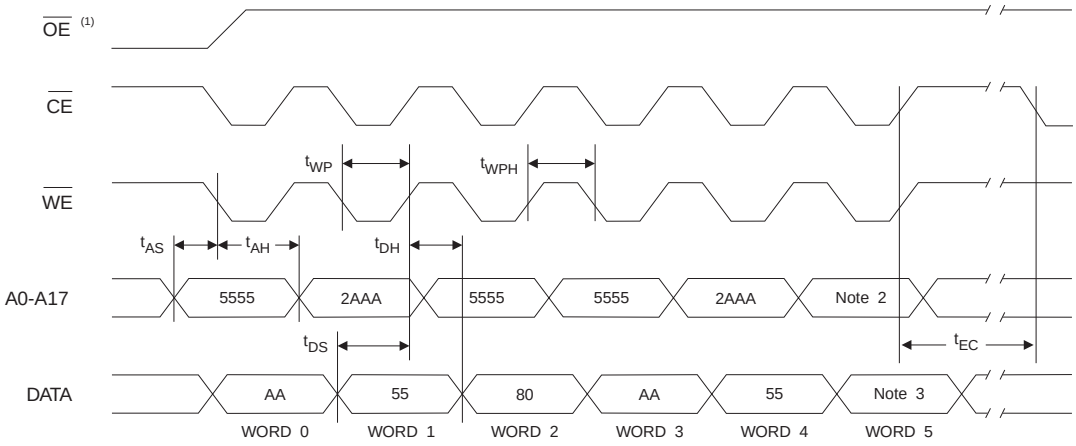
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time		30	50	µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	100			ns
t_{DS}	Data Set-up Time	100			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	200			ns
t_{WPH}	Write Pulse Width High	200			ns
t_{EC}	Erase Cycle Time			10	seconds

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



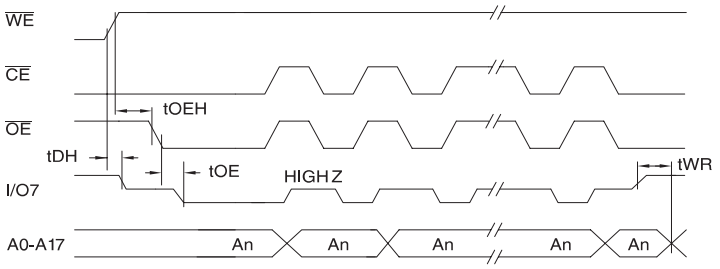
Notes:
1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 4 under command definitions.)
3. For chip erase, the data should be 10_H, and for sector erase, the data should be 30_H.

$\overline{\text{Data}}$ Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2))				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

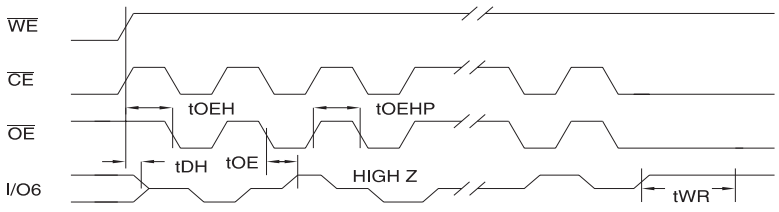


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

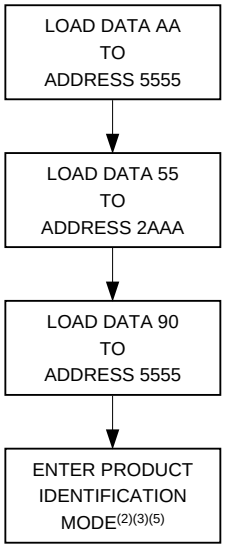
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms(1)(2)(3)

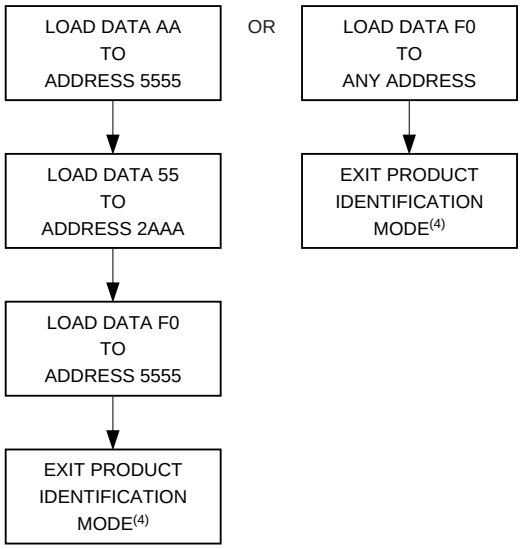


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]



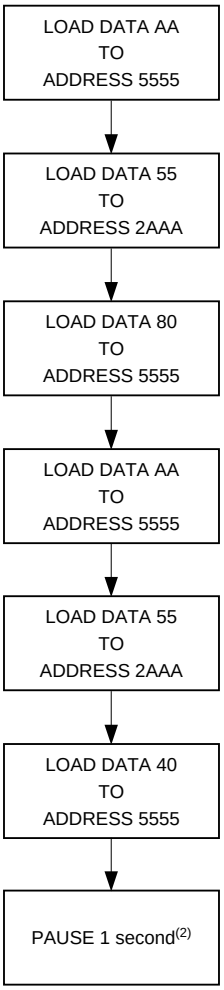
Software Product Identification Exit[1][6]



Notes for software product identification:

1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A14 - A0 (Hex).
2. A1 - A17 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: 82H
6. Either one of the Product ID Exit commands can be used.

Boot Block Lockout Enable Algorithm[1]



Notes for boot block lockout feature enable:

1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
   Address Format: A14 - A0 (Hex).
2. Boot block lockout feature enabled.

Ordering Information

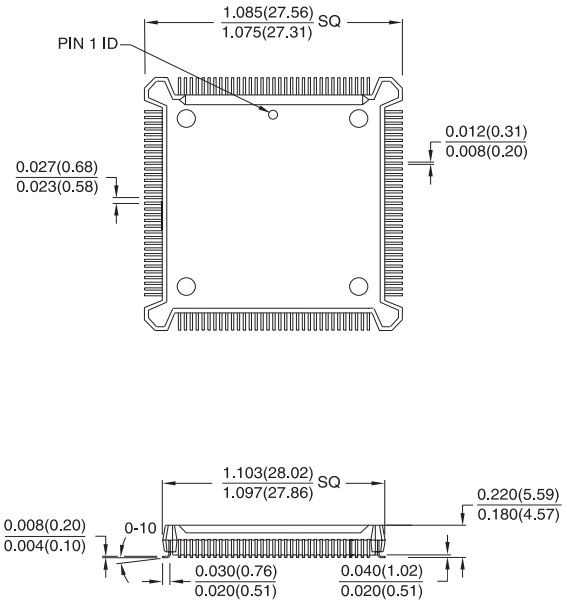
t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	25	0.05	AT49LV4096-12RC AT49LV4096-12TC	44R 48T	Commercial (0° to 70°C)
			AT49LV4096-12RI AT49LV4096-12TI	44R 48T	Industrial (-40° to 85°C)
150	25	0.05	AT49LV4096-15RC AT49LV4096-15TC	44R 48T	Commercial (0° to 70°C)
			AT49LV4096-15RI AT49LV4096-15TI	44R 48T	Industrial (-40° to 85°C)
200	25	0.05	AT49LV4096-20RC AT49LV4096-20TC	44R 48T	Commercial (0° to 70°C)
			AT49LV4096-20RI AT49LV4096-20TI	44R 48T	Industrial (-40° to 85°C)
150	25	0.05	AT49BV4096-15RC AT49BV4096-15TC	44R 48T	Commercial (0° to 70°C)
			AT49BV4096-15RI AT49BV4096-15TI	44R 48T	Industrial (-40° to 85°C)
200	25	0.05	AT49BV4096-20RC AT49BV4096-20TC	44R 48T	Commercial (0° to 70°C)
			AT49BV4096-20RI AT49BV4096-20TI	44R 48T	Industrial (-40° to 85°C)

Note: 1. The AT49BV4096/LV4096 has an optional boot block feature. The part number shown in the Ordering Information table is for devices with the boot block in the lower address range (i.e., 00000H to 01FFFH). Users requiring the boot block to be in the higher address range should contact Atmel.

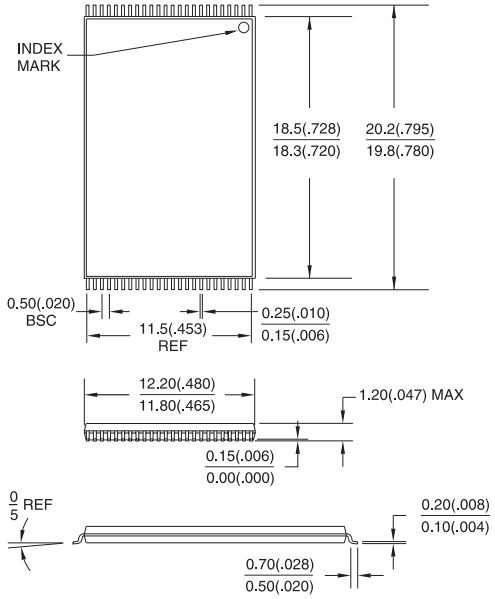
Package Type	
44R	44-Lead, 0.525" Wide, Plastic Gull Wing Small Outline Package (SOIC/SOP)
48T	48-Lead, Thin Small Outline Package (TSOP)

Packaging Information

44R, 44-Lead, 0.525" Wide,
Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



48T, 48-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 DD



*Controlling dimension: millimeters

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686677
FAX (44) 1276-686697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road
Tsimshatsui East
Kowloon, Hong Kong
TEL (852) 27219778
FAX (852) 27221369

Japan
Atmel Japan K.K.
Tonetsu Shinkawa Bldg., 9F
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4 42 53 60 00
FAX (33) 4 42 53 60 01

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

0985B–10/98/xM