Features

- Single Voltage Read/Write Operation: 2.65V to 3.6V
- Access Time 70 ns
- Sector Erase Architecture
 - Thirty-one 32K Word (64K Bytes) Sectors with Individual Write Lockout
 - Eight 4K Word (8K Bytes) Sectors with Individual Write Lockout
- Fast Word Program Time 12 μs
- Fast Sector Erase Time 300 ms
- Suspend/Resume Feature for Erase and Program
 - Supports Reading and Programming from Any Sector by Suspending Erase of a Different Sector
 - Supports Reading Any Word by Suspending Programming of Any Other Word
- Low-power Operation
 - 12 mA Active
 - 13 µA Standby
- VPP Pin for Write Protection
- WP Pin for Sector Protection
- RESET Input for Device Initialization
- Flexible Sector Protection
- TSOP and CBGA Package Options
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register
- Minimum 100,000 Erase Cycles
- Common Flash Interface (CFI)
- Green (Pb/Halide-free) Packaging Option

1. Description

The AT49BV160C(T) is a 2.7-volt 16-megabit Flash memory organized as 1,048,576 words of 16 bits each. The memory is divided into 39 sectors for erase operations. The device is offered in a 48-lead TSOP and a 46-ball CBGA package. The device has \overline{CE} and \overline{OE} control signals to avoid any bus contention. This device can be read or reprogrammed using a single power supply, making it ideally suited for in-system programming.

The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector (see "Flexible Sector Protection" on page 6).

To increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the memory.

The VPP pin provides data protection. When the V_{PP} input is below 0.4V, the program and erase functions are inhibited. When V_{PP} is at 1.5V or above, normal program and erase operations can be performed.



16-megabit (1M x 16) 3-volt Only Flash Memory

AT49BV160C AT49BV160CT

3367F-FLASH-4/05

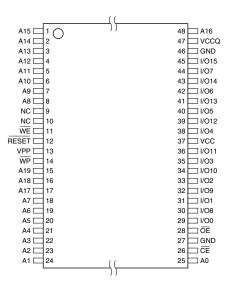




2. Pin Configurations

Pin Name	Function	
A0 - A19	Addresses	
CE	Chip Enable	
ŌĒ	Output Enable	
WE	Write Enable	
RESET	Reset	
VPP	Write Protection	
I/O0 - I/O15	Data Inputs/Outputs	
NC	No Connect	
VCCQ	Output Power Supply	
WP	Write Protect	

2.1 TSOP Top View (Type 1)

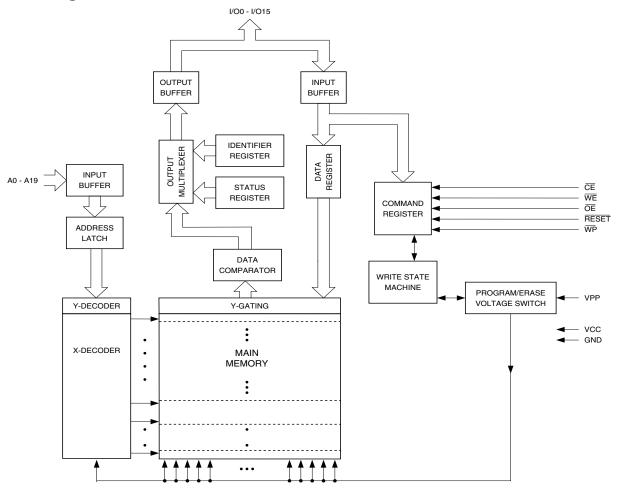


2.2 CBGA Top View (Ball Down)

	1	2	3	4	5	6	7	8	
	•								
А	\odot	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	\bigcirc	
в	A13	A11 ()	A8 ()		WP ()	A19 ()	A7 ()	A4 ()	
с	A14	A10	WE ()	RST	A18	A17 ()	A5 ()	A2 ()	
D	A15	A12	A9 ()	\odot	\bigcirc	A6 ()	A3 ()	A1 ()	
Е	A16 ()	l/014 ()	I/O5 ()	l/011 ()	I/02 ()	I/08	CE ()	A0 ()	
F	VCCQ () GND	I/015 () I/07	I/06 () I/013	I/012 () I/04	I/03 () VCC	I/O9 () I/O10	I/00 () I/01		

AT49BV160C(T)

3. Block Diagram



4. Device Operation

4.1 Read

When the AT49BV160C(T) is in the read mode, with \overline{CE} and \overline{OE} low and \overline{WE} high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high impedance state whenever \overline{CE} or \overline{OE} is high. This dual-line control gives designers flexibility in preventing bus contention.

4.2 Command Sequences

When the device is first powered on, it will be in the read mode. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the "Command Definition Table" on page 15 (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high. The address and data are latched by the first rising edge of \overline{CE} or \overline{WE} . Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.





4.3 Reset

A RESET input pin is provided to ease some system applications. When RESET is at a logic high level, the device is in its standard operating mode. A low level on the RESET input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the RESET pin, the device returns to the read mode, depending upon the state of the control inputs.

4.4 Erasure

Before a word can be reprogrammed, it must be erased. The erased state of memory bits is a logical "1". The individual sectors can be erased by using the Sector Erase command.

4.4.1 Sector Erase

The device is organized into 39 sectors (SA0 - SA38) that can be individually erased. The Sector Erase command is a two-bus cycle operation. The sector address and the D0H Data Input command are latched on the rising edge of $\overline{\text{WE}}$. The sector erase starts after the rising edge of $\overline{\text{WE}}$ of the second cycle provided the given sector has not been protected. The erase operation is internally controlled; it will automatically time to completion. The maximum time to erase a sector is t_{SEC} . An attempt to erase a sector that has been protected will result in the operation terminating immediately.

4.5 Word Programming

Once a memory sector is erased, it is programmed (to a logical "0") on a word-by-word basis. Programming is accomplished via the Internal Device command register and is a two-bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified t_{BP} cycle time. If the program status bit is a "1", the device was not able to verify that the program operation was performed successfully. The status register indicates the programming status. While the program sequence executes, status bit I/O7 is "0". While programming, the only valid commands are Read Status Register, Program Suspend and Program Resume.

4.6 VPP Pin

The circuitry of the AT49BV160C(T) is designed so that the device cannot be programmed or erased if the V_{PP} voltage is less that 0.4V. When V_{PP} is at 1.5V or above, normal program and erase operations can be performed. The VPP pin cannot be left floating.

4.7 Read Status Register

The status register indicates the status of device operations and the success/failure of that operation. The Read Status Register command causes subsequent reads to output data from the status register until another command is issued. To return to reading from the memory, issue a Read command.

The status register bits are output on I/O7 - I/O0. The upper byte, I/O15 - I/O8, outputs 00H when a Read Status Register command is issued.

The contents of the status register [SR7:SR0] are latched on the falling edge of \overline{OE} or \overline{CE} (whichever occurs last), which prevents possible bus errors that might occur if status register contents change while being read. \overline{CE} or \overline{OE} must be toggled with each subsequent status read, or the status register will not indicate completion of a Program or Erase operation.

When the Write State Machine (WSM) is active, SR7 will indicate the status of the WSM; the remaining bits in the status register indicate whether the WSM was successful in performing the preferred operation (see Table 4-1).

 Table 4-1.
 Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS	PSS	SLS	R
7	6	5	4	3	2	1	0
					No	tes	
SR7 WRITE ST 1 = Ready 0 = Busy	ATE MACHINE S	STATUS (WSMS)			ate Machine bit fi completion, befo		
1 = Erase Susp	SUSPEND STAT ended ogress/Complete			both WSMS and	ispend is issued, d ESS bits to "1" ne command is is	– ESS bit remain	
SR5 = ERASE 1 = Error in Sec 0 = Successful	tor Erase				set to "1", WSM the sector and is		
SR4 = PROGR 1 = Error in Pro 0 = Successful	• •)		When this bit is program a word	set to "1", WSM	has attempted bi	ut failed to
SR3 = VPP ST/ 1 = VPP Low D 0 = VPP OK	ATUS (VPPS) etect, Operation	Abort		level. The WSN Erase comman system if V _{PP} ha	bit does not provi l interrogates V _{PF} d sequences hav as not been switc ation is verified b	blevel only after t e been entered a hed on. The V _{PP}	he Program or nd informs the
SR2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed				sets both WSM	Suspend is issue S and PSS bits to Resume comma	o "1". PSS bit ren	
 SR1 = SECTOR LOCK STATUS 1 = Prog/Erase attempted on a locked sector; Operation aborted. 0 = No operation to locked sectors 			sectors, this bit	Erase operation i is set by the WSI device is returne	M. The operation	specified is	
SR0 = RESER	/ED FOR FUTUF	RE ENHANCEME	NTS (R)		ved for future use e status register.	e and should be r	nasked out

Note: 1. A Command Sequence Error is indicated when SR1, SR3, SR4 and SR5 are set.





4.7.1 Clear Status Register

The WSM can set status register bits 1 through 7 and can clear bits 2, 6 and 7; but, the WSM cannot clear status register bits 1, 3, 4 or 5. Because bits 1, 3, 4 and 5 indicate various error conditions, these bits can be cleared only through the Clear Status Register command. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several addresses or erasing multiple sectors in sequence) before reading the status register to determine if an error occurred during those operations. The status register should be cleared before beginning another operation. The Read command must be issued before data can be read from the memory array. The status register can also be cleared by resetting the device.

4.8 Flexible Sector Protection

The AT49BV160C(T) offers two sector protection modes, the Softlock and the Hardlock. The Softlock mode is optimized as sector protection for sectors whose content changes frequently. The Hardlock protection mode is recommended for sectors whose content changes infrequently. Once either of these two modes is enabled, the contents of the selected sector is read-only and cannot be erased or programmed. Each sector can be independently programmed for either the Softlock or Hardlock sector protection mode. At power-up and reset, all sectors have their Softlock protection mode enabled.

4.8.1 Softlock and Unlock

The Softlock protection mode can be disabled by issuing a two-bus cycle Unlock command to the selected sector. Once a sector is unlocked, its contents can be erased or programmed. To enable the Softlock protection mode, a two-bus cycle Softlock command must be issued to the selected sector.

4.8.2 Hardlock and Write Protect

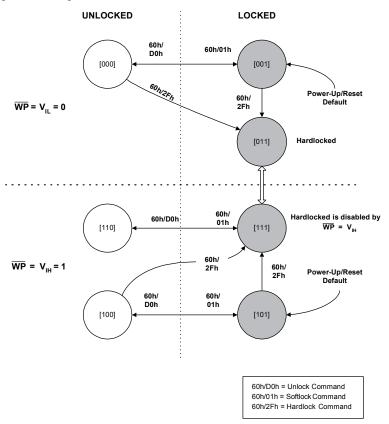
The Hardlock sector protection mode operates in conjunction with the Write Protect (\overline{WP}) pin. The Hardlock sector protection mode can be enabled by issuing a two-bus cycle Hardlock Software command to the selected sector. The state of the Write Protect pin affects whether the Hardlock protection mode can be overridden.

- When the WP pin is low and the Hardlock protection mode is enabled, the sector cannot be unlocked and the contents of the sector is read-only.
- When the WP pin is high, the Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command.
- To disable the Hardlock sector protection mode, the chip must be either reset or power cycled.

V _{PP}	WP	Hard- lock	Soft- lock	Erase/ Prog Allowed?	Comments
$V_{CC}/5V$	0	0	0	Yes	No sector is locked
V _{CC} /5V	0	0	1	No	Sector is Softlocked. The Unlock command can unlock the sector.
V _{CC} /5V	0	1	1	No	Hardlock protection mode is enabled. The sector cannot be unlocked.
$V_{CC}/5V$	1	0	0	Yes	No sector is locked.
V _{CC} /5V	1	0	1	No	Sector is Softlocked. The Unlock command can unlock the sector.
V _{CC} /5V	1	1	0	Yes	Hardlock protection mode is overridden and the sector is not locked.
V _{CC} /5V	1	1	1	No	Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command.
V _{IL}	x	x	x	No	Erase and Program Operations cannot be performed.

 Table 4-2.
 Hardlock and Softlock Protection Configurations in Conjunction with \overline{WP}

Figure 4-1. Sector Locking State Diagram



Note: 1. The notation [X, Y, Z] denotes the locking state of a sector. The current locking state of a sector is defined by the state of WP and the two bits of the sector-lock status D[1:0].





4.8.3 Sector Protection Detection

A software method is available to determine if the sector protection Softlock or Hardlock features are enabled. When the device is in the software product identification mode, a read from the I/O0 and I/O1 at address location 00002H within a sector will show if the sector is unlocked, softlocked, or hardlocked.

I/O1	I/O0	Sector Protection Status
0	0	Sector Not Locked
0	1	Softlock Enabled
1	0	Hardlock Enabled
1	1	Both Hardlock and Softlock Enabled

 Table 4-3.
 Sector Protection Status

4.9 Erase Suspend/Erase Resume

The Erase Suspend command allows the system to interrupt a sector erase operation and then program or read data from a different sector within the memory. After the Erase Suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the erase operation has been suspended, the system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command. The only valid commands while erase is suspended are Read Status Register, Product ID Entry, CFI Query, Program, Program Resume, Erase Resume, Sector Softlock/Hardlock, Sector Unlock.

4.10 Program Suspend/Program Resume

The Program Suspend command allows the system to interrupt a programming operation and then read data from a different word within the memory. After the Program Suspend command is given, the device requires a maximum of 20 µs to suspend the programming operation. After the programming operation has been suspended, the system can then read data from any other word within the device. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same and the command sequence for the erase resume and program resume are the same. The only other valid commands while program is suspended are Read Status Register, Product ID Entry, CFI Query and Program Resume.

4.11 Product Identification

The product identification mode identifies the device and manufacturer as Atmel. It may be accessed a software operation. For details, see "Operating Modes" on page 19.

4.12 128-bit Protection Register

The AT49BV160C(T) contains a 128-bit register that can be used for security purposes in system design. The protection register is divided into two 64-bit sectors. The two sectors are designated as sector A and sector B. The data in sector A is non-changeable and is programmed at the factory with a unique number. The data in sector B is programmed by the user and can be locked out such that data in the sector cannot be reprogrammed. To program sector B in the protection register, the two-bus cycle Program Protection Register command must be used as shown in the "Command Definition Table" on page 15. To lock out sector B, the two-bus cycle Lock Protection Register command must be used as shown in the "Command Definition Table". Data bit D1 must be zero during the second bus cycle. All other data bits during the second bus cycle are don't cares. To determine whether sector B is locked out, use the status of sector B protection command. If data bit D1 is zero, sector B is locked. If data bit D1 is one, sector B can be reprogrammed. Please see the "Protection Register Addressing Table" on page 16 for the address locations in the protection register. To read the protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After determining whether sector B is protected or not, or reading the protection register, the Read command must be given to return to the read mode.

4.13 Common Flash Interface (CFI)

CFI is a published, standardized data structure that may be read from a flash device. CFI allows system software to query the installed device to determine the configurations, various electrical and timing parameters and functions supported by the device. CFI is used to allow the system to learn how to interface to the flash device most optimally. The two primary benefits of using CFI are ease of upgrading and second source availability. The command to enter the CFI Query mode is a one-bus cycle command which requires writing data 98h to any address. The CFI Query command can be written when the device is ready to read data or can also be written when the part is in the product ID mode. Once in the CFI Query mode, the system can read CFI data at the addresses given in "Common Flash Interface Definition Table" on page 25. To return to the read mode, issue the Read command.

4.14 Hardware Data Protection

The Hardware Data Protection feature protects against inadvertent programs to the AT49BV160C(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high inhibits program cycles. (d) Program inhibit: V_{PP} is less than V_{ILPP} . (e) V_{PP} power-on delay: once V_{PP} has reached 0.9V, program and erase operations are inhibited for 100 ns.

4.15 Input Levels

While operating with a 2.65V to 3.6V power supply, the address inputs and control inputs (\overline{OE} , \overline{CE} and \overline{WE}) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CCQ} + 0.6V.

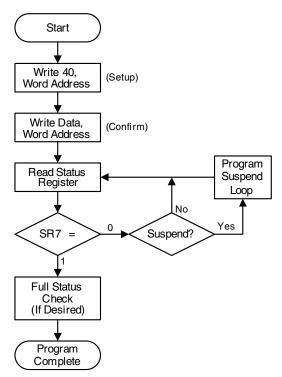
4.16 Output Levels

For the AT49BV160C(T), output high levels (V_{OH}) are equal to V_{CCQ} - 0.1V (not V_{CC}). For 2.65V -3.6V output levels, V_{CCQ} must be tied to V_{CC}. For 1.8V - 2.2V output levels, V_{CCQ} must be regulated to 2.0V \pm 10%, while V_{CC} must be regulated to 2.65V - 3.0V (for minimum power).





5. Word Program Flowchart

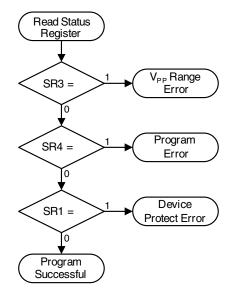


6. Word Program Procedure

Bus Operation	Command	Comments		
Write	Program Setup	Data = 40 Addr = Location to program		
Write	Data	Data = Data to program Addr = Location to program		
Read	None	Status register data: Toggle \overline{CE} or \overline{OE} to update status register		
Idle	None	Check SR7 1 = WSM Ready 0 = WSM Busy		
	Repeat for subsequent Word Program operations.			

Full status register check can be done after each program, or after a sequence of program operations. Write FF after the last operation to set to the Read state.

7. Full Status Check Flowchart



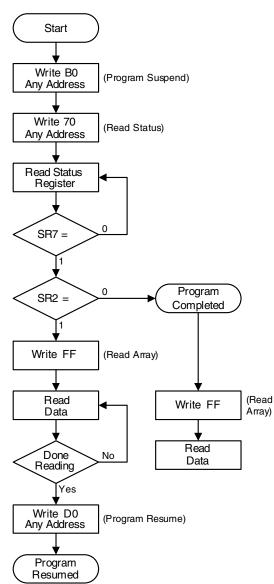
8. Full Status Check Procedure

Command	Comments
None	Check SR3: 1 = V _{PP} Error
None	Check SR4: 1 = Data Program Error
None	Check SR1: 1 = Sector locked; operation aborted
	None None

SR3 MUST be cleared before the Write State Machine allows further program attempts.

If an error is detected, clear the status register before continuing operations – only the Clear Status Register command clears the status register error bits.

9. Program Suspend/Resume Flowchart



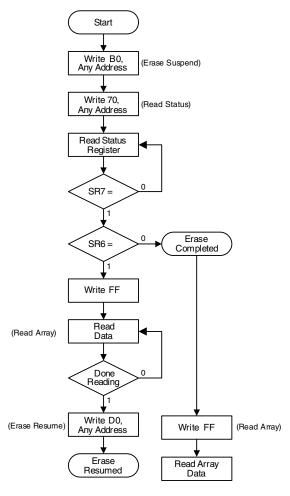
10. Program Suspend/Resume Procedure

Bus Operation	Command	Comments
Write	Read Status	Data = 70 Addr = Any address
Write	Program Suspend	Data = B0 Addr = Any address
Read	None	Status register data: Toggle \overline{CE} or \overline{OE} to update status register Addr = Any address
ldle	None	Check SR7 1 = WSM Ready 0 = WSM Busy
ldle	None	Check SR2 1 = Program suspended 0 = Program completed
Write	Read Array	Data = FF Addr = Any address
Read	None	Read data from any word in the memory
Write	Program Resume	Data = D0 Addr = Any address





11. Erase Suspend/Resume Flowchart



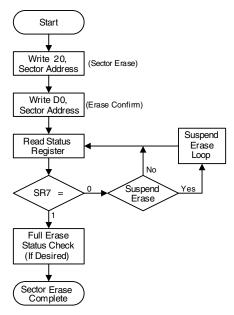
Bus Operation	Command	Comments
Write	Read Status	Data = 70 Addr = Any address
Write	Erase Suspend	Data = B0 Addr = Any address
Read	None	Status register data: Toggle \overline{CE} or \overline{OE} to update status register Addr = Any address
ldle	None	Check SR7 1 = WSM Ready 0 = WSM Busy
ldle	None	Check SR6 1 = Erase suspended 0 = Erase completed
Write	Read or Program	Data = FF or 40 Addr = Any address
Read or Write	None	Read or program data from/to sector other than the one being erased
Write	Program Resume	Data = D0 Addr = Any address

12. Erase Suspend/Resume Procedure

12 AT49BV160C(T)

3367F-FLASH-4/05

13. Sector Erase Flowchart



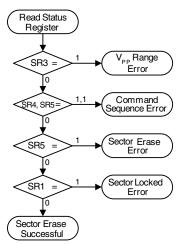
14. Sector Erase Procedure

Bus Operation	Command	Comments		
Write	Sector Erase Setup	Data = 20 Addr = Sector to be erased (SA)		
Write	Erase Confirm	Data = D0 Addr = Sector to be erased (SA)		
Read	None	Status register data: Toggle \overline{CE} or \overline{OE} to update status register data		
Idle	None	Check SR7 1 = WSM Ready 0 = WSM Busy		
	Repeat for subsequent sector erasures. Full status register check can be done after each sector erase,			

or after a sequence of sector erasures.

Write FF after the last operation to enter read mode.

15. Full Erase Status Check Flowchart



16. Full Erase Status Check Procedure

Bus Operation	Command	Comments
Idle	None	Check SR3: 1 = V _{PP} Range Error
Idle	None	Check SR4, SR5: Both 1 = Command Sequence Error
Idle	None	Check SR5: 1 = Sector Erase Error
Idle	None	Check SR1: 1 = Attempted erase of locked sector; erase aborted.

SR1, SR3 must be cleared before the Write State Machine allows further erase attempts.

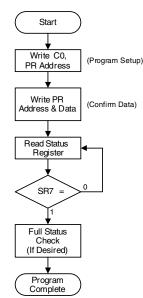
Only the Clear Status Register command clears SR1, SR3, SR4, SR5.

If an error is detected, clear the status register before attempting an erase retry or other error recovery.





17. Protection Register Programming Flowchart



18. Protection Register Programming Procedure

Bus Operation	Command	Comments		
Write	Program PR Setup	Data = C0 Addr = First Location to Program		
Write	Protection Program	Data = Data to Program Addr = Location to Program		
Read	None	Status register data: Toggle \overline{CE} or \overline{OE} to update status register data		
Idle	None	Check SR7 1 = WSM Ready 0 = WSM Busy		
Program Pro	Program Protection Register operation addresses must be			

Program Protection Register operation addresses must be within the protection register address space. Addresses outside this space will return an error.

Repeat for subsequent programming operations.

Full status register check can be done after each program, or after a sequence of program operations.

Write FF after the last operation to return to the Read mode.

20. Full Status Check Procedure

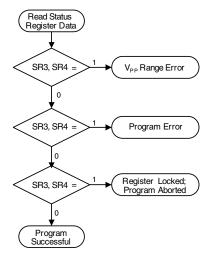
Bus Operation	Command	Comments
Idle	None	Check SR1, SR3, SR4: 0,1,1 = V _{PP} Range Error
Idle	None	Check SR1, SR3, SR4: 0,0,1 = Programming Error
Idle	None	Check SR1, SR3, SR4: 1, 0,1 = Sector locked; operation aborted

SR3 must be cleared before the Write State Machine allows further program attempts.

Only the Clear Status Register command clears SR1, SR3, SR4.

If an error is detected, clear the status register before attempting a program retry or other error recovery.

19. Full Status Check Flowchart



21. Command Definition Table

	Bus	1st Bus Cycle		2nd Bus Cycle	
Command Sequence	Cycles	Addr	Data	Addr	Data
Read	1	XX	FF		
Sector Erase/Confirm	2	XX	20	SA ⁽²⁾	D0
Word Program	2	XX	40/10	Addr	D _{IN}
Erase/Program Suspend	1	XX	B0		
Erase/Program Resume	1	XX	D0		
Product ID Entry	1	XX	90		
Sector Softlock	2	XX	60	SA ⁽²⁾	01
Sector Hardlock	2	XX	60	SA ⁽²⁾	2F
Sector Unlock	2	XX	60	SA ⁽²⁾	D0
Read Status Register	2	XX	70	XX	D _{OUT} ⁽³⁾
Clear Status Register	1	XX	50		
Program Protection Register	2	XX	CO	Addr	D _{IN}
Lock Protection Register – Sector B	2	XX	C0	80	FFFD
Status of Sector B Protection	2	XX	90	80	D _{OUT} ⁽⁴⁾
CFI Query	1	XX	98		

Notes: 1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). I/O15 - I/O8 are don't care. The ADDRESS FORMAT shown for each bus cycle is as follows: A7 - A0 (Hex). Address A19 through A8 are don't care.

- 2. SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 17 and 18 for details).
- 3. The status register bits are output on I/O7 I/O0.
- 4. If data bit D1 is "0", sector B is locked. If data bit D1 is "1", sector B can be reprogrammed.

22. Absolute Maximum Ratings*

Temperature under Bias55°C to +125°C
Storage Temperature65°C to +150°C
All Input Voltages
(including NC Pins) with Respect to Ground0.6V to +6.25V
All Output Voltages with Respect to Ground0.6V to V_{CC} + 0.6V
Voltage on V _{PP} with Respect to Ground0.6V to +13.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





23. Protection Register Addressing Table

Word	Use	Sector	A7	A6	A5	A 4	A3	A2	A1	A0
0	Factory	А	1	0	0	0	0	0	0	1
1	Factory	Α	1	0	0	0	0	0	1	0
2	Factory	Α	1	0	0	0	0	0	1	1
3	Factory	Α	1	0	0	0	0	1	0	0
4	User	В	1	0	0	0	0	1	0	1
5	User	В	1	0	0	0	0	1	1	0
6	User	В	1	0	0	0	0	1	1	1
7	User	В	1	0	0	0	1	0	0	0

Note: All address lines not specified in the above table must be "0" when accessing the protection register, i.e., A19 - A8 = 0.

16 AT49BV160C(T)

24. AT49BV160C – Sector Address Table

Sector	Size (Bytes/Words)	Address Range (A19 - A0)
SA0	8K/4K	00000 - 00FFF
SA1	8K/4K	01000 - 01FFF
SA2	8K/4K	02000 - 02FFF
SA3	8K/4K	03000 - 03FFF
SA4	8K/4K	04000 - 04FFF
SA5	8K/4K	05000 - 05FFF
SA6	8K/4K	06000 - 06FFF
SA7	8K/4K	07000 - 07FFF
SA8	64K/32K	08000 - 0FFFF
SA9	64K/32K	10000 - 17FFF
SA10	64K/32K	18000 - 1FFFF
SA11	64K/32K	20000 - 27FFF
SA12	64K/32K	28000 - 2FFFF
SA13	64K/32K	30000 - 37FFF
SA14	64K/32K	38000 - 3FFFF
SA15	64K/32K	40000 - 47FFF
SA16	64K/32K	48000 - 4FFFF
SA17	64K/32K	50000 - 57FFF
SA18	64K/32K	58000 - 5FFFF
SA19	64K/32K	60000 - 67FFF
SA20	64K/32K	68000 - 6FFFF
SA21	64K/32K	70000 - 77FFF
SA22	64K/32K	78000 - 7FFFF
SA23	64K/32K	80000 - 87FFF
SA24	64K/32K	88000 - 8FFFF
SA25	64K/32K	90000 - 97FFF
SA26	64K/32K	98000 - 9FFFF
SA27	64K/32K	A0000 - A7FFF
SA28	64K/32K	A8000 - AFFF
SA29	64K/32K	B0000 - B7FFF
SA30	64K/32K	B8000 - BFFFF
SA31	64K/32K	C0000 - C7FFF
SA32	64K/32K	C8000 - CFFFF
SA33	64K/32K	D0000 - D7FFF
SA34	64K/32K	D8000 - DFFFF
SA35	64K/32K	E0000 - E7FFF
SA36	64K/32K	E8000 - EFFFF
SA37	64K/32K	F0000 - F7FFF
SA38	64K/32K	F8000 - FFFF





18 AT49BV160C(T)

		x16		
Sector	Size (Bytes/Words)	Address Range (A19 - A0)		
SA0	64K/32K	00000 - 07FFF		
SA1	64K/32K	08000 - 0FFFF		
SA2	64K/32K	10000 - 17FFF		
SA3	64K/32K	18000 - 1FFFF		
SA4	64K/32K	20000 - 27FFF		
SA5	64K/32K	28000 - 2FFFF		
SA6	64K/32K	30000 - 37FFF		
SA7	64K/32K	38000 - 3FFFF		
SA8	64K/32K	40000 - 47FFF		
SA9	64K/32K	48000 - 4FFFF		
SA10	64K/32K	50000 - 57FFF		
SA11	64K/32K	58000 - 5FFFF		
SA12	64K/32K	60000 - 67FFF		
SA13	64K/32K	68000 - 6FFFF		
SA14	64K/32K	70000 - 77FFF		
SA15	64K/32K	78000 - 7FFFF		
SA16	64K/32K	80000 - 87FFF		
SA17	64K/32K	88000 - 8FFFF		
SA18	64K/32K	90000 - 97FFF		
SA19	64K/32K	98000 - 9FFFF		
SA20	64K/32K	A0000 - A7FFF		
SA21	64K/32K	A8000 - AFFFF		
SA22	64K/32K	B0000 - B7FFF		
SA23	64K/32K	B8000 - BFFFF		
SA24	64K/32K	C0000 - C7FFF		
SA25	64K/32K	C8000 - CFFFF		
SA26	64K/32K	D0000 - D7FFF		
SA27	64K/32K	D8000 - DFFFF		
SA28	64K/32K	E0000 - E7FFF		
SA29	64K/32K	E8000 - EFFFF		
SA30	64K/32K	F0000 - F7FFF		
SA31	8K/4K	F8000 - F8FFF		
SA32	8K/4K	F9000 - F9FFF		
SA33	8K/4K	FA000 - FAFFF		
SA34	8K/4K	FB000 - FBFFF		
SA35	8K/4K	FC000 - FCFFF		
SA36	8K/4K	FD000 - FDFFF		
SA37	8K/4K	FE000 - FEFFF		
SA38	8K/4K	FF000 - FFFFF		

25. AT49BV160CT – Sector Address Table



26. DC and AC Operating Range

		AT49BV160C(T)-70
Operating Temperature (Case)	Ind.	-40°C - 85°C
V _{CC} Power Supply		2.65V to 3.6V

27. Operating Modes

Mode	CE	OE	WE	RESET	V _{PP}	Ai	I/O
Read	V _{IL}	V _{IL}	V _{IH}	V _{IH}	Х	Ai	D _{OUT}
Program/Erase ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	V _{IH}	V _{IHPP} ⁽⁵⁾	Ai	D _{IN}
Standby/Program Inhibit	V _{IH}	X ⁽¹⁾	х	V _{IH}	Х	Х	High-Z
	Х	х	V _{IH}	V _{IH}	Х		
Program Inhibit	Х	V _{IL}	х	V _{IH}	Х		
	Х	Х	х	V _{IH}	V _{ILPP} ⁽⁶⁾		
Output Disable	Х	V _{IH}	Х	V _{IH}	Х		High-Z
Reset	Х	Х	х	V _{IL}	Х	Х	High-Z
Product Identification						$A0 = V_{IL}, A1 - A19 = V_{IL}$	Manufacturer Code ⁽⁴⁾
Software				V _{IH}		A0 = V _{IH} , A1 - A19 = V _{IL}	Device Code ⁽⁴⁾

Notes: 1. X can be V_{IL} or V_{IH} .

2. Refer to "Program Cycle Waveforms" on page 24.

3. $V_{\rm H} = 12.0V \pm 0.5V$.

4. Manufacturer Code: 001FH, Device Code: 88C3H - AT49BV160C; 88C2H - AT49BV160CT

5. V_{IHPP} (min) = 0.9V; V_{IHPP} (max) = 1.95V.

6. V_{ILPP} (max) = 0.4V.





28. DC Characteristics

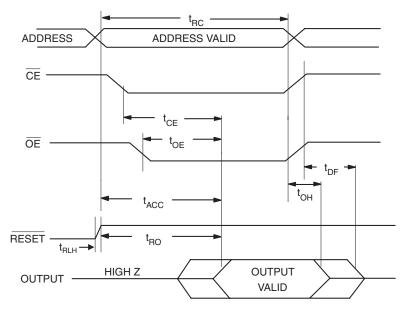
Symbol	Parameter	Condition	Min	Тур	Max	Units
I _{LI}	Input Load Current	$V_{IN} = 0V$ to V_{CC}			10	μΑ
I _{LO}	Output Leakage Current	$V_{I/O} = 0V$ to V_{CC}			10	μA
I _{SB}	V _{CC} Standby Current CMOS	$\overline{\text{CE}} = \text{V}_{\text{CC}} - 0.3\text{V} \text{ to } \text{V}_{\text{CC}}$		13	25	μA
I _{CC} ⁽¹⁾	V _{CC} Active Read Current	f = 5 MHz; I _{OUT} = 0 mA		12	25	mA
I _{CC1}	V _{CC} Programming Current				45	mA
I _{PP1}	V _{PP} Input Load Current				10	μΑ
V _{IL}	Input Low Voltage				0.4	V
V _{IH}	Input High Voltage		V _{CCQ} - 0.2			V
V _{OL}	Output Low Voltage	I _{OL} = 100 μA			0.10	V
V _{OH}	Output High Voltage	I _{OH} = -100 μA	V _{CCQ} - 0.1			V

Note: 1. In the erase mode, I_{CC} is 65 mA.

29. AC Read Characteristics

		AT49BV	AT49BV160C(T)-70	
Symbol	Parameter	Min	Max	Units
t _{RC}	Read Cycle Time	70		ns
t _{ACC}	Address to Output Delay		70	ns
t _{CE} ⁽¹⁾	CE to Output Delay		70	ns
t _{OE} ⁽²⁾	OE to Output Delay	0	20	ns
$t_{DF}^{(3)(4)}$	CE or OE to Output Float	0	25	ns
t _{OH}	Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first	0		ns
t _{RO}	RESET to Output Delay		100	ns
t _{RLH}	RESET Low to High Time		300	ns

30. AC Read Waveforms $^{(1)(2)(3)(4)}$



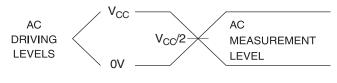
- Notes: 1. \overline{CE} may be delayed up to t_{ACC} t_{CE} after the address transition without impact on t_{ACC} . 2. \overline{OE} may be delayed up to t_{CE} t_{OE} after the falling edge of \overline{CE} without impact on t_{CE} or by t_{ACC} t_{OE} after an address change without impact on t_{ACC} . 3. t_{DF} is specified from \overrightarrow{OE} or \overrightarrow{CE} , whichever occurs first (CL = 5 pF).

 - 4. This parameter is characterized and is not 100% tested.



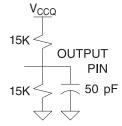


31. Input Test Waveforms and Measurement Level



 t_R , t_F < 5 ns

32. Output Test Load



33. Pin Capacitance

f = 1 MHz, T = $25^{\circ}C^{(1)}$

Symbol	Тур	Max	Units	Conditions
C _{IN}	4	6	pF	$V_{IN} = 0V$
C _{OUT}	8	12	pF	$V_{OUT} = 0V$

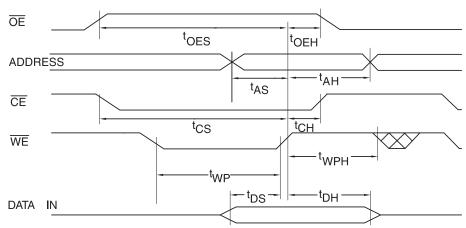
Note: This parameter is characterized and is not 100% tested.

34. AC Word Load Characteristics

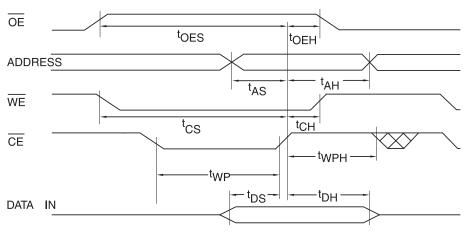
Symbol	Parameter	Min	Мах	Units
t _{AS} , t _{OES}	Address, OE Setup Time	45		ns
t _{AH}	Address Hold Time	0		ns
t _{cs}	Chip Select Setup Time	0		ns
t _{CH}	Chip Select Hold Time	0		ns
t _{wP}	Write Pulse Width (\overline{WE} or \overline{CE})	40		ns
t _{DS}	Data Setup Time	45		ns
t _{DH} , t _{OEH}	Data, OE Hold Time	0		ns
t _{WPH}	Write Pulse Width High	30		ns

35. AC Word Load Waveforms

35.1 WE Controlled



35.2 CE Controlled



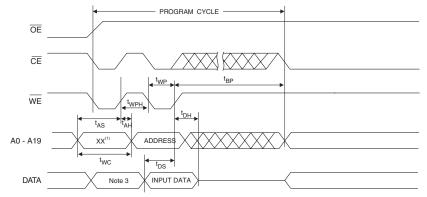




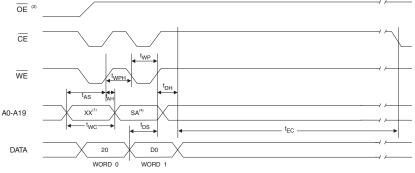
36. Program Cycle Characteristics

Symbol	Parameter	Min	Тур	Max	Units
t _{BP}	Word Programming Time		12	120	μs
t _{AS}	Address Setup Time	45			ns
t _{AH}	Address Hold Time	0			ns
t _{DS}	Data Setup Time	45			ns
t _{DH}	Data Hold Time	0			ns
t _{WP}	Write Pulse Width	40			ns
t _{WPH}	Write Pulse Width High	30			ns
t _{WC}	Write Cycle Time	70			ns
t _{RP}	Reset Pulse Width	500			ns
t _{SEC1}	Sector Erase Cycle Time (4K Word Sectors)		0.3	3.0	seconds
t _{SEC2}	Sector Erase Cycle Time (32K Word Sectors)		0.8	6.0	seconds
t _{ES}	Erase Suspend Time			15	μs
t _{PS}	Program Suspend Time			20	μs

37. Program Cycle Waveforms



38. Sector Erase Cycle Waveforms



- Notes: 1. Any address can be used to load the data.
 - 2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.
 - 3. The data can be 40H or 10H.
 - 4. The address depends on what sector is to be erased.

²⁴ AT49BV160C(T)

39. Common Flash Interface Definition Table

Address	AT49BV160CT	AT49BV160C	
10h	0051h	0051h	"Q"
11h	0052h	0052h	"R"
12h	0059h	0059h	"Y"
13h	0003h	0003h	
14h	0000h	0000h	
15h	0041h	0041h	
16h	0000h	0000h	
17h	0000h	0000h	
18h	0000h	0000h	
19h	0000h	0000h	
1Ah	0000h	0000h	
1Bh	0027h	0027h	VCC min write/erase
1Ch	0036h	0036h	VCC max write/erase
1Dh	00B5h	00B5h	VPP min voltage
1Eh	00C5h	00C5h	VPP max voltage
1Fh	0004h	0004h	Typ word write – 12 μs
20h	0000h	0000h	
21h	000Ah	000Ah	Typ sector erase, 1,000 ms
22h	0000h	0000h	Typ chip erase, not supported
23h	0003h	0003h	Max word write/typ time
24h	0000h	0000h	n/a
25h	0003h	0003h	Max sector erase/typ sector erase
26h	0000h	0000h	Max chip erase/ typ chip erase
27h	0015h	0015h	Device size
28h	0001h	0001h	x16 device
29h	0000h	0000h	x16 device
2Ah	0000h	0000h	Multiple byte write not supported
2Bh	0000h	0000h	Multiple byte write not supported
2Ch	0002h	0002h	2 regions, x = 2
2Dh	001Eh	0007h	64K bytes, Y = 30 (Top); 8K bytes, Y = 7 (Bottom)
2Eh	0000h	0000h	64K bytes, Y = 30 (Top); 8K bytes, Y = 7 (Bottom)
2Fh	0000h	0020h	64K bytes, Z = 256 (Top); 8K bytes, Z = 32 (Bottom)
30h	0001h	0000h	64K bytes, Z = 256 (Top); 8K bytes, Z = 32 (Bottom)
31h	0007h	001Eh	8K bytes, Y = 7 (Top); 64K bytes, Y = 30 (Bottom)
32h	0000h	0000h	8K bytes, Y = 7 (Top); 64K bytes, Y = 30 (Bottom)
33h	0020h	0000h	8K bytes, Z = 32 (Top); 64K bytes, Z = 256 (Bottom)
34h	0000h	0001h	8K bytes, Z = 32 (Top); 64K bytes, Z = 256 (Bottom)





39. Common Flash Interface Definition Table (Continued)

Address	AT49BV160CT	AT49BV160C				
	VENDOR SPECIFIC EXTENDED QUERY					
41h	0050h	0050h	"P"			
42h	0052h	0052h	"R"			
43h	0049h	0049h	"["			
44h	0031h	0031h	Major version number, ASCII			
45h	0030h	0030h	Minor version number, ASCII			
46h	0086h	0086h	Bit 0 – chip erase supported, 0 – no, 1 – yes Bit 1 – erase suspend supported, 0 – no, 1 – yes Bit 2 – program suspend supported, 0 – no, 1 – yes Bit 3 – simultaneous operations supported, 0 – no, 1 – yes Bit 4 – burst mode read supported, 0 – no, 1 – yes Bit 5 – page mode read supported, 0 – no, 1 – yes Bit 6 – queued erase supported, 0 – no, 1 – yes Bit 7 – protection bits supported, 0 – no, 1 – yes			
47h	0000h	0001h	Bit 8 – top ("0") or bottom ("1") boot sector device undefined bits are "0"			
48h	0000h	0000h	Bit 0 – 4 word linear burst with wrap around, 0 – no, 1 – yes Bit 1 – 8 word linear burst with wrap around, 0 – no, 1 – yes Bit 2 – continuos burst, 0 - no, 1 - yes Undefined bits are "0"			
49h	0000h	0000h	Bit 0 – 4 word page, 0 – no, 1 – yes Bit 1 – 8 word page, 0 – no, 1 – yes Undefined bits are "0"			
4Ah	0080h	0080h	Location of protection register lock byte, the section's first byte			
4Bh	0003h	0003h	# of bytes in the factory prog section of prot register - 2*n			
4Ch	0003h	0003h	# of bytes in the user prog section of prot register – 2*n			

40. Ordering Information

40.1 Standard Package

t _{ACC}	I _{CC} (mA)				
(ns)	Active	Standby	Ordering Code	Package	Operation Range
70 25	25	0.025	AT49BV160C-70CI	46C3	Industrial
	25		AT49BV160C-70TI	48T	(-40° to 85°C)
70	25	25 0.025	AT49BV160CT-70CI	46C3	Industrial
			AT49BV160CT-70TI	48T	(-40° to 85°C)

40.2 Green Package Option (Pb/Halide-free)

t _{ACC} I _{CC} (mA)		_; (mA)			
(ns)	Active	Standby	Ordering Code	Package	Operation Range
70	25	0.025	AT49BV160C-70TU	48T	Industrial (-40° to 85°C)
70	25	0.025	AT49BV160CT-70CU AT49BV160CT-70TU	46C3 48T	Industrial (-40° to 85°C)

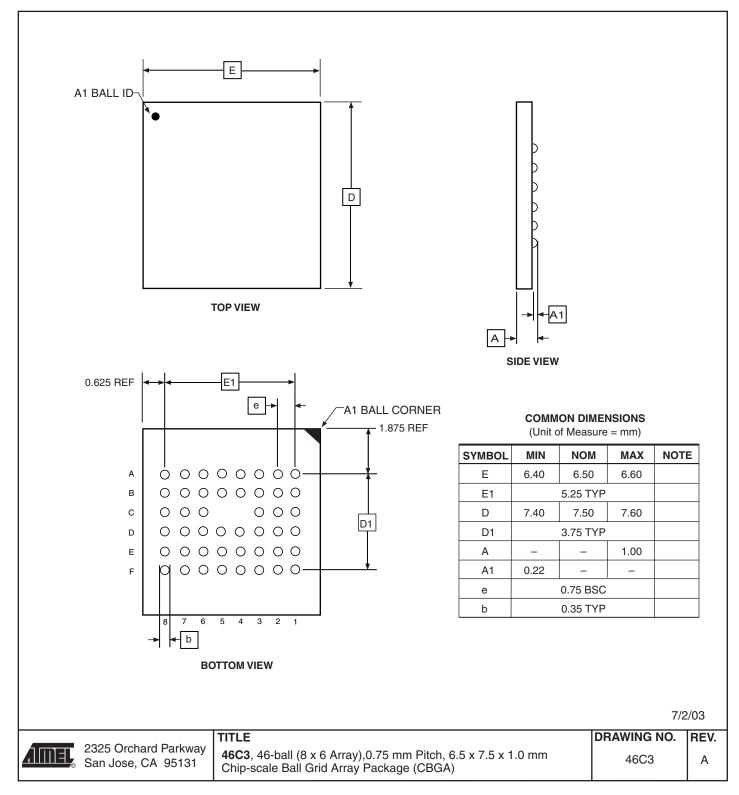
Package Type		
46C3	46-ball, Plastic Chip-Size Ball Grid Array Package (CBGA)	
48T	48-lead, Plastic Thin Small Outline Package (TSOP)	





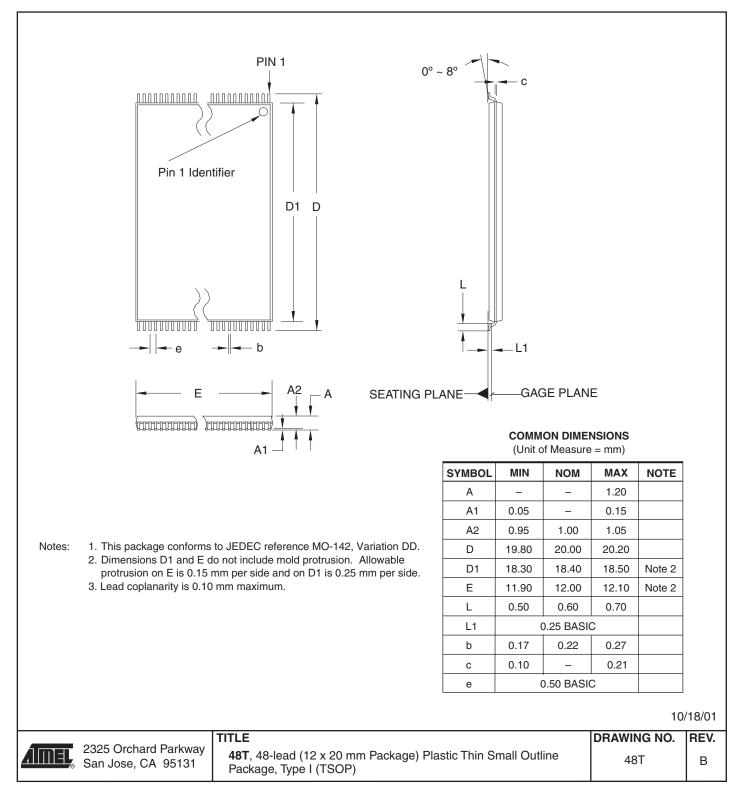
41. Packaging Information

41.1 46C3 - CBGA



AT49BV160C(T)

41.2 48T – TSOP







Atmel Corporation

2325 Orchard Parkway San Jose, CA 95131, USA Tel: 1(408) 441-0311 Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl Route des Arsenaux 41 Case Postale 80 CH-1705 Fribourg Switzerland Tel: (41) 26-426-5555 Fax: (41) 26-426-5500

Asia

Room 1219 Chinachem Golden Plaza 77 Mody Road Tsimshatsui East Kowloon Hong Kong Tel: (852) 2721-9778 Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan Tel: (81) 3-3523-3551 Fax: (81) 3-3523-7581

Atmel Operations

Memory 2325 Orchard Parkway San Jose, CA 95131, USA Tel: 1(408) 441-0311 Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway San Jose, CA 95131, USA Tel: 1(408) 441-0311 Fax: 1(408) 436-4314

La Chantrerie BP 70602 44306 Nantes Cedex 3, France Tel: (33) 2-40-18-18-18 Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle 13106 Rousset Cedex, France Tel: (33) 4-42-53-60-00 Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd. Colorado Springs, CO 80906, USA Tel: 1(719) 576-3300 Fax: 1(719) 540-1759

Scottish Enterprise Technology Park Maxwell Building East Kilbride G75 0QR, Scotland Tel: (44) 1355-803-000 Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2 Postfach 3535 74025 Heilbronn, Germany Tel: (49) 71-31-67-0 Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd. Colorado Springs, CO 80906, USA Tel: 1(719) 576-3300 Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/

High Speed Converters/RF Datacom Avenue de Rochepleine BP 123 38521 Saint-Egreve Cedex, France Tel: (33) 4-76-58-30-00 Fax: (33) 4-76-58-34-80

Literature Requests www.atmel.com/literature

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDI-TIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNTIVE, SPECIAL OR INCIDEN-TAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© Atmel Corporation 2005. All rights reserved. Atmel[®], logo and combinations thereof, and others, are registered trademarks, and Everywhere You AreSM and others are the trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.

