

24AA02E48

2K I²C[™] Serial EEPROM with EUI-48[™] Node Identity

Device Selection Table

Part	Vcc	Max. Clock	Temp.
Number	Range	Frequency	Ranges
24AA02E48	1.7-5.5V	400 kHz ⁽¹⁾	I

Note 1: 100 kHz for Vcc <2.5V

Features:

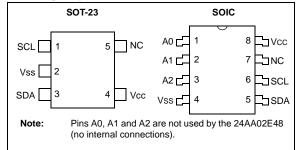
- Pre-programmed Globally Unique, 48-bit Node Address
- Compatible with EUI-48[™] and EUI-64[™]
- Single Supply with Operation Down to 1.7V
- Low-Power CMOS Technology:
 - Read current 1 mA, max.
- Standby current 1 µA, max.
- 2-Wire Serial Interface, I²C[™] Compatible
- Schmitt Trigger Inputs for Noise Suppression
- · Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Clock Compatibility
- Page Write Time 3 ms, typical
- Self-Timed Erase/Write Cycle
- 8-Byte Page Write Buffer
- ESD Protection >4,000V
- More than 1 Million Erase/Write Cycles
- Data Retention >200 Years
- Factory Programming Available
- Packages include 8-lead SOIC and 5-lead SOT-23
- Pb-free and RoHS Compliant
- Temperature Ranges:
 - Industrial (I): -40°C to +85°C

Note: This document is supplemented by the "24AA02 Data Sheet" (DS21709). See Section 2.0 "Functional Description".

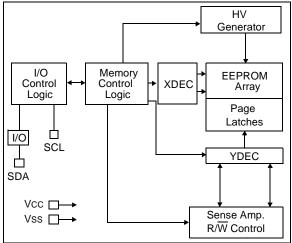
Description:

The Microchip Technology Inc. 24AA02E48 is a 2 Kbit Electrically Erasable PROM. The device is organized as two blocks of 128 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.7V, with maximum standby and active currents of only 1 μ A and 1 mA, respectively. The 24AA02E48 also has a page write capability for up to 8 bytes of data. The 24AA02E48 is available in the standard 8-pin SOIC and 5-lead SOT-23 packages.

Package Types



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Vcc	6.5V
All inputs and outputs w.r.t. Vss	-0.3V to Vcc +1.0V
Storage temperature	65°C to +150°C
Ambient temperature with power applied	-40°C to +85°C
ESD protection on all pins	≥ 4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): Ta	$= -40^{\circ}$ C to	+85°C, \	/cc = +1.7V to +5.5V
Param. No.	Sym.	Characteristic	Min.	Тур.	Max.	Units	Conditions
D1	Vih	WP, SCL and SDA pins	_	—	—		—
D2	—	High-level Input Voltage	0.7 Vcc	—	—	V	—
D3	VIL	Low-level Input Voltage	—	—	0.3 Vcc	V	—
D4	VHYS	Hysteresis of Schmitt Trigger inputs	0.05 Vcc	—	—	V	(Note)
D5	Vol	Low-level Output Voltage	—	—	0.40	V	IOL = 3.0 mA, VCC = 2.5V
D6	LI	Input Leakage Current	_	—	±1	μA	VIN = VSS or VCC
D7	Ilo	Output Leakage Current	—	_	±1	μA	VOUT = VSS or VCC
D8	CIN, COUT	Pin Capacitance (all inputs/outputs)	_	_	10	pF	Vcc = 5.0V (Note) Ta = 25°C, Fclk = 1 MHz
D9	ICC write	Operating Current	—	0.1	3	mA	Vcc = 5.5V, SCL = 400 kHz
D10	ICC read		—	0.05	1	mA	—
D11	Iccs	Standby Current		0.01	1	μΑ	Industrial SDA = SCL = VCC WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS		Industrial (I): $TA = -40^{\circ}C$ to $+85^{\circ}C$, $VCC = +1.7V$ to $+5.5V$				C, VCC = +1.7V to +5.5V	
Param. No.	Sym.	Characteristic	Min.	Тур.	Max.	Units	Conditions
1	FCLK	Clock frequency	—	_	400 100	kHz	$\begin{array}{l} 2.5V \leq VCC \leq 5.5V \\ 1.7V \leq VCC < 2.5V \end{array}$
2	THIGH	Clock high time	600 4000	_	_	ns	$\begin{array}{l} 2.5 V \leq V C C \leq 5.5 V \\ 1.7 V \leq V C C < 2.5 V \end{array}$
3	TLOW	Clock low time	1300 4700	_	_	ns	$\begin{array}{l} 2.5 V \leq V C C \leq 5.5 V \\ 1.7 V \leq V C C < 2.5 V \end{array}$
4	TR	SDA and SCL rise time (Note 1)	—	_	300 1000	ns	$2.5V \le VCC \le 5.5V$ (Note 1) $1.7V \le VCC < 2.5V$ (Note 1)
5	TF	SDA and SCL fall time	—	_	300	ns	(Note 1)
6	THD:STA	Start condition hold time	600 4000	_	_	ns	$\begin{array}{l} 2.5V \leq VCC \leq 5.5V \\ 1.7V \leq VCC < 2.5V \end{array}$
7	TSU:STA	Start condition setup time	600 4700	_	_	ns	$\begin{array}{l} 2.5 V \leq V C C \leq 5.5 V \\ 1.7 V \leq V C C < 2.5 V \end{array}$
8	THD:DAT	Data input hold time	0	_	—	ns	(Note 2)
9	TSU:DAT	Data input setup time	100 250	_	_	ns	$\begin{array}{l} 2.5V \leq VCC \leq 5.5V \\ 1.7V \leq VCC < 2.5V \end{array}$
10	Tsu:sto	Stop condition setup time	600 4000	_	_	ns	$\begin{array}{l} 2.5V \leq VCC \leq 5.5V \\ 1.7V \leq VCC < 2.5V \end{array}$
11	ΤΑΑ	Output valid from clock (Note 2)	—	_	900 3500	ns	$\begin{array}{l} 2.5V \leq VCC \leq 5.5V \\ 1.7V \leq VCC < 2.5V \end{array}$
12	TBUF	Bus free time: Time the bus must be free before a new transmission can start	1300 4700	_	_	ns	$2.5V \le Vcc \le 5.5V$ $1.7V \le Vcc < 2.5V$
13	Tof	Output fall time from VIH minimum to VIL maximum	—	_	250 250	ns	$\begin{array}{l} 2.5V \leq Vcc \leq 5.5V \\ 1.7V \leq Vcc < 2.5V \end{array}$
14	TSP	Input filter spike suppression (SDA and SCL pins)	—	_	50	ns	(Notes 1 and 3)
15	Twc	Write cycle time (byte or page)	—	—	5	ms	—
16	—	Endurance	1M	—	—	cycles	25°C (Note 4)

TABLE 1-2: AC CHARACTERISTICS

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

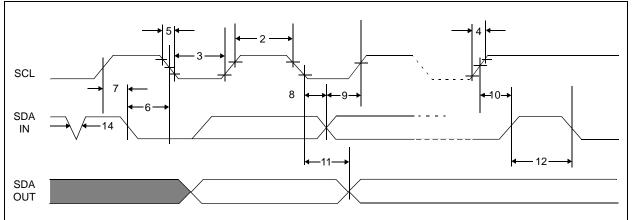
3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance[™] Model which can be obtained from Microchip's web site at www.microchip.com.

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24AA02E48





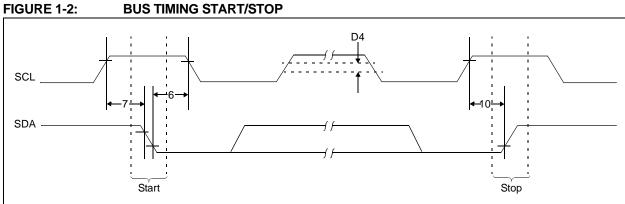


FIGURE 1-2:

2.0 FUNCTIONAL DESCRIPTION

The 24AA02E48 supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24AA02E48 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

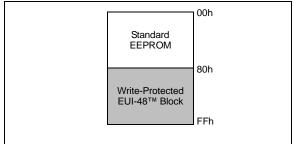
Note: This data sheet documents only the device's features and specifications that are in addition to the features and specifications of the 24AA02 device. For information on the features and specifications shared by the 24AA02E48 and 24AA02 devices, see the "24AA02 Data Sheet" (DS21709).

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3.0 PRE-PROGRAMMED EUI-48™ NODE ADDRESS

The 24AA02E48 is programmed at the factory with a globally unique, EUI-48TM and EUI-64TM compatible node address stored in the upper half of the array and permanently write-protected. The remaining 1,024 bits are available for application use.

FIGURE 3-1: MEMORY ORGANIZATION

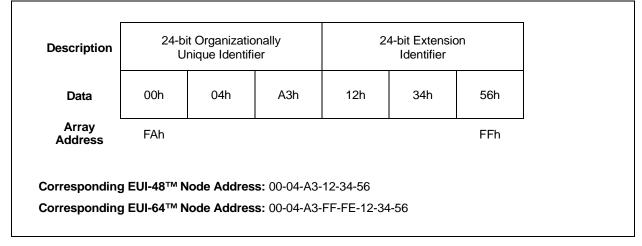


The 6-byte EUI-48 node address value is stored in array locations 0xFA through 0xFF, as shown in Figure 3-2. The first 3 bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining 3 bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 48-bit value.

3.1 EUI-64[™] Support

The pre-programmed EUI-48 node address can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by adding 0xFFFE between the OUI and the Extension Identifier, as shown below.

FIGURE 3-2: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE



4.0 WRITE PROTECTION

The upper half of the array (80h-FFh) is permanently write-protected. Write operations to this address range are inhibited. Read operations are not affected.

The remaining half of the array (00h-7Fh) can be written to and read from normally.

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5.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 5-1.

Name	SOIC	SOT23	Description
A0	1	—	Not Connected
A1	2	—	Not Connected
A2	3	—	Not Connected
Vss	4	2	Ground
SDA	5	3	Serial Address/Data I/O
SCL	6	1	Serial Clock
NC	7	5	Not Connected
Vcc	8	4	+1.7V to 5.5V Power Supply

TABLE 5-1: PIN FUNCTION TABLE

5.1 Serial Address/Data Input/Output (SDA)

SDA is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an opendrain terminal, the SDA bus requires a pull-up resistor to Vcc (typical 10 k Ω for 100 kHz, 2 k Ω for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating Start and Stop conditions.

5.2 Serial Clock (SCL)

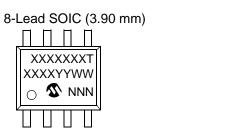
The SCL input is used to synchronize the data transfer to and from the device.

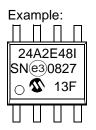
5.3 A0, A1, A2

These A0, A1 and A2 pins are not used by the 24AA02E48. They may be left floating or tied to either Vss or Vcc.

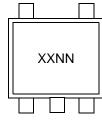
6.0 PACKAGING INFORMATION

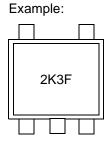
6.1 Package Marking Information





5-Lead SOT-23





	1st Line Marking Code	
Part Number	SOT-23	
	l Temp.	
24AA02E48	2KNN	

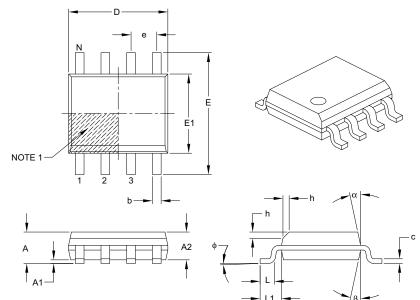
Note: NN = Alphanumeric traceability code

Legend	T Temperat Y Year code YY Year code WW Week coo NNN Alphanum	ber or part number code ure (I, E) e (last digit of calendar year) e (last 2 digits of calendar year) de (week of January 1 is week '01') neric traceability code (2 characters for small packages) EDEC designator for Matte Tin (Sn)			
Note:	Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.				
Note:	be carried over to	Aicrochip part number cannot be marked on one line, it will the next line, thus limiting the number of available ner-specific information.			

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

*Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

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For the most current package drawings, please see the Microchip Packaging Specification located at

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

http://www.microchip.com/packaging

MILLIMETERS Units NOM **Dimension Limits** MIN MAX Number of Pins Ν 8 Pitch 1.27 BSC е **Overall Height** А _ 1.75 Molded Package Thickness A2 1.25 Standoff § 0.10 0.25 A1 _ Overall Width Е 6.00 BSC Molded Package Width 3.90 BSC E1 **Overall Length** D 4.90 BSC Chamfer (optional) h 0.25 0.50 _ Foot Length 0.40 1.27 L Footprint 1.04 REF L1 0° 8° Foot Angle ø _ Lead Thickness С 0.17 0.25 _ Lead Width b 0.31 _ 0.51 Mold Draft Angle Top 5° 15° _ α Mold Draft Angle Bottom 5° 15° β _

Notes:

Note:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

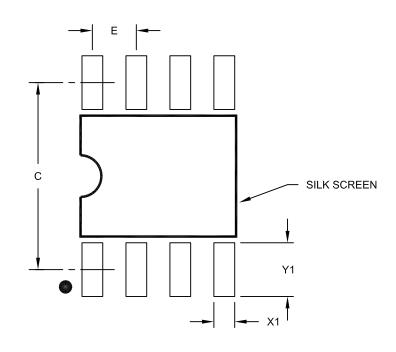
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	N	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Е		1.27 BSC	
Contact Pad Spacing	С		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

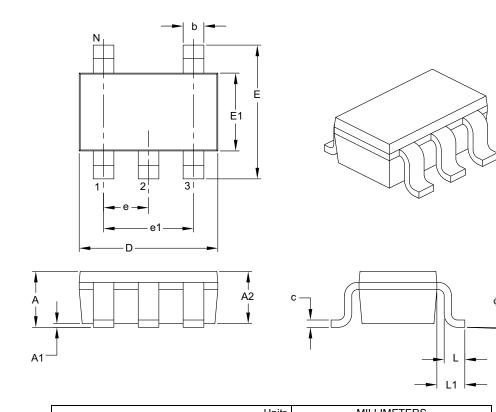
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

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For the most current package drawings, please see the Microchip Packaging Specification located at

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

http://www.microchip.com/packaging

	Units		MILLIMETERS	6
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	е	0.95 BSC		
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	А	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	0.00	-	0.15
Overall Width	E	2.20	-	3.20
Molded Package Width	E1	1.30	-	1.80
Overall Length	D	2.70	-	3.10
Foot Length	L	0.10	-	0.60
Footprint	L1	0.35	-	0.80
Foot Angle	ф	0°	-	30°
Lead Thickness	С	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

Note:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.

2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

APPENDIX A: REVISION HISTORY

Revision A (12/08)

Original release of this document.

Revision B (01/09)

Removed preliminary status.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART N Device		Examples: a) 24AA02E48-I/SN: Industrial Tempera- ture, 1.7V, SOIC package b) 24AA02E48T-I/OT: Industrial Tempera-
Device:	24AA02E48: = 1.7V, 2 Kbit I ² C Serial EEPROM with EUI-48 [™] Node Identity 24AA02E48T: = 1.7V, 2 Kbit I ² C Serial EEPROM with EUI-48 [™] Node Identity (Tape and Reel)	ture, 1.7V, SOT-23 package, tape and reel
Temperature Range:	$I = -40^{\circ}C \text{ to } +85^{\circ}C$	
Package:	SN = Plastic SOIC (3.90 mm body), 8-lead OT = SOT-23, 5-lead (Tape and Reel only)	

24AA02E48

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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