

24LC174

16K 2.5V Cascadable I²C™ Serial EEPROM with OTP Security Page

FEATURES

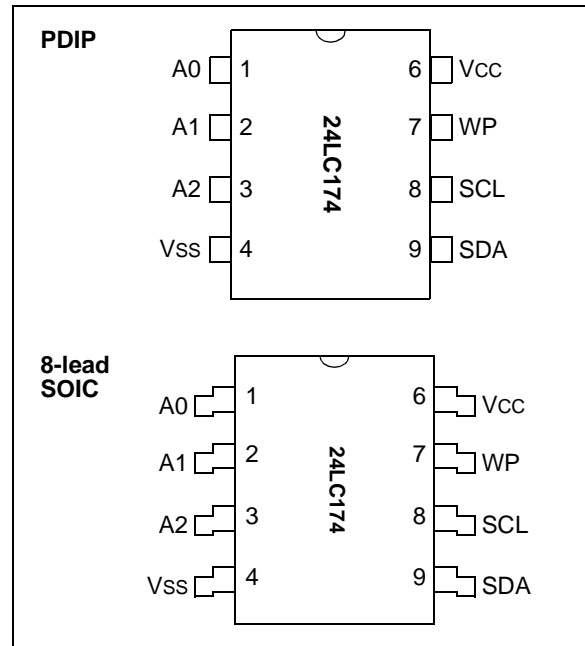
- Single supply with operation down to 2.5V
- 16 bytes OTP Secure Memory
- Low power CMOS technology
 - 1 mA active current typical
 - 10 μ A standby current typical at 5.5V
 - 5 μ A standby current typical at 3.0V
- Organized as eight blocks of 256 bytes (8 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Functional address inputs for cascading up to 8 devices
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 Erase/Write cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead SOIC packages
- Available temperature ranges:
 - Commercial (C): 0°C to +70°C
 - Industrial (I): -40° to +85°

DESCRIPTION

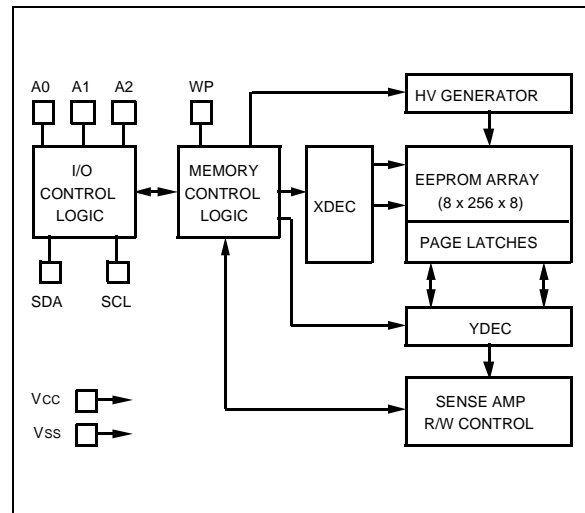
The Microchip Technology Inc. 24LC174 is a cascadable 16K bit Electrically Erasable PROM. The device is organized as eight blocks of 256 x 8-bit memory with a 2-wire serial interface and provides a specially addressed OTP (one-time programmable) 16 byte security block. Low voltage design permits operation down to 2.5 volts with standby and active currents of only 5 μ A and 1 mA respectively. The 24LC174 also has a page-write capability for up to 16 bytes of data. The 24LC174 is available in the standard 8-pin DIP and 8-lead surface mount SOIC packages.

The three select pins, A0, A1, and A2, function as chip select inputs and allow up to eight devices to share a common bus, for up to 128K bits total system EEPROM.

PACKAGE TYPES



BLOCK DIAGRAM



I²C is a trademark of Philips Corporation.

24LC174

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC}.....7.0V
 All inputs and outputs w.r.t. V_{SS} -0.3V to V_{CC} +1.0V
 Storage temperature -65°C to +150°C
 Ambient temp. with power applied -65°C to +125°C
 Soldering temperature of leads (10 seconds) +300°C
 ESD protection on all pins ≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
V _{SS}	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
V _{CC}	+2.5V to 5.5V Power Supply
A0, A1, A2	Chip Address Inputs

TABLE 1-2: DC CHARACTERISTICS

V _{CC} = +2.5V to 5.5V Commercial (C): T _{amb} = 0°C to +70°C Industrial (I): T _{amb} = -40°C to +85°C					
Parameter	Symbol	Min	Max	Units	Conditions
WP, SCL and SDA pins: High level input voltage	V _{IH}	.7 V _{CC}	—	V	(Note) I _{OL} = 3.0 mA, V _{CC} = 2.5V
Low level input voltage	V _{IL}	—	.3 V _{CC}	V	
Hysteresis of Schmitt trigger inputs	V _{HYS}	.05 V _{CC}	—	V	
Low level output voltage	V _{OL}	—	.40	V	
Input leakage current	I _{LI}	-10	10	μA	V _{IN} = .1V to V _{CC}
Output leakage current	I _{LO}	-10	10	μA	V _{OUT} = .1V to V _{CC}
Pin capacitance (all inputs/outputs)	C _{IN} , C _{OUT}	—	10	pF	V _{CC} = 5.0V (Note1), T _{amb} = 25°C, F _{CLK} = 1 MHz
Operating current	I _{CC} Write I _{CC} Read	—	3 1	mA mA	V _{CC} = 5.5V, SCL = 400 kHz
Standby current	I _{CCS}	—	30 100	μA μA	V _{CC} = 3.0V, SDA = SCL = V _{CC} V _{CC} = 5.5V, SDA = SCL = V _{CC} WP = V _{SS}

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

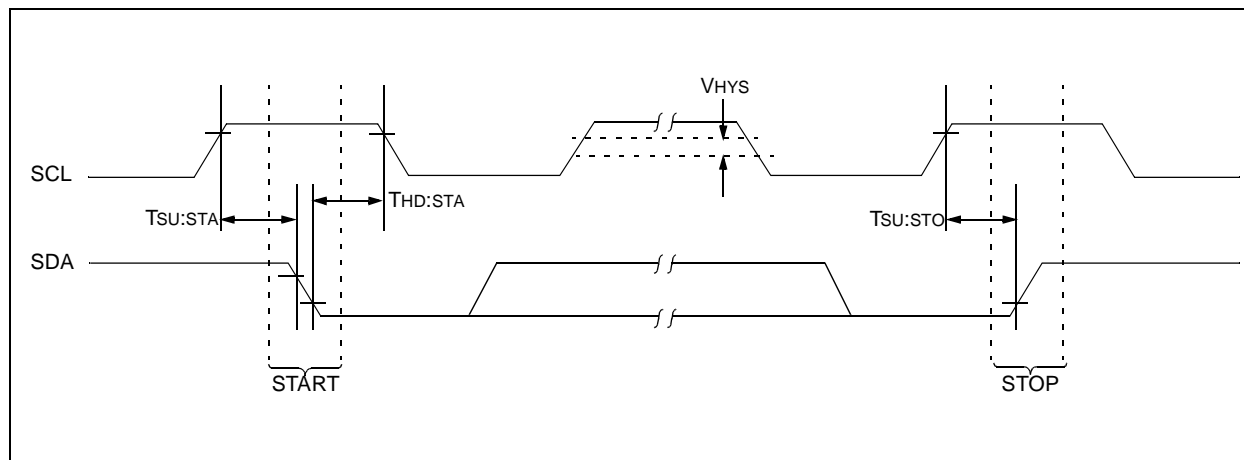


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Standard Mode		Vcc= 4.5 - 5.5V Fast Mode		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 Cb	250	ns	(Note 1), Cb ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	10	—	10	ms	Byte or Page mode
Endurance	—	1M	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 4)

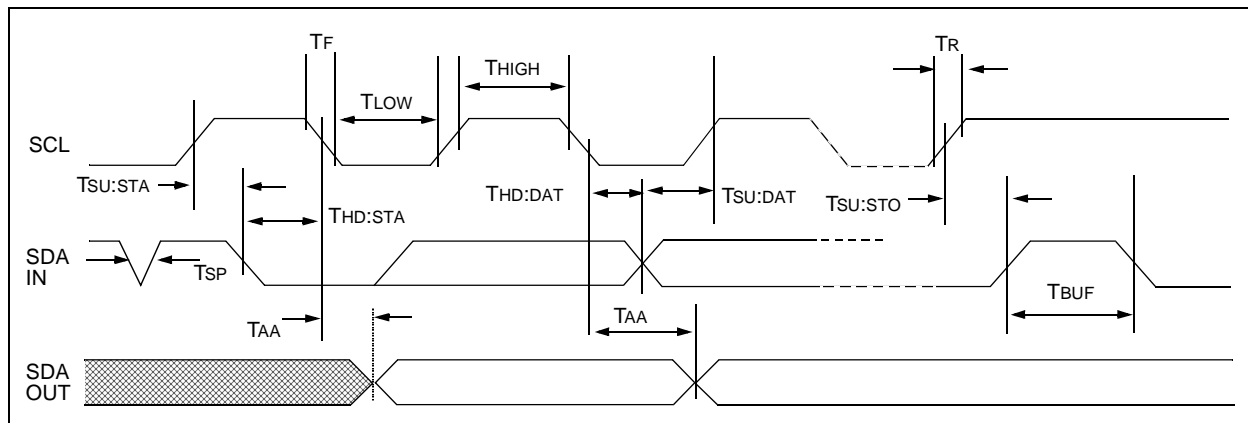
Note 1: Not 100% tested. Cb = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our website.

FIGURE 1-2: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC174 supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC174 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

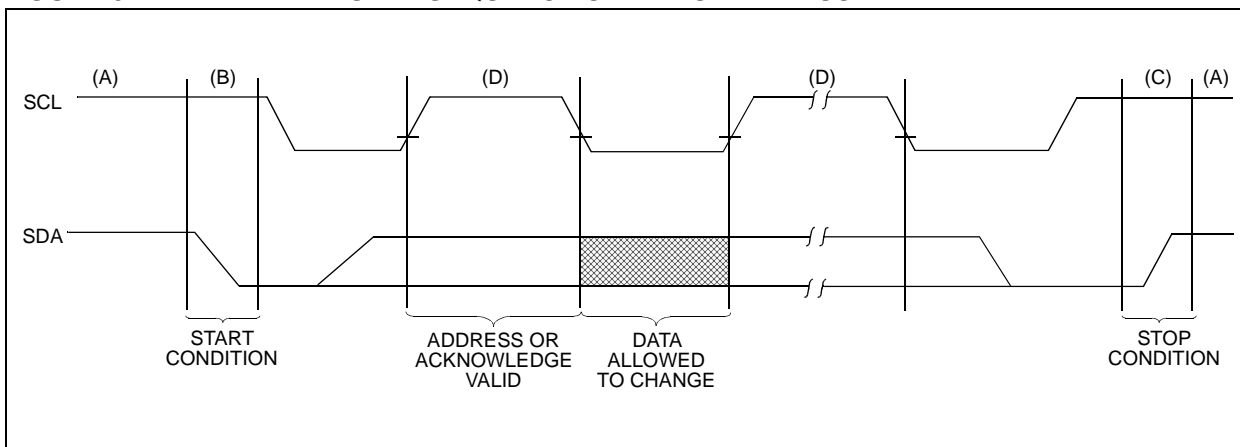
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24LC174 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24LC174) will leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing and Operation

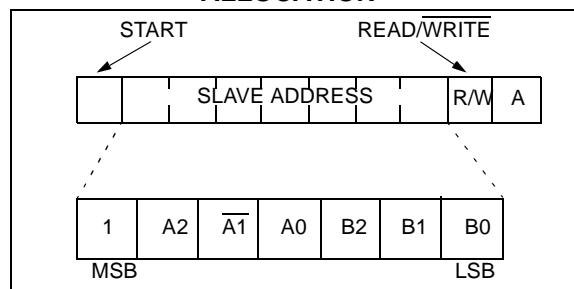
A control byte is the first byte received following the start condition from the master device. The first bit is always a one. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used to select which of the eight devices are to be accessed. The A1 bit must be the inverse of the A1 device select pin.

The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC174 looks for the slave address for the device selected. Depending on the state of the R/W bit, the 24LC174 will select a read or write operation.

Operation	Control Code	Block Select	R/W
Read	1 A2 $\overline{A1}$ A0	Block Address	1
Write	1 A2 $A1$ A0	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/W bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC174. After receiving another acknowledge signal from the 24LC174 the master device will transmit the data word to be written into the addressed memory location. The 24LC174 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC174 will not generate acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC174 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24LC174 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 7.3).

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a page write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 4-1: BYTE WRITE

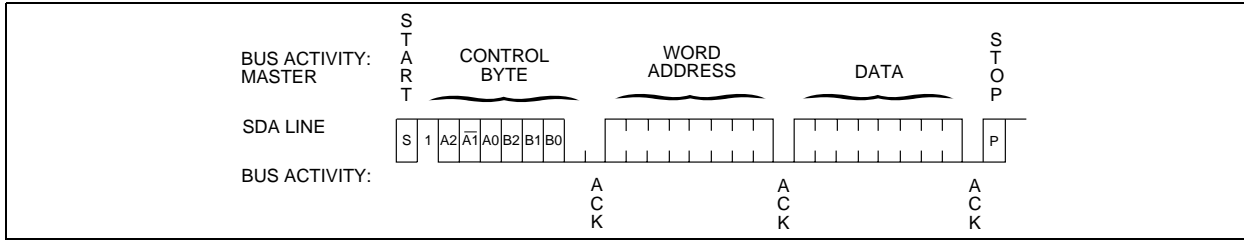
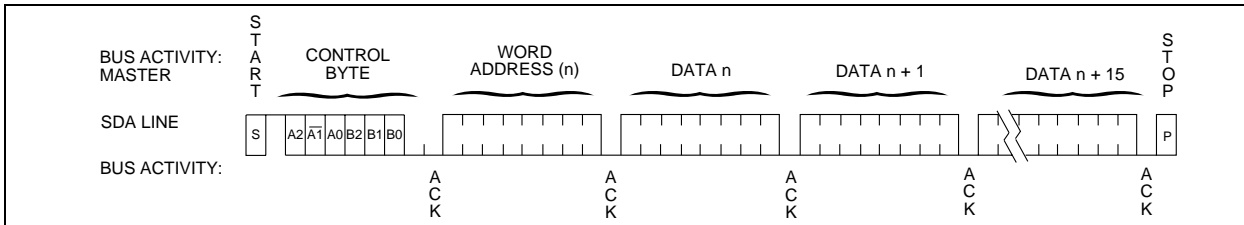


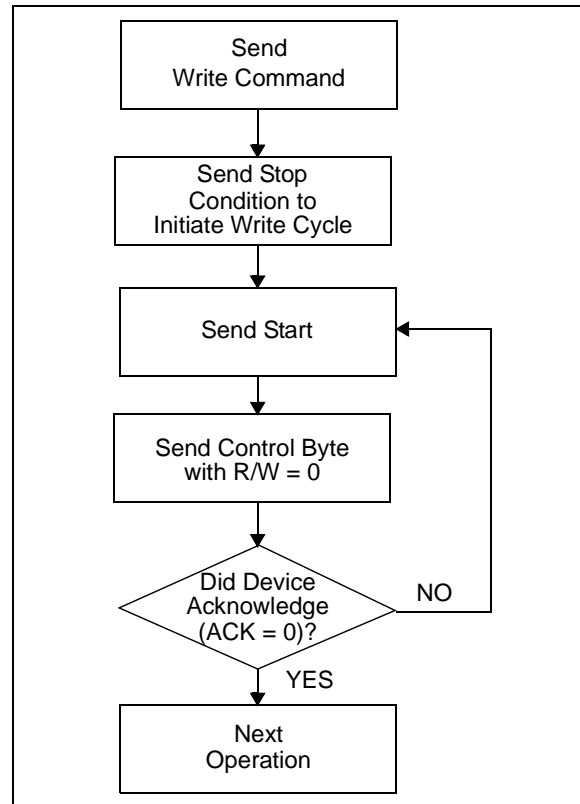
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\bar{W} = 0$). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 WRITE PROTECTION

The 24LC174 can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/\bar{W} bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24LC174 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n , the next current address read operation would access data from address $n + 1$. Upon receipt of the slave address with R/\bar{W} bit set to one, the 24LC174 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC174 discontinues transmission (Figure 8-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC174 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/\bar{W} bit set to a one. The 24LC174 will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC174 discontinues transmission (Figure 8-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC174 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC174 to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads the 24LC174 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows an entire device memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC174 employs a V_{CC} threshold detector circuit which disables the internal erase/write logic if the V_{CC} is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

8.0 PIN DESCRIPTIONS

8.1 SDA Serial Address/Data Input/Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to Vcc (typical 10KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3 WP

This pin must be connected to either Vss or Vcc.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

If tied to Vcc, WRITE operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC174 as a serial ROM when WP is enabled (tied to Vcc).

8.4 A0, A1, A2

These pins are used to configure the proper chip address in multiple-chip applications (more than one 24LC174 on the same bus). The levels on these pins are compared to the corresponding bits in the slave address. The chip is selected if the compare is true.

Note: The level on A1 is compared to the inverse of the slave address.

Up to eight 24LC174s may be connected to the same bus. These pins must be connected to either Vss or Vcc.

8.5 Security Access Control

The security row is enabled by sending the control sequence with the I²C slave address of 0110. Bit 0 of the control byte must be set to a one for a READ OPERATION or a zero for the OTP WRITE OPERATION. The SECURITY ACCESS DATA is always read starting at byte 0 for N bytes up to and including byte 15. (See Figure 8-3).

8.6 Security Access Write

The S.A.W. data is written to the device using a normal page write following the proper control access sequence. Upon receiving the final stop bit, the internal write sequence will commence. At the completion of the internal write sequence a fuse will be set disabling the write function for the 16 byte security page.

8.7 Security Access Read

The security access read is accomplished by executing the normal read sequences, following the security access control sequence with bit 0 set to a one. The security page read starts at data byte 0.

FIGURE 8-1: CURRENT ADDRESS READ

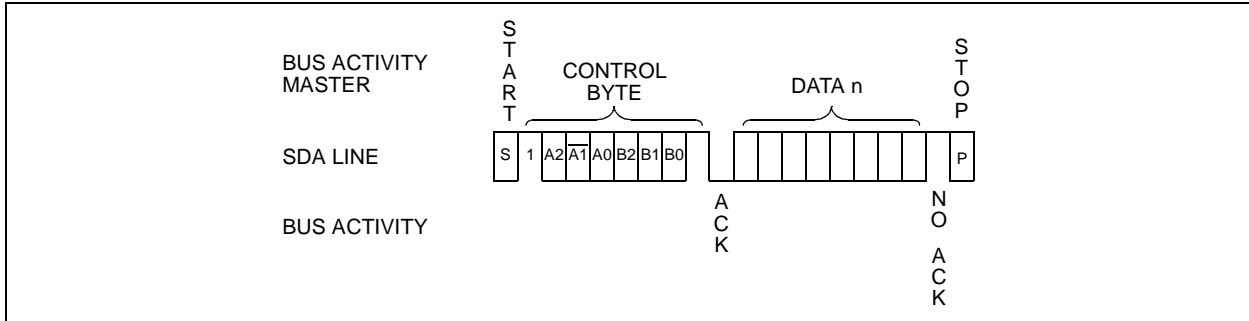


FIGURE 8-2: RANDOM READ

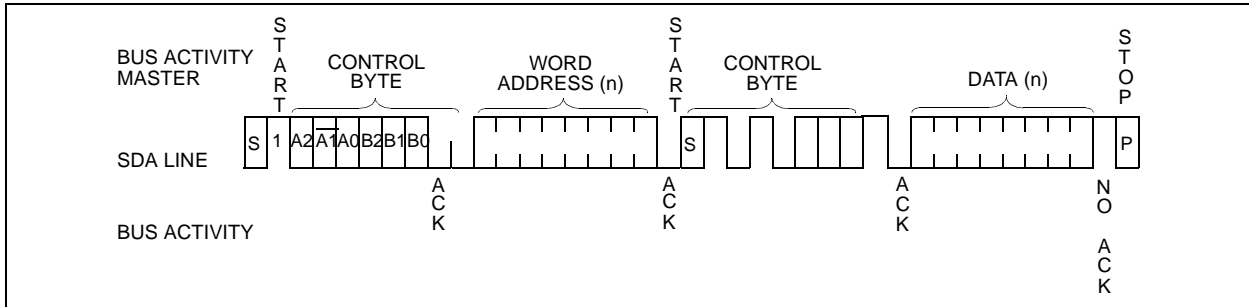


FIGURE 8-3: SEQUENTIAL READ

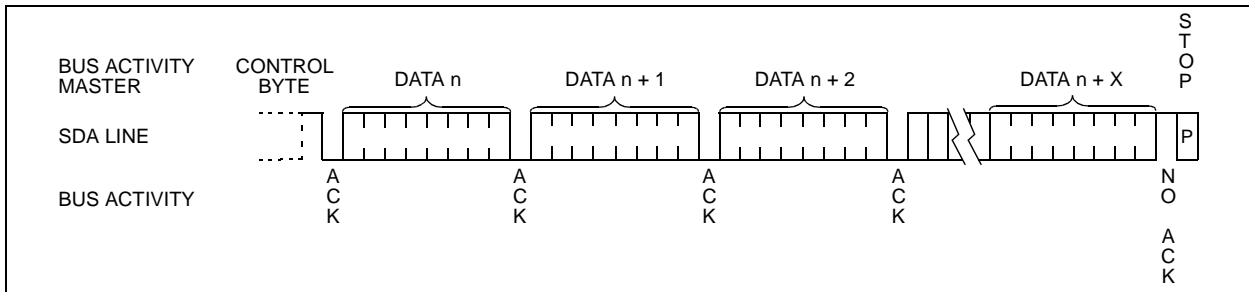


FIGURE 8-4: SECURITY CONTROL BYTE ALLOCATION

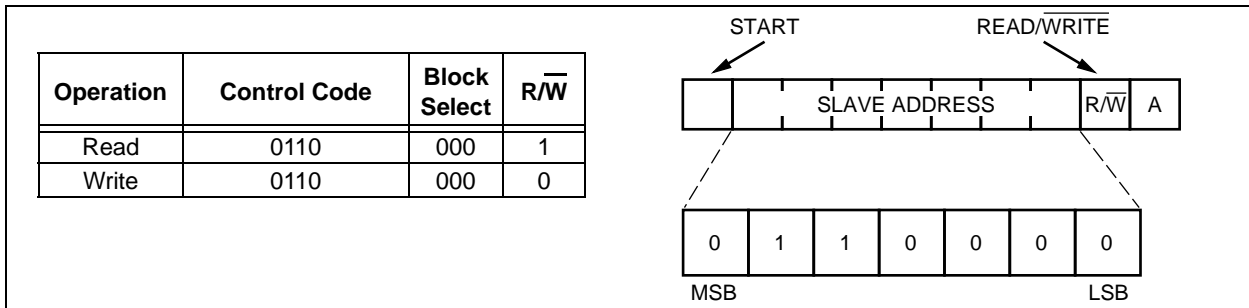


FIGURE 8-5: SECURITY PAGE READ

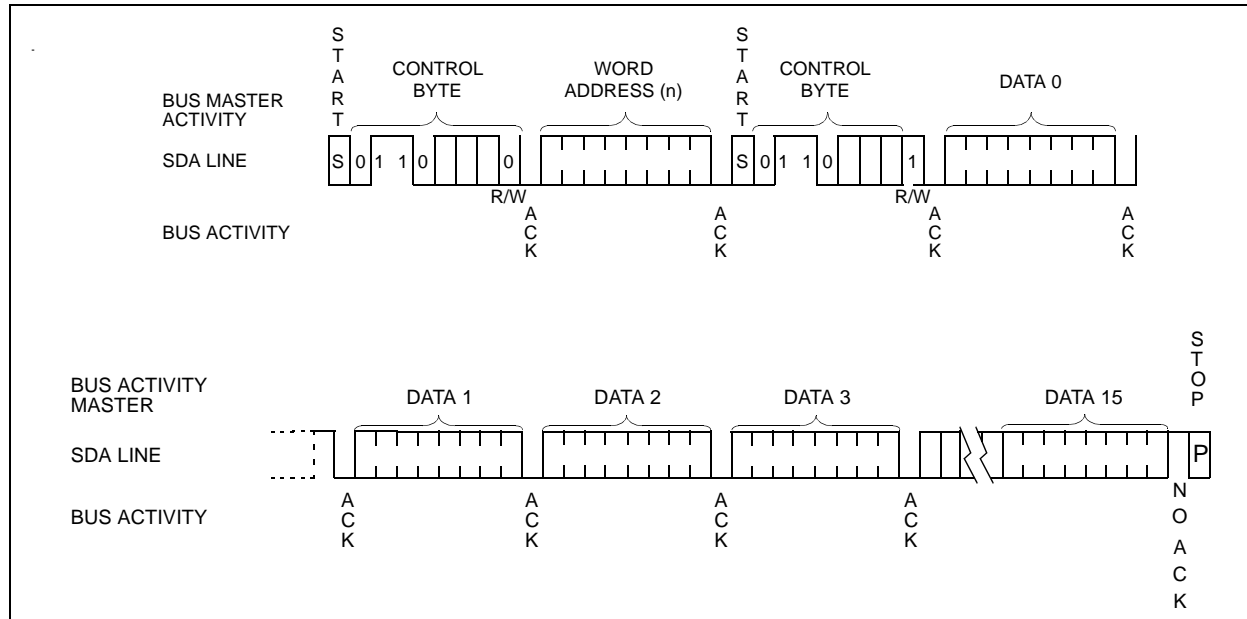
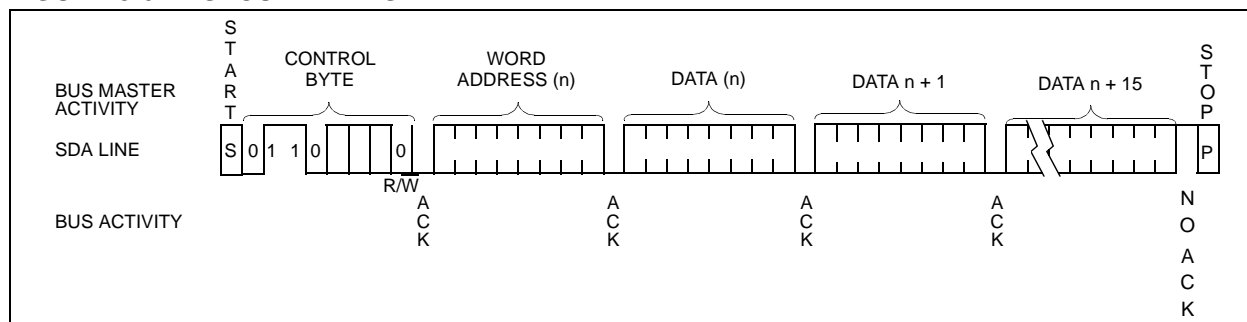


FIGURE 8-6: SECURITY PAGE WRITE



24LC174 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC174 -	/P		
		Package:	P = Plastic DIP (300 mil Body), 8-lead SN = Plastic SOIC (150 mil Body), 8-lead
		Temperature Range:	Blank = 0°C to +70°C I = -40°C to +85°C
		Device:	24LC174 16K I ² C Serial EEPROM 24LC174T 16K I ² C Serial EEPROM (Tape and Reel)

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

24LC174

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rfPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


AmpLab, FilterLab, MXDEV, MXLAB, PICMASTER, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, rfLAB, rfPICDEM, Select Mode, Smart Serial, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2004, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==**

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: www.microchip.com

Atlanta

3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034
Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848
Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

16200 Addison Road, Suite 255
Addison Plaza
Addison, TX 75001
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, IN 46902
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

25950 Acero St., Suite 200
Mission Viejo, CA 92691
Tel: 949-462-9523
Fax: 949-462-9608

San Jose

1300 Terra Bella Avenue
Mountain View, CA 94043
Tel: 650-215-1444
Fax: 650-961-0286

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Unit 32 41 Rawson Street
Epping 2121, NSW
Sydney, Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Unit 706B
Wan Tai Bei Hai Bldg.
No. 6 Chaoyangmen Bei Str.
Beijing, 100027, China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu

Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou

Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

China - Hong Kong SAR

Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai

Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700
Fax: 86-21-6275-5060

China - Shenzhen

Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380
Fax: 86-755-8295-1393

China - Shunde

Room 401, Hongjian Building, No. 2
Fengxiangnan Road, Ronggui Town, Shunde
District, Foshan City, Guangdong 528303, China
Tel: 86-757-28395507 Fax: 86-757-28395571

China - Qingdao

Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India

Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessey Road
Bangalore, 560 025, India
Tel: 91-80-22290061 Fax: 91-80-22290062

Japan

Yusen Shin Yokohama Building 10F
3-17-2, Shin Yokohama, Kohoku-ku,
Yokohama, Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or
82-2-558-5934

Singapore

200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Kaohsiung Branch
30F - 1 No. 8
Min Chuan 2nd Road
Kaohsiung 806, Taiwan
Tel: 886-7-536-4816
Fax: 886-7-536-4817

Taiwan

Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

Taiwan

Taiwan Branch
13F-3, No. 295, Sec. 2, Kung Fu Road
Hsinchu City 300, Taiwan
Tel: 886-3-572-9526
Fax: 886-3-572-6459

EUROPE

Austria

Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark

Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France

Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany

Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy

Via Salvatore Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands

Waegenburghtplein 4
NL-5152 JR, Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom

505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820

07/12/04