# 24AA024H/24LC024H

## 2K I²C™ Serial EEPROM with Half-Array Write Protect

### Device Selection Table

| Part Number | Vcc Range | Max. Clock | Temp. Range |
|---|---|---|---|
| 24AA024H | 1.7V-5.5V | 400 kHz(1) | I |
| 24LC024H | 2.5V-5.5V | 1 MHz | I, E |

**Note 1:** 100 kHz for VCC < 1.8V

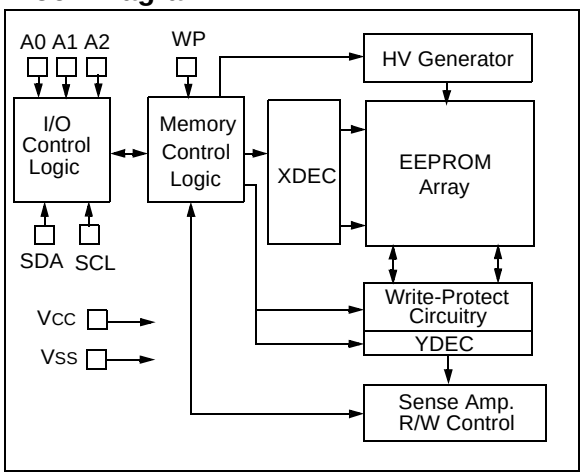
### Features:

- Single-Supply with Operation Down to 1.7V
- Low-Power CMOS Technology:
  - 400 μA active current, max.
  - 1 μA standby current, max.
- Organized as a Single Block of 256 Bytes (256 x 8)
- 2-Wire Serial Interface Bus, I²C™ Compatible
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Compatibility
- 1 MHz Compatibility (LC)
- Page Write Buffer for up to 16 Bytes
- Self-Timed Write Cycle (including Auto-Erase)
- Hardware Write Protection for Half Array (80h-FFh)
- Address Lines Allow up to Eight Devices on Bus
- 1 Million Erase/Write Cycles
- ESD Protection > 4,000V
- Data Retention > 200 Years
- Factory Programming (QTP) Available
- 8-pin PDIP, SOIC, TSSOP, TDFN and MSOP Packages
- Available for Extended Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C
- Pb-Free and RoHS compliant

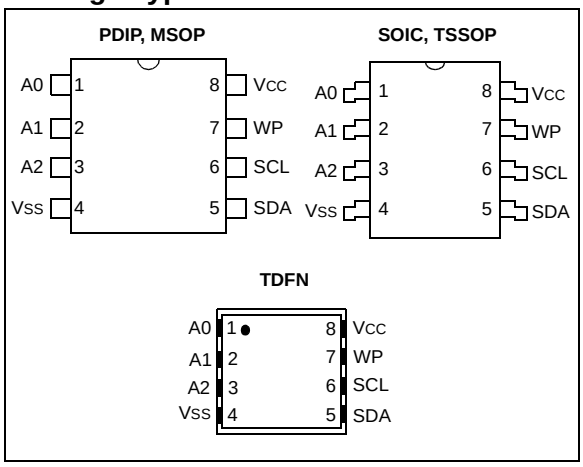
### Description:

The Microchip Technology Inc. 24AA024H/24LC024H is a 2 Kbit Serial Electrically Erasable PROM with operation down to 1.7V. The device is organized as a single block of 256 x 8-bit memory with a 2-wire serial interface. Low-current design permits operation with maximum standby and active currents of only 1 μA and 400 μA, respectively. The device has a page write capability for up to 16 bytes of data. Functional address lines allow the connection of up to eight 24AA024H/24LC024H devices on the same bus for up to 16 Kbits of contiguous EEPROM memory. The device is available in the standard 8-pin PDIP, 8-pin SOIC (150 mil), TSSOP, 2x3 TDFN and MSOP packages.

### Block Diagram




### Package Types



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

| **DC CHARACTERISTICS** | | | **Electrical Characteristics:**<br>Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C<br>Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to +125°C | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Max.** | **Units** | **Conditions** |
| D1 | — | A0, A1, A2, SCL, SDA and WP pins: | — | — | — | — |
| D2 | VIH | High-level input voltage | 0.7 VCC | — | V | — |
| D3 | VIL | Low-level input voltage | — | 0.3 VCC | V | — |
| D4 | VHYS | Hysteresis of Schmitt Trigger inputs (SDA, SCL pins) | 0.05 VCC | — | V | **(Note)** |
| D5 | VOL | Low-level output voltage | — | 0.40 | V | IOL = 3.0 ma @ VCC = 4.5V<br>IOL = 2.1 ma @ VCC = 2.5V |
| D6 | ILI | Input leakage current | — | ±1 | µA | VIN = VSS or VCC, WP = VSS |
| D7 | ILO | Output leakage current | — | ±1 | µA | VOUT = VSS or VCC |
| D8 | CIN, COUT | Pin capacitance (all inputs/outputs) | — | 10 | pF | VCC = 5.0V **(Note)**<br>TA = 25°C, f = 1 MHz |
| D9 | ICC Read | Operating current | — | 400 | µA | VCC = 5.5V, SCL = 400 kHz |
| | ICC Write | | — | 3 | mA | VCC = 5.5V |
| D10 | ICCS | Standby current | — | 1 | µA | VCC = 5.5V, SCL = SDA = VCC<br>WP = VSS, A0, A1, A2 = VSS |

**Note:** This parameter is periodically sampled and not 100% tested.

## TABLE 1-2: AC CHARACTERISTICS

| AC CHARACTERISTICS | | | Electrical Characteristics: Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C; Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to +125°C | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min.** | **Max.** | **Units** | **Conditions** |
| 1 | FCLK | Clock frequency | —<br>—<br>— | 100<br>400<br>1000 | kHz | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 2 | THIGH | Clock high time | 4000<br>600<br>500 | —<br>—<br>— | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 3 | TLOW | Clock low time | 4700<br>1300<br>500 | —<br>—<br>— | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 4 | TR | SDA and SCL rise time **(Note 1)** | —<br>—<br>— | 1000<br>300<br>300 | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 5 | TF | SDA and SCL fall time **(Note 1)** | —<br>—<br>— | 1000<br>300<br>300 | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 6 | THD:STA | Start condition hold time | 4000<br>600<br>250 | —<br>—<br>— | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 7 | TSU:STA | Start condition setup time | 4700<br>600<br>250 | —<br>—<br>— | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 8 | THD:DAT | Data input hold time | 0 | — | ns | **(Note 2)** |
| 9 | TSU:DAT | Data input setup time | 250<br>100<br>100 | —<br>—<br>— | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 10 | TSU:STO | Stop condition setup time | 4000<br>600<br>250 | —<br>—<br>— | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 11 | TSU:WP | WP setup time | 4000<br>600<br>600 | —<br>—<br>— | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 12 | THD:WP | WP hold time | 4700<br>600<br>600 | —<br>—<br>— | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 13 | TAA | Output valid from clock **(Note 2)** | —<br>—<br>— | 3500<br>900<br>400 | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 14 | TBUF | Bus free time: Time the bus must be free before a new transmission can start | 1300<br>4700<br>4700 | —<br>—<br>— | ns | 1.7V ≤ VCC < 1.8V<br>1.8V ≤ VCC ≤ 5.5V<br>2.5V ≤ VCC ≤ 5.5V (24LC024H) |
| 16 | TSP | Input filter spike suppression (SDA and SCL pins) | — | 50 | ns | 24AA024H<br>**(Note 1 and Note 3)** |
| 17 | TWC | Write cycle time (byte or page) | — | 5 | ms | — |
| 18 | — | Endurance | 1M | — | cycles | 25°C, VCC = 5.5V, Block mode<br>**(Note 4)** |

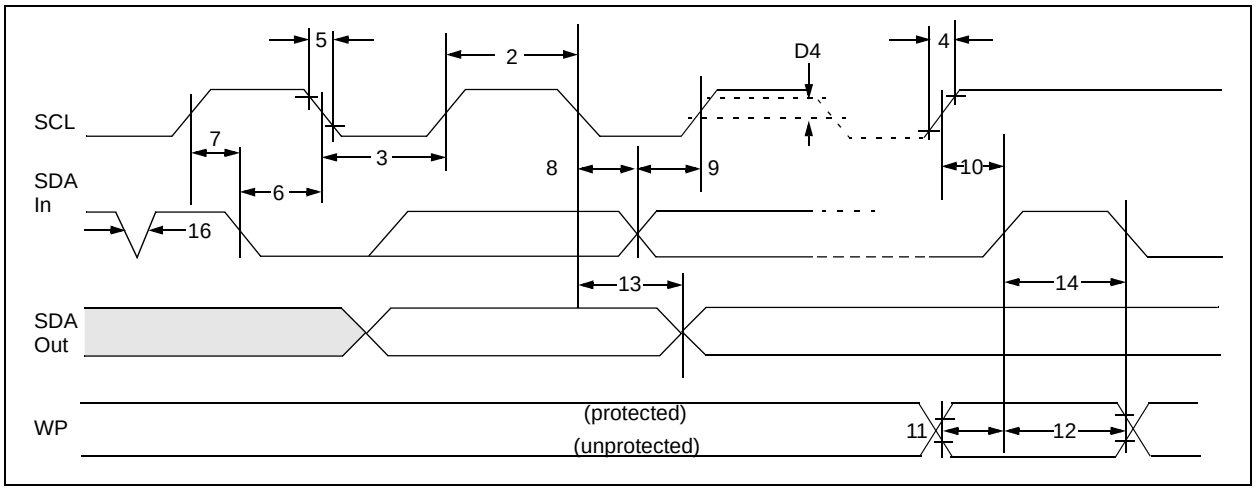
**Note 1:** Not 100% tested. CB = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

**4:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

**FIGURE 1-1: BUS TIMING DATA**



## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Name | 8-pin PDIP | 8-pin SOIC | 8-pin TSSOP | 8-pin MSOP | 8-pin TDFN | Function |
|---|---|---|---|---|---|---|
| A0 | 1 | 1 | 1 | 1 | 1 | User Configurable Chip Select |
| A1 | 2 | 2 | 2 | 2 | 2 | User Configurable Chip Select |
| A2 | 3 | 3 | 3 | 3 | 3 | User Configurable Chip Select |
| VSS | 4 | 4 | 4 | 4 | 4 | Ground |
| SDA | 5 | 5 | 5 | 5 | 5 | Serial Data |
| SCL | 6 | 6 | 6 | 6 | 6 | Serial Clock |
| WP | 7 | 7 | 7 | 7 | 7 | Write-Protect Input |
| VCC | 8 | 8 | 8 | 8 | 8 | +1.7V to 5.5V (24AA024H)<br>+2.5V to 5.5V (24LC024H) |

### 2.1 SDA Serial Data

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

### 2.2 SCL Serial Clock

The SCL input is used to synchronize the data transfer to and from the device.

### 2.3 A0, A1, A2

The A0, A1 and A2 inputs are used by the 24AA024H/24LC024H for multiple device operations. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24AA024H/24LC024H devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VCC or VSS.

In most applications, the chip address inputs A0, A1 and A2 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

### 2.4 WP

WP is the hardware write-protect pin. It must be tied to VCC or VSS. If tied to VCC, the hardware write protection is enabled and will protect half of the array (80h-FFh). If the WP pin is tied to VSS the hardware write protection is disabled.

### 2.5 Noise Protection

The 24AA024H/24LC024H employs a VCC threshold detector circuit that disables the internal erase/write logic if the VCC is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits that suppress noise spikes to assure proper device operation even on a noisy bus.

## 3.0 FUNCTIONAL DESCRIPTION

The 24AA024H/24LC024H supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device that generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions while the 24AA024H/24LC024H works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

## 4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

### 4.1 Bus Not Busy (A)

Both data and clock lines remain high.

### 4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

### 4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

### 4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is, theoretically, unlimited, though only the last sixteen will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first-in first-out fashion.

### 4.5 Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

| **Note:** | The 24AA024H/24LC024H does not generate any Acknowledge bits if an internal programming cycle is in progress. |
|---|---|

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition (Figure 4-2).

**FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS**

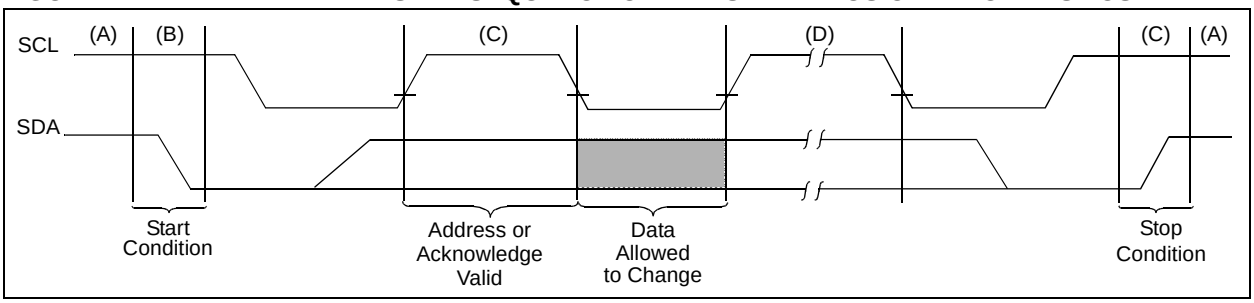
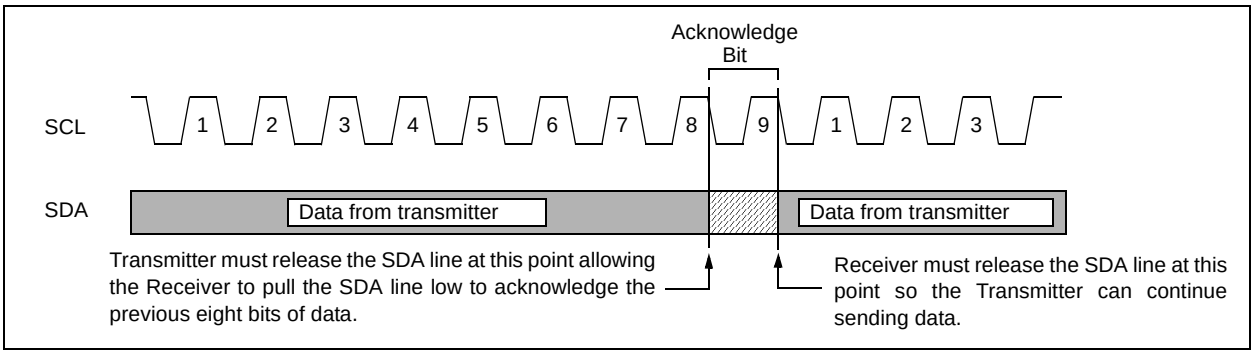



**FIGURE 4-2: ACKNOWLEDGE TIMING**

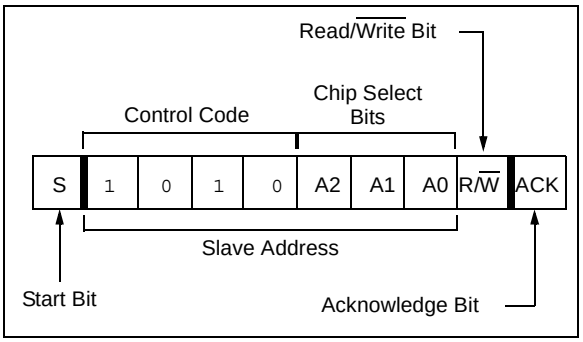


## 5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the master device (Figure 5-1). The control byte consists of a four-bit control code; for the 24AA024H/24LC024H this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24AA024H/24LC024H devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a '1', a read operation is selected. When set to a '0', a write operation is selected. Following the Start condition, the 24AA024H/24LC024H monitors the SDA bus, checking the control byte being transmitted. Upon receiving a '1010' code and appropriate Chip Select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24AA024H/24LC024H will select a read or write operation.

**FIGURE 5-1: CONTROL BYTE FORMAT**




### 5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 16K bits by adding up to eight 24AA024H/24LC024H devices on the same bus. In this case, software can use A0 of the control byte as address bit A9, A1 as address bit A10, and A2 as address bit A11. It is not possible to sequentially read across device boundaries.

## 6.0 WRITE OPERATIONS

### 6.1 Byte Write

Following the Start signal from the master, the device code (4 bits), the Chip Select bits (3 bits) and the R/$\overline{W}$ bit (which is a logic low) are placed onto the bus by the master transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the master is the word address and will be written into the Address Pointer of the 24AA024H/24LC024H. After receiving another Acknowledge signal from the 24AA024H/24LC024H, the master device will transmit the data word to be written into the addressed memory location. The 24AA024H/24LC024H acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and the 24AA024H/24LC024H will not generate Acknowledge signals during this time (Figure 6-1). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if write protection is enabled.

### 6.2 Page Write

The write-control byte, word address and the first data byte are transmitted to the 24AA024H/24LC024H in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to 15 additional data bytes to the 24AA024H/24LC024H that are temporarily stored in the on-chip page buffer and will be written into the memory once the master has transmitted a Stop condition. Upon receipt of each word, the four lower order Address Pointer bits are internally incremented by one.

The higher order four bits of the word address remain constant. If the master should transmit more than 16 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if write protection is enabled.

| | |
|---|---|
| **Note:** | Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary that the application software prevent page write operations that would attempt to cross a page boundary. |

### 6.3 Write Protection

The WP pin must be tied to VCC or VSS. If tied to VCC, half of the array will be write-protected (80h-FFh). If the WP pin is tied to VSS, write operations to all address locations are allowed.

**FIGURE 6-1: BYTE WRITE**

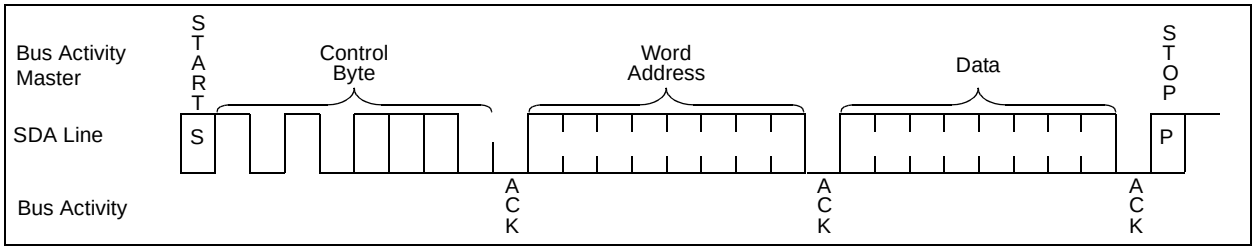
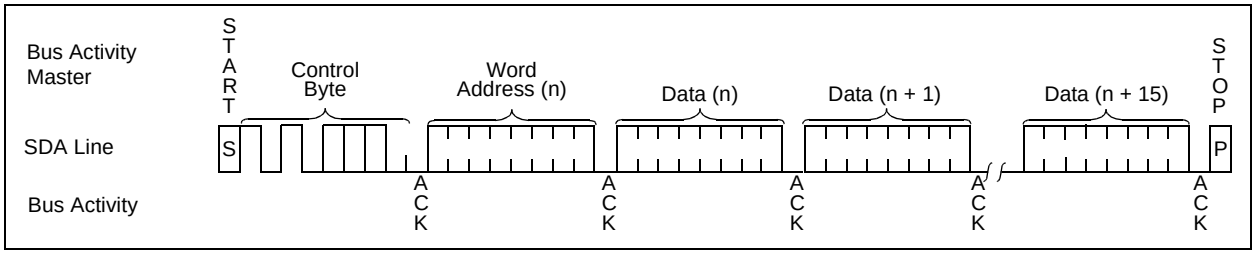


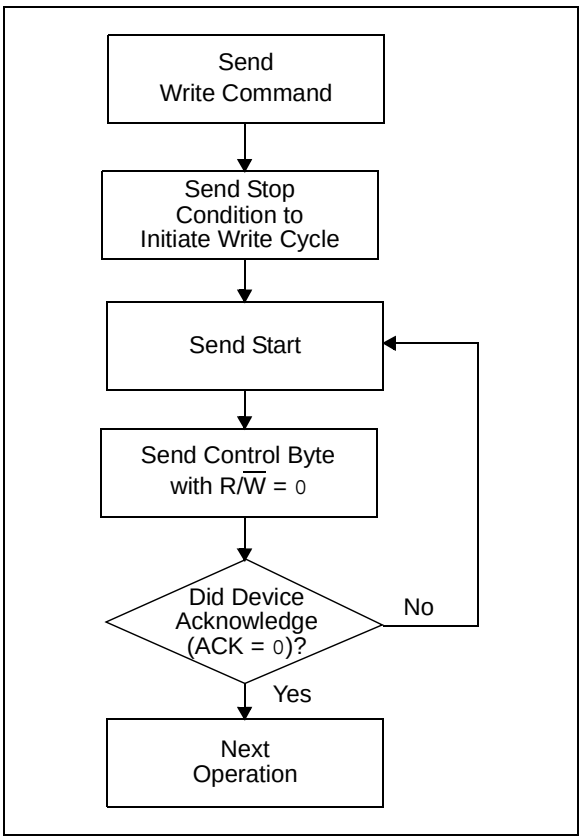

**FIGURE 6-2: PAGE WRITE**



## 7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the master, the device initiates the internally-timed write cycle and ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for a flow diagram of this operation.

**FIGURE 7-1: ACKNOWLEDGE POLLING FLOW**



## 8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

### 8.1 Current Address Read

The 24AA024H/24LC024H contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to '1', the 24AA024H/24LC024H issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24AA024H/24LC024H discontinues transmission (Figure 8-1).

### 8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 24AA024H/24LC024H as part of a write operation.

Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The master then issues the control byte again but with the R/$\overline{W}$ bit set to a '1'. The 24AA024H/24LC024H will then issue an acknowledge and transmits the eight-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24AA024H/24LC024H discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

### 8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA024H/24LC024H transmits the first data byte, the master issues an acknowledge as opposed to a Stop condition in a random read. This directs the 24AA024H/24LC024H to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads, the 24AA024H/24LC024H contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address FFh to address 00h.

**FIGURE 8-1: CURRENT ADDRESS READ**

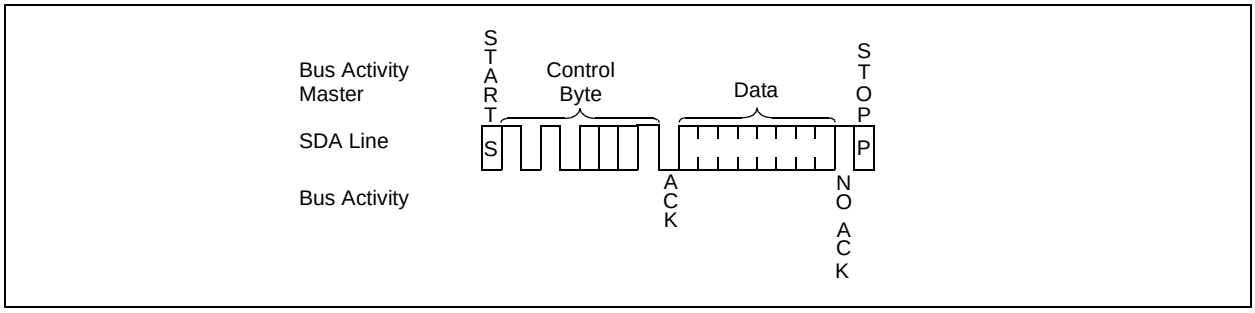


**FIGURE 8-2: RANDOM READ**

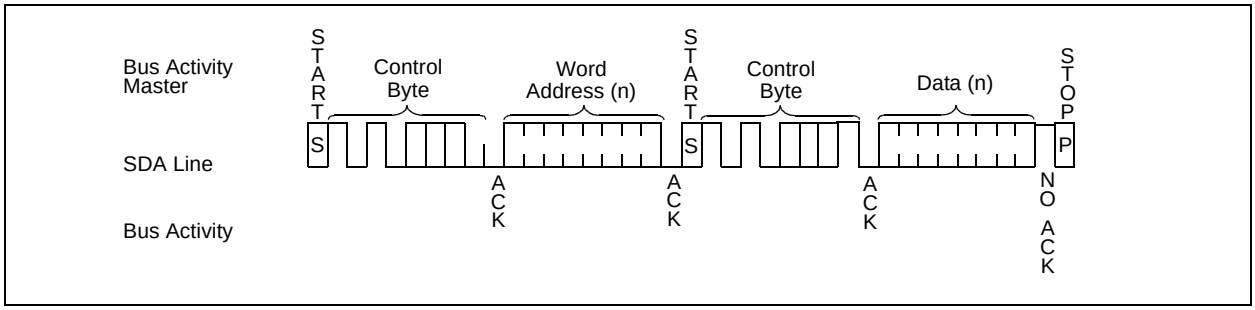
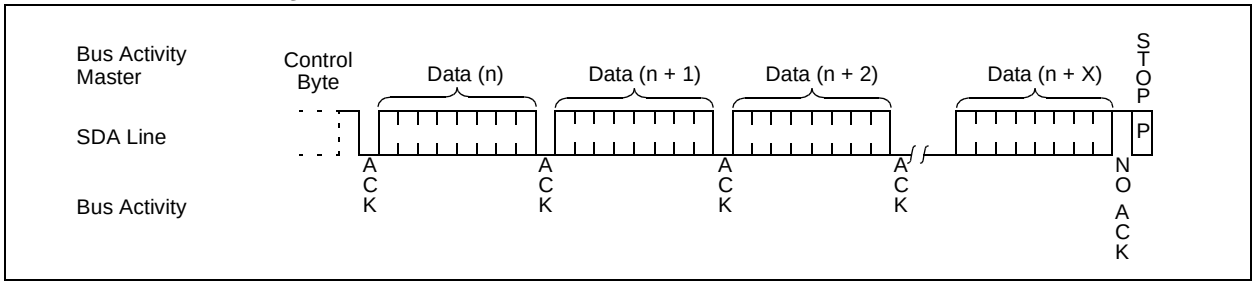


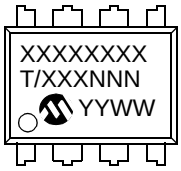

**FIGURE 8-3: SEQUENTIAL READ**



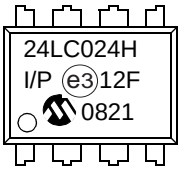
## 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information

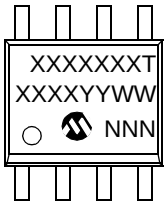
8-Lead PDIP (300 mil)



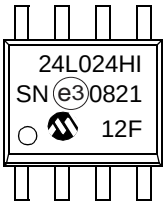

Example:



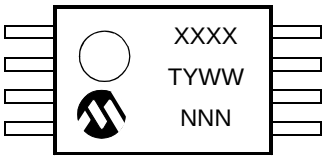

8-Lead SOIC (3.90 mm)



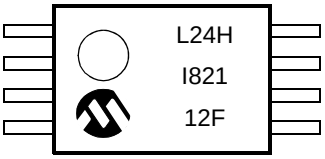

Example:



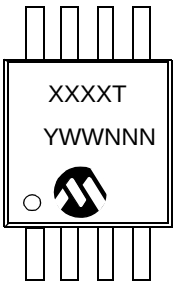

8-Lead TSSOP



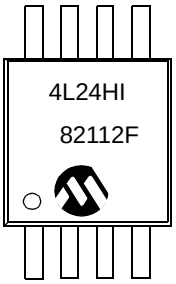

Example:




8-Lead MSOP

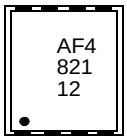



Example:




8-Lead 2x3 TDFN


Example:



| Part Number | 1st Line Marking Codes | | | | | |
|---|---|---|---|---|---|---|
| | TSSOP | | MSOP | | TDFN | |
| | I | E | I | E | I | E |
| 24AA024H | A24H | A24H | 4A24HI | 4A24HE | AF1 | AF2 |
| 24LC024H | L24H | L24H | 4L24HI | 4L24HE | AF4 | AF5 |

| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |

**Note**: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

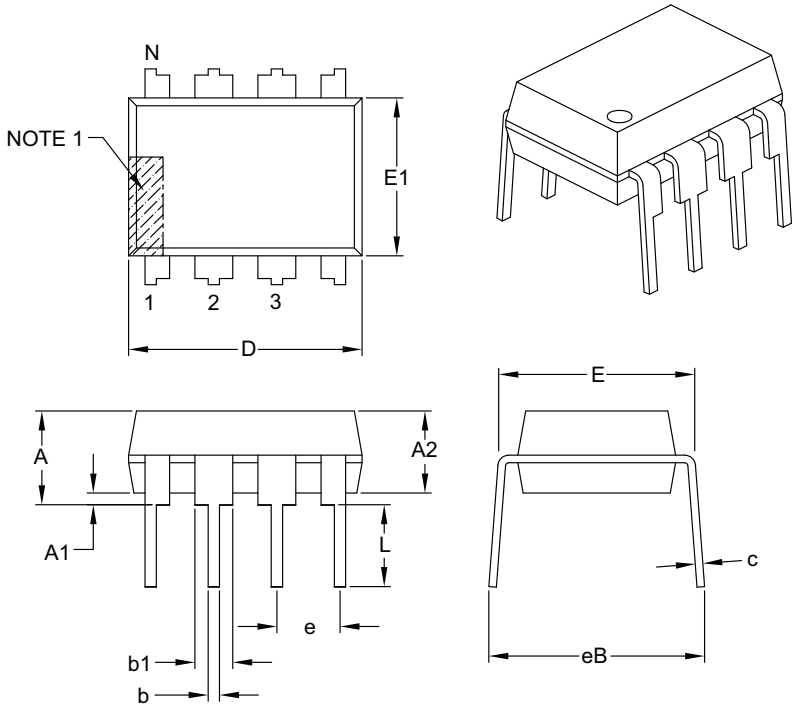
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

**Note:** Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

***Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

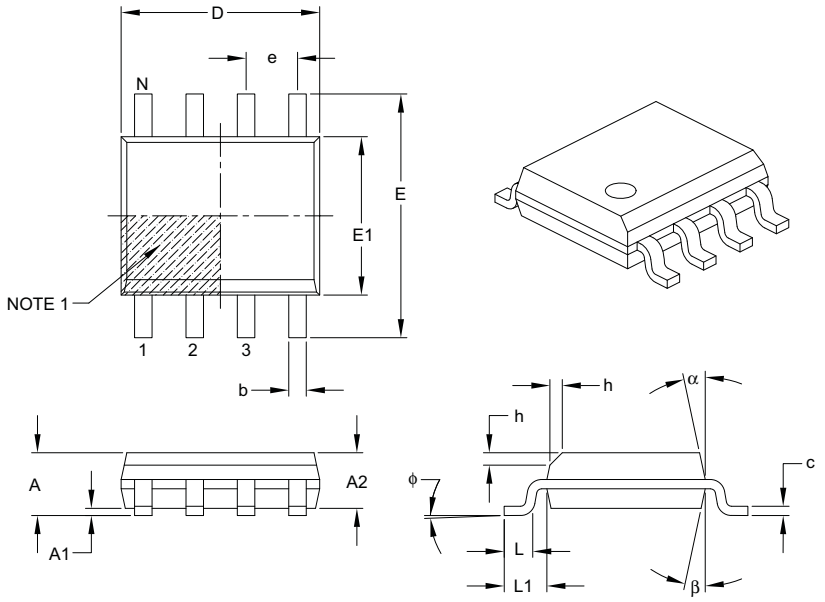
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | φ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

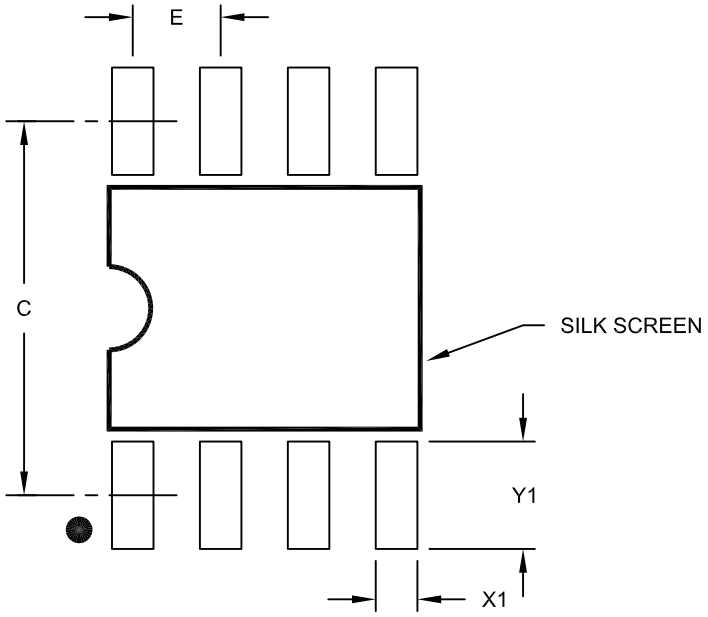
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

### 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

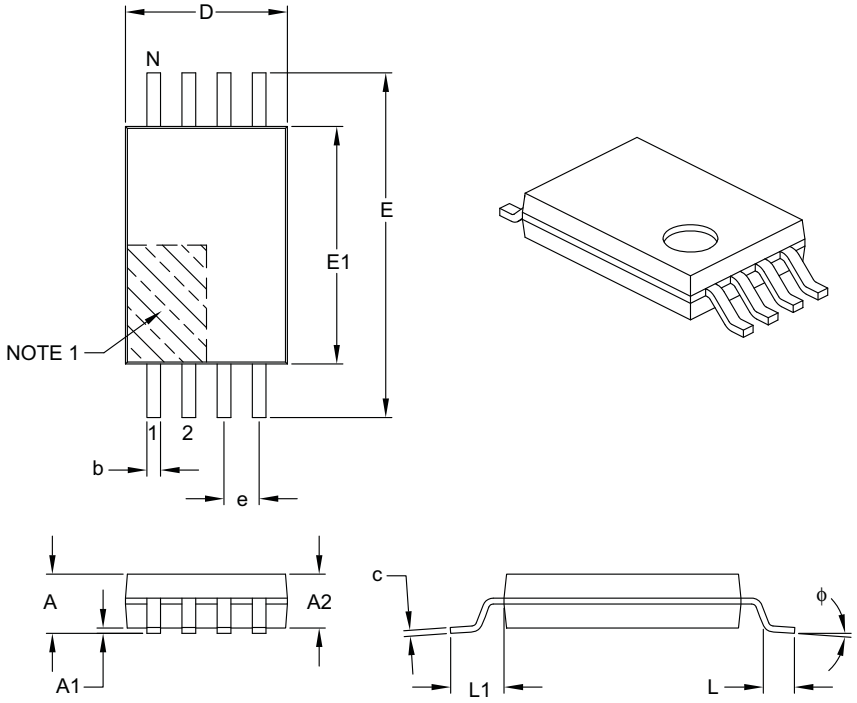
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

## 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | 2.90 | 3.00 | 3.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.19 | – | 0.30 |

**Notes:**

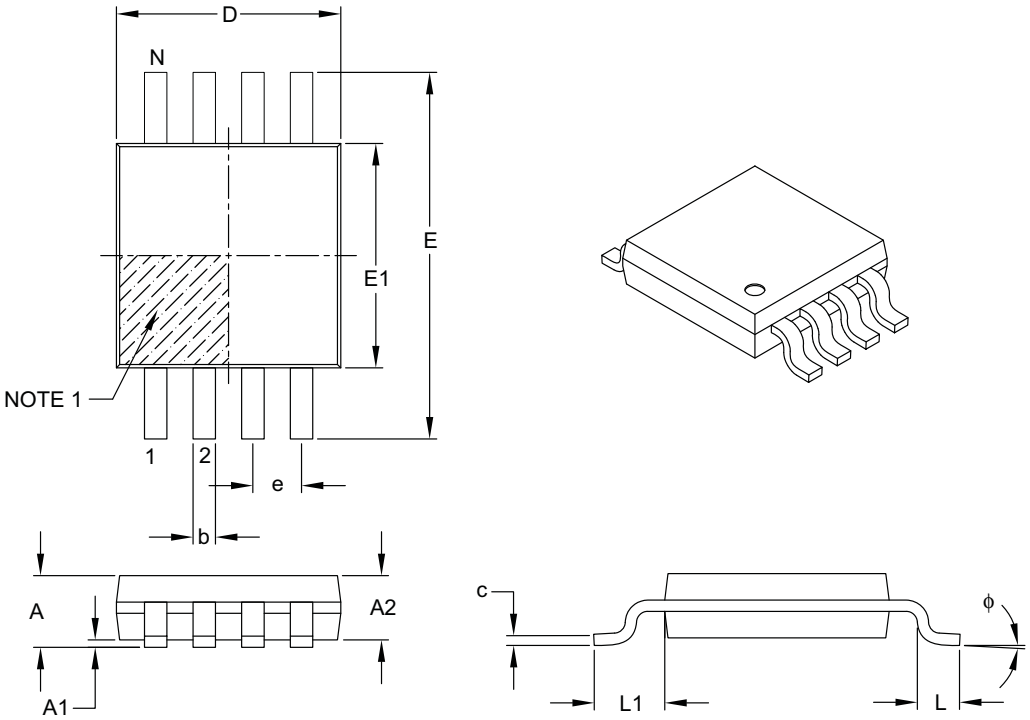
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Overall Length | D | | 3.00 BSC | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.08 | – | 0.23 |
| Lead Width | b | 0.22 | – | 0.40 |

**Notes:**

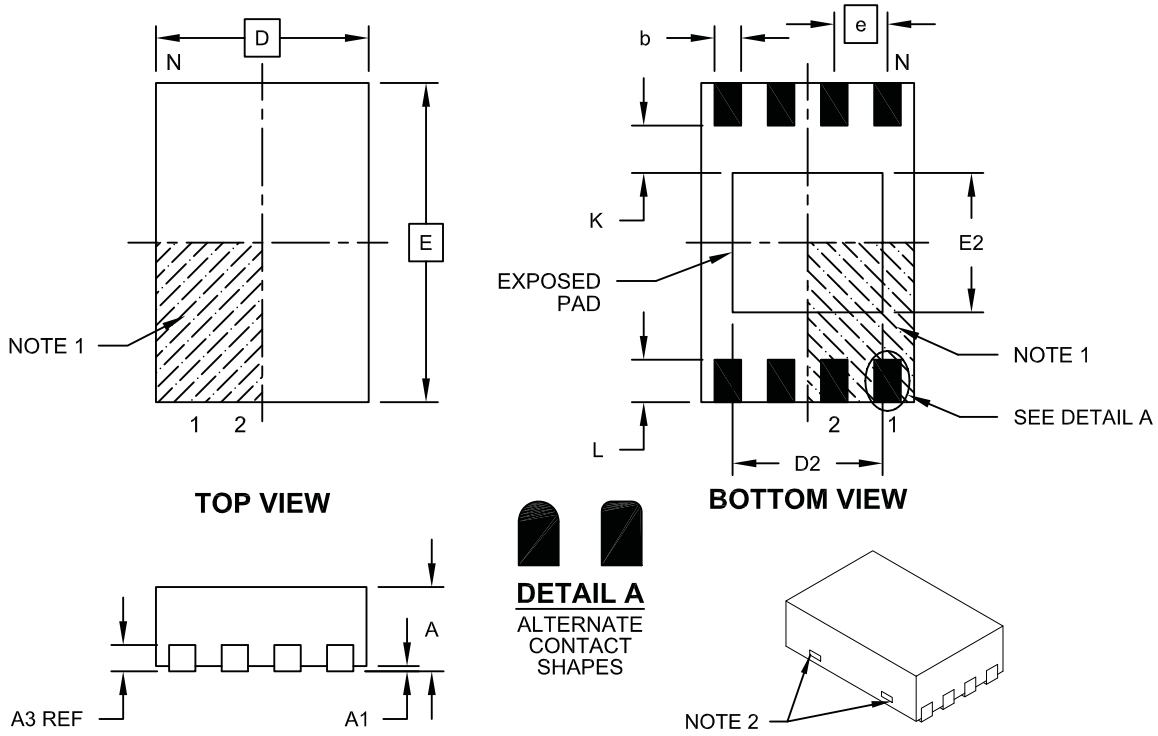
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

## 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.70 | 0.75 | 0.80 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.20 | - | 1.60 |
| Exposed Pad Width | E2 | 1.20 | - | 1.60 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.30 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

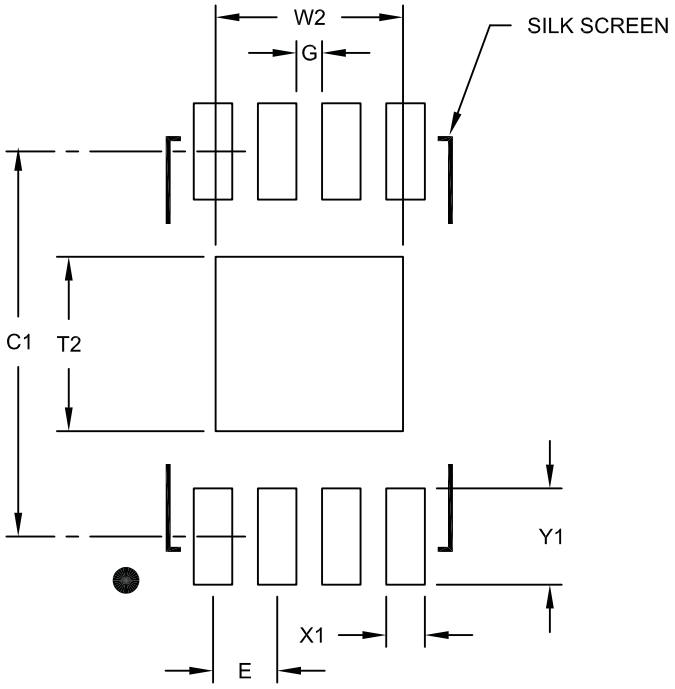
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129B

### 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 1.46 |
| Optional Center Pad Length | T2 | | | 1.36 |
| Contact Pad Spacing | C1 | | 3.00 | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

## REVISION HISTORY

### Revision A (08/2008)

Original release.

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4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX |
|---|---|---|
| Device | Temperature Range | Package |

| | | | |
|---|---|---|---|
| **Device:** | 24AA024H: | | 1.7V, 2 Kbit Addressable Serial EEPROM |
| | 24AA024HT: | | 1.7V, 2 Kbit Addressable Serial EEPROM (Tape and Reel) |
| | 24LC024H: | | 2.5V, 2 Kbit Addressable Serial EEPROM |
| | 24LC024HT: | | 2.5V, 2 Kbit Addressable Serial EEPROM (Tape and Reel) |
| **Temperature Range:** | I | = | -40°C to +85°C |
| | E | = | -40°C to +125°C |
| **Package:** | P | = | Plastic DIP, (300 mil Body), 8-lead |
| | SN | = | Plastic SOIC, (3.90 mm Body) |
| | ST | = | TSSOP, (4.4 mm Body), 8-lead |
| | MS | = | MSOP, (Plastic Micro Small Outline), 8-lead |
| | MNY(1) | = | TDFN, (2x3x0.75 mm Body), 8-lead |

**Note 1:** "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.

**Examples:**

a) 24AA024H-I/P: Industrial Temperature, 1.7V, PDIP package.

b) 24AA024H-I/SN: Industrial Temperature, 1.7V, SOIC Package.

c) 24AA024HT-I/ST: Industrial Temperature, 1.7V, TSSOP Package, Tape and Reel

a) 24LC024H-I/P: Industrial Temperature, 2.5V, PDIP Package.

b) 24LC024HT-E/SN: Automotive Temperature, 2.5V, SOIC Package, Tape and Reel

c) 24LC024HT-I/MS: Industrial Temperature, 2.5V, MSOP Package, Tape and Reel.

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