NLSX3373

2-Bit 20 Mb/s Dual-Supply Level Translator

The NLSX3373 is a 2−bit configurable dual−supply bidirectional auto sensing translator that does not require a directional control pin. The V_{CC} I/O and V_L I/O ports are designed to track two different power supply rails, V_{CC} and V_L respectively. The V_{CC} supply rail is configurable from 1.65 V to 5.5 V while V_L supply rail is configurable to 1.2 V to 5.5 V. This allows lower voltage logic signals on the V_L side to be translated into higher voltage logic signals on the V_{CC} side, and vice−versa.

The NLSX3373 translator has open−drain outputs with integrated 10 kΩ pullup resistors on the I/O lines. The integrated pullup resistors are used to pullup the I/O lines to either V_L or V_{CC}. The NLSX3373 is an excellent match for open−drain applications such as the I^2C communication bus.

Features

- Wide High−Side V_{CC} Operating Range: 1.65 V to 5.5 V
  Wide Low−Side V_L Operating Range: 1.2 V to 5.5 V
- High−Speed with 16 Mb/s Guaranteed Date Rate for $V_L > 2.5$ V
- Low Bit−to−Bit Skew
- Enable Input and I/O Lines have Overvoltage Tolerant (OVT) to 5.5 V
- Nonpreferential Powerup Sequencing
- Integrated 10 kΩ Pullup Resistors
- Small Space Saving Package − 1.8 x 1.2 x 0.5 mm UDFN8
- This is a Pb−Free Device

Typical Applications

- I^2C, SMBus, PMBus
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

Important Information

- ESD Protection for Power, Enable and I/O Pins:
  Human Body Model (HBM): ± 7.5 kV
  Machine Model (MM): 400 V

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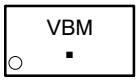
http://onsemi.com

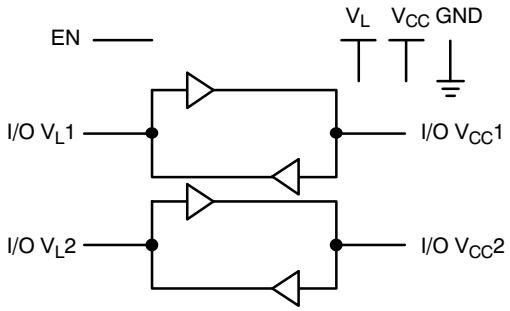
MARKING DIAGRAM

UDFN8
MU SUFFIX
CASE 517AJ

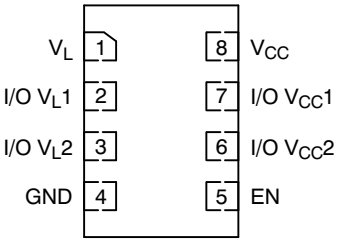


VB = Specific Device Code
M = Date Code
▪ = Pb−Free Package

LOGIC DIAGRAM



PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NLSX3373MUTAG	UDFN8 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

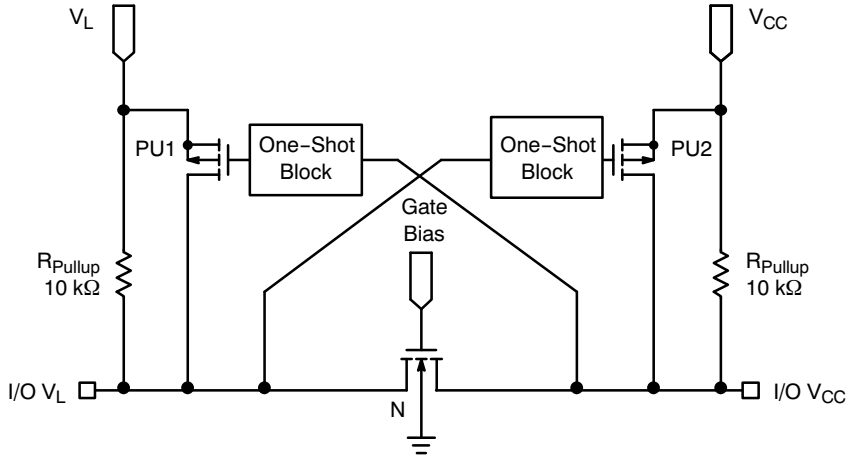


Figure 1. Block Diagram (1 I/O Line)

PIN ASSIGNMENT

Pins	Description
V_{CC}	V_{CC} Input Voltage
V_L	V_L Input Voltage
GND	Ground
EN	Output Enable
I/O V_{CC}n	V_{CC} I/O Port, Referenced to V_{CC}
I/O V_Ln	V_L I/O Port, Referenced to V_L

FUNCTION TABLE

EN	Operating Mode
L	Hi−Z
H	I/O Buses Connected

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	High−side DC Supply Voltage	−0.3 to +7.0		V
V_L	High−side DC Supply Voltage	−0.3 to +7.0		V
I/O V_{CC}	V_{CC}−Referenced DC Input/Output Voltage	−0.3 to (V_{CC} + 0.3)		V
I/O V_L	V_L−Referenced DC Input/Output Voltage	−0.3 to (V_L + 0.3)		V
V_{EN}	Enable Control Pin DC Input Voltage	−0.3 to +7.0		V
I_{I/O_SC}	Short−Circuit Duration (I/O V_L and I/O V_{CC} to GND)	40	Continuous	mA
T_{STG}	Storage Temperature	−65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	High−side Positive DC Supply Voltage	1.65	5.5	V
V_L	High−side Positive DC Supply Voltage	1.2	5.5	V
V_{EN}	Enable Control Pin Voltage	GND	5.5	V
V_{IO}	Enable Control Pin Voltage	GND	5.5	V
T_A	Operating Temperature Range	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 1.65 V to 5.5 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	−40°C to +85°C			Unit
			Min	Typ (Notes 1, 2)	Max	
V_{IHC}	I/O V_{CC} Input HIGH Voltage		2/3 * V_{CC}	–	–	V
V_{ILC}	I/O V_{CC} Input LOW Voltage		–	–	1/3 * V_{CC}	V
V_{IHL}	I/O V_L Input HIGH Voltage		2/3 * V_L	–	–	V
V_{ILL}	I/O V_L Input LOW Voltage		–	–	1/3 * V_L	V
V_{IH}	Control Pin Input HIGH Voltage	T_A = +25°C	2/3 * V_L	–	–	V
V_{IL}	Control Pin Input LOW Voltage	T_A = +25°C	–	–	1/3 * V_L	V
V_{OHC}	I/O V_{CC} Output HIGH Voltage	I/O V_{CC} Source Current = 20 μA	2/3 * V_{CC}	–	–	V
V_{OLC}	I/O V_{CC} Output LOW Voltage	I/O V_{CC} Sink Current = 20 μA	–	–	1/3 * V_{CC}	V
V_{OHL}	I/O V_L Output HIGH Voltage	I/O V_L Source Current = 20 μA	2/3 * V_L	–	–	V
V_{OLL}	I/O V_L Output LOW Voltage	I/O V_L Sink Current = 20 μA	–	–	1/3 * V_L	V
I_{QVCC}	V_{CC} Supply Current	I/O V_{CC} and I/O V_L Unconnected, V_{EN} = V_L, T_A = +25°C	–		10	μA
I_{QVL}	V_L Supply Current	I/O V_{CC} and I/O V_L Unconnected, V_{EN} = V_L, T_A = +25°C	–		5	μA
I_{TS-VCC}	V_{CC} Tristate Output Mode Supply Current	I/O V_{CC} and I/O V_L Unconnected, V_{EN} = GND, T_A = +25°C	–		1	μA
I_{TS-VL}	V_L Tristate Output Mode Supply Current	I/O V_{CC} and I/O V_L Unconnected, V_{EN} = GND, T_A = +25°C	–		1	μA
I_{OZ}	I/O Tristate Output Mode Leakage Current	T_A = +25°C	–		1	μA
R_{PU}	Pullup Resistor I/O V_L and V_{CC}	T_A = +25°C		10		kΩ

1. Typical values are for V_{CC} = +3.3 V, V_L = +1.8 V and T_A = +25°C.
2. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS – RAIL–TO–RAIL DRIVING CONFIGURATIONS

(I/O test circuit of Figures 2 and 3, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	–40°C to +85°C (Notes 3 and 4)			Unit
			Min	Typ	Max	
+1.2 ≤ V_L ≤ V_{CC} ≤ +5.5 V						
t_{RVCC}	I/O V_{CC} Risetime				25	ns
t_{FVCC}	I/O V_{CC} Falltime				37	ns
t_{RVL}	I/O V_L Risetime				30	ns
t_{FVL}	I/O V_L Falltime				30	ns
$t_{PDVL–VCC}$	Propagation Delay (Driving I/O V_L)				30	ns
$t_{PDVCC–VL}$	Propagation Delay (Driving I/O V_{CC})				30	ns
t_{PPSKEW}	Part–to–Part Skew				20	nS
	Maximum Data Rate		8			Mb/s
+1.2 ≤ V_L ≤ V_{CC} ≤ +3.3 V						
t_{RVCC}	I/O V_{CC} Risetime				25	ns
t_{FVCC}	I/O V_{CC} Falltime				30	ns
t_{RVL}	I/O V_L Risetime				30	ns
t_{FVL}	I/O V_L Falltime				30	ns
$t_{PDVL–VCC}$	Propagation Delay (Driving I/O V_L)				20	ns
$t_{PDVCC–VL}$	Propagation Delay (Driving I/O V_{CC})				20	ns
t_{PPSKEW}	Part–to–Part Skew				10	nS
	Maximum Data Rate		10			Mb/s
+1.8 ≤ V_L ≤ V_{CC} ≤ +2.5 V						
t_{RVCC}	I/O V_{CC} Risetime				15	ns
t_{FVCC}	I/O V_{CC} Falltime				15	ns
t_{RVL}	I/O V_L Risetime				15	ns
t_{FVL}	I/O V_L Falltime				15	ns
$t_{PDVL–VCC}$	Propagation Delay (Driving I/O V_L)				15	ns
$t_{PDVCC–VL}$	Propagation Delay (Driving I/O V_{CC})				15	ns
t_{PPSKEW}	Part–to–Part Skew				10	nS
	Maximum Data Rate		16			Mb/s
+2.5 ≤ V_L ≤ V_{CC} ≤ +3.3 V						
t_{RVCC}	I/O V_{CC} Risetime				15	ns
t_{FVCC}	I/O V_{CC} Falltime				15	ns
t_{RVL}	I/O V_L Risetime				15	ns
t_{FVL}	I/O V_L Falltime				15	ns
$t_{PDVL–VCC}$	Propagation Delay (Driving I/O V_L)				15	ns
$t_{PDVCC–VL}$	Propagation Delay (Driving I/O V_{CC})				15	ns
t_{PPSKEW}	Part–to–Part Skew				10	nS
	Maximum Data Rate		16			Mb/s

3. Typical values are for V_{CC} = +3.3 V, V_L = +1.8 V and T_A = +25°C.
4. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS – OPEN DRAIN DRIVING CONFIGURATIONS

(I/O test circuit of Figures 4 and 5, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (Notes 5 and 6)			Unit
			Min	Typ	Max	
+1.2 ≤ V_L ≤ V_{CC} ≤ +5.5 V						
t_{RVCC}	I/O V_{CC} Risetime				400	ns
t_{FVCC}	I/O V_{CC} Falltime				50	ns
t_{RVL}	I/O V_L Risetime				400	ns
t_{FVL}	I/O V_L Falltime				60	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)				1000	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})				1000	ns
t_{PPSKEW}	Part−to−Part Skew				50	nS
MDR	Maximum Data Rate		2			Mb/s

5. Typical values are for V_{CC} = +3.3 V, V_L = +1.8 V and T_A = +25°C.
6. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design. Limits over the operating temperature range are guaranteed by design.

TEST SETUPS

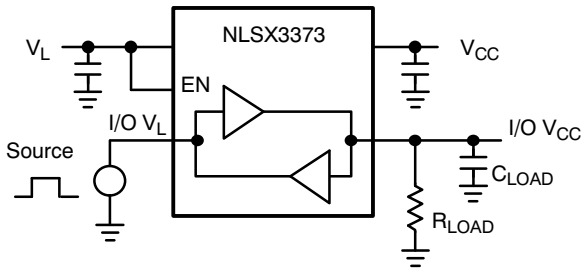


Figure 2. Rail−to−Rail Driving I/O V_L

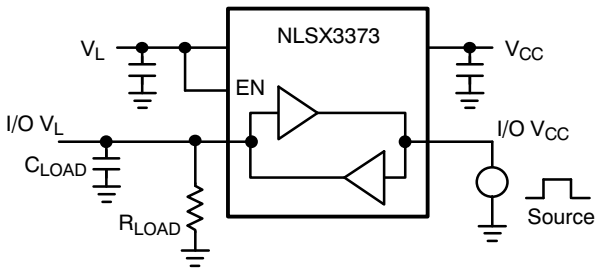


Figure 3. Rail−to−Rail Driving I/O V_{CC}

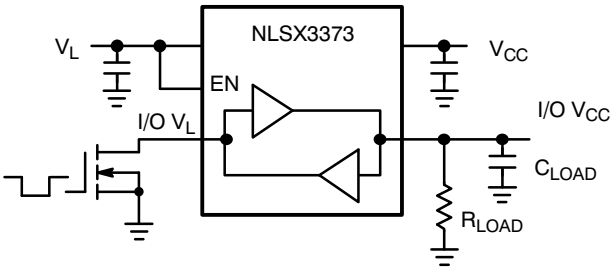


Figure 4. Open−Drain Driving I/O V_L

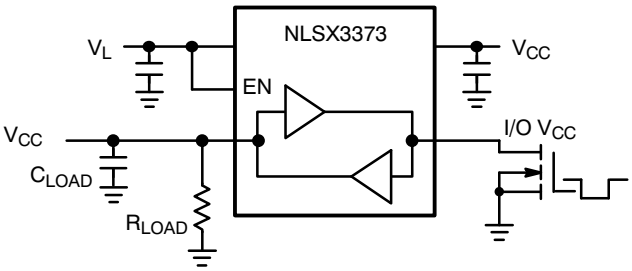


Figure 5. Open−Drain Driving I/O V_{CC}

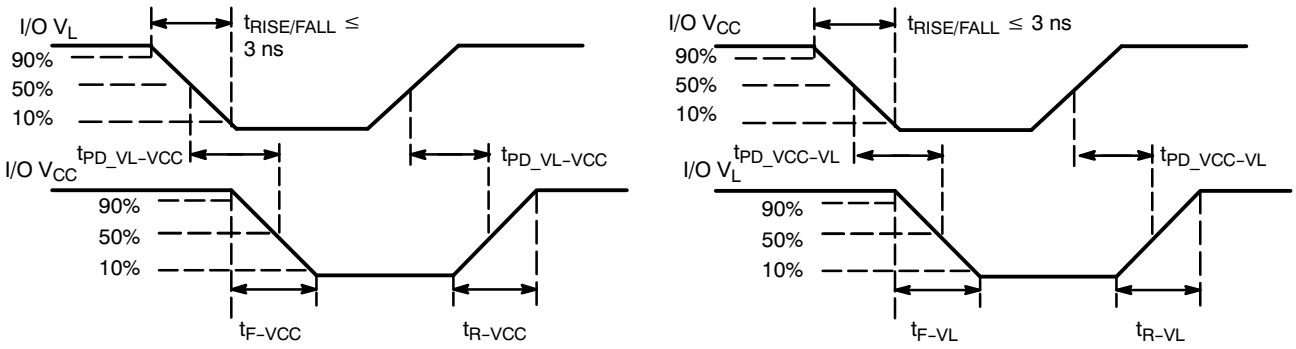
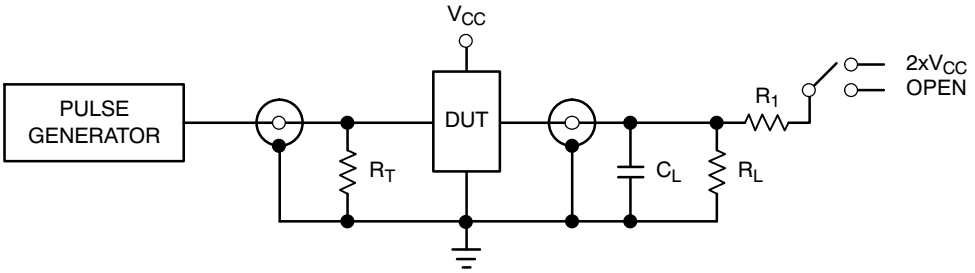


Figure 6. Definition of Timing Specification Parameters



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 x V_{CC}

C_L = 15 pF or equivalent (Includes jig and probe capacitance)
R_L = R_1 = 50 kΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 7. Test Circuit for Enable/Disable Time Measurement

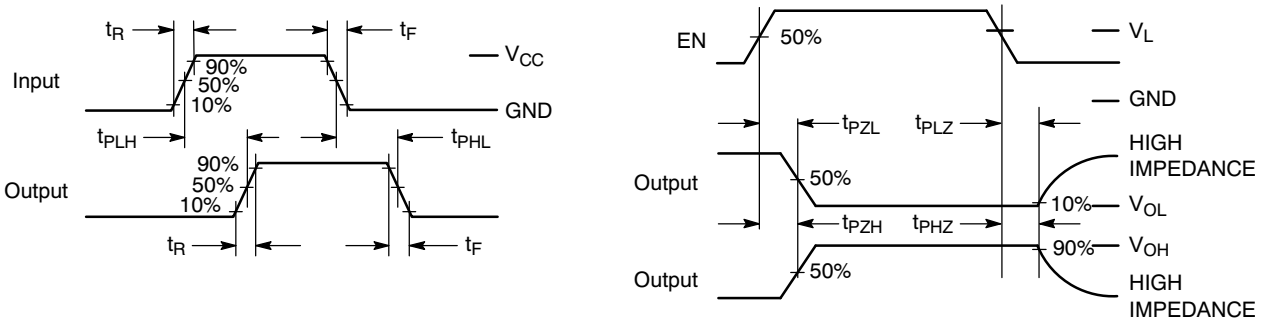


Figure 8. Timing Definitions for Propagation Delays and Enable/Disable Measurement

APPLICATIONS INFORMATION

Level Translator Architecture

The NLSX3373 auto sense translator provides bi−directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages, V_L and V_{CC}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the V_L to the V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC}. In a similar manner, the V_{CC} to V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L.

The NLSX3373 consists of two bi−directional channels that independently determine the direction of the data flow without requiring a directional pin. The one−shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high−to−low and low−to−high transitions.

Each input/output channel has an internal 10 kΩ pull. The magnitude of the pullup resistors can be reduced by connecting external resistors in parallel to the internal 10 kΩ resistors.

Input Driver Requirements

The rise (t_R) and fall (t_F) timing parameters of the open drain outputs depend on the magnitude of the pull−up resistors. In addition, the propagation times (t_{PD}), skew (t_{PSKEW}) and maximum data rate depend on the impedance of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 kΩ.

Enable Input (EN)

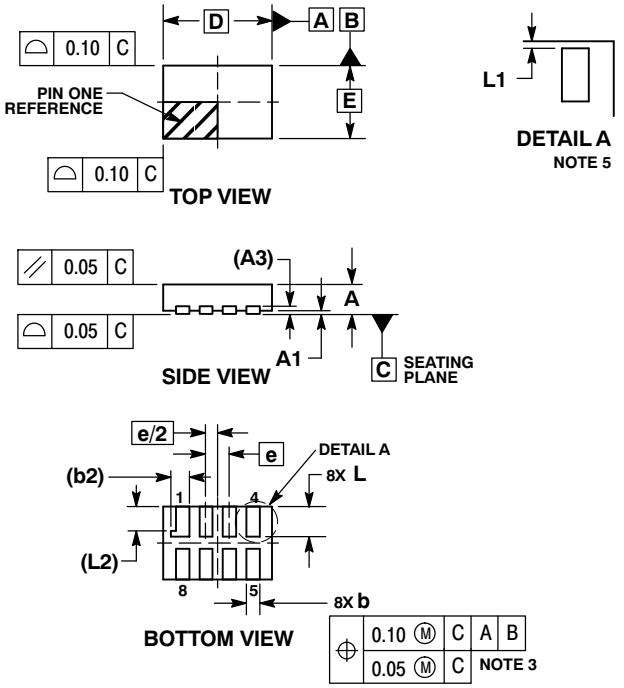
The NLSX3373 has an Enable pin (EN) that provides tri−state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CC} and I/O V_L pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Overvoltage Tolerant (OVT) protection.

Power Supply Guidelines

During normal operation, supply voltage V_L should be less than or equal to V_{CC}. The sequencing of the power supplies will not damage the device during the power up operation. In addition, the I/O V_{CC} and I/O V_L pins are in the high impedance state if either supply voltage is equal to 0 V. For optimal performance, 0.01 μF to 0.1 μF decoupling capacitors should be used on the V_L and V_{CC} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

PACKAGE DIMENSIONS

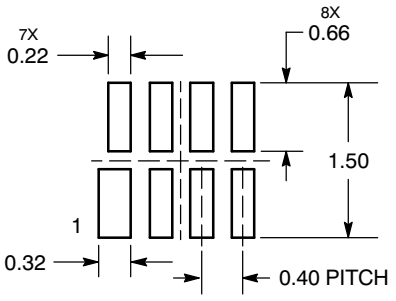
UDFN8 1.8 x 1.2, 0.4P
CASE 517AJ−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
b2	0.30 REF	
D	1.80 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.45	0.55
L1	0.00	0.03
L2	0.40 REF	

MOUNTING FOOTPRINT
SOLDERMASK DEFINED



DIMENSIONS: MILLIMETERS

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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